Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

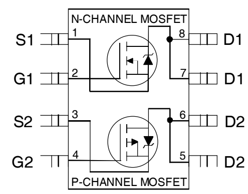
International
IOR Rectifier

PD - 95179

IRF7307PbF

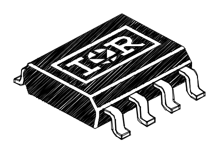
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



Top View

	N-Ch	P-Ch
V_{DSS}	20V	-20V
$R_{DS(on)}$	0.050Ω	0.090Ω


SO-8

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ T_A = 25°C	10 Sec. Pulse Drain Current, V_{GS} @ 4.5V	5.7	-4.7	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	5.2	-4.3	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	4.1	-3.4	
I_{DM}	Pulsed Drain Current ①	21	-17	
P_D @T_A = 25°C	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 12		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	–––	62.5	°C/W

10/7/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-20	—	—		V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.044	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.012	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	Ω	V_{GS} = 4.5V, I_D = 2.6A ③
			—	—	0.070		V_{GS} = 2.7V, I_D = 2.2A ③
		P-Ch	—	—	0.090		V_{GS} = -4.5V, I_D = -2.2A ③
			—	—	0.140		V_{GS} = -2.7V, I_D = -1.8A ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.70	—	—	V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-0.70	—	—		V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	N-Ch	8.30	—	—	S	V_{DS} = 15V, I_D = 2.6A ③
		P-Ch	4.00	—	—		V_{DS} = -15V, I_D = -2.2A ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
		P-Ch	—	—	-1.0		V_{DS} = -16V, V_{GS} = 0V,
		N-Ch	—	—	25		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
		P-Ch	—	—	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	±100		V_{GS} = ± 12V
Q_g	Total Gate Charge	N-Ch	—	—	20	nC	N-Channel I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V ③ P-Channel I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V
		P-Ch	—	—	22		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.2		
		P-Ch	—	—	3.3		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	8.0		
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	9.0	—	ns	N-Channel V_{DD} = 10V, I_D = 2.6A, R_G = 6.0Ω, R_D = 3.8Ω ③ P-Channel V_{DD} = -10V, I_D = -2.2A, R_G = 6.0Ω, R_D = 4.5Ω
		P-Ch	—	8.4	—		
t_r	Rise Time	N-Ch	—	42	—		
		P-Ch	—	26	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	32	—		
		P-Ch	—	51	—		
t_f	Fall Time	N-Ch	—	51	—		
		P-Ch	—	33	—		
L_D	Internal Drain Inductace	N-P	—	4.0	—	nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{iss}	Input Capacitance	N-Ch	—	660	—	pF	N-Channel V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz ③ P-Channel V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz
		P-Ch	—	610	—		
C_{oss}	Output Capacitance	N-Ch	—	280	—		
		P-Ch	—	310	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	140	—		
		P-Ch	—	170	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.5	A	
		P-Ch	—	—	-2.5		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	21		
		P-Ch	—	—	-17		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
		P-Ch	—	—	-1.0		T_J = 25°C, I_S = -1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	N-Ch	—	29	44	ns	N-Channel T_J = 25°C, I_F = 2.6A, di/dt = 100A/μs ③ P-Channel T_J = 25°C, I_F = -2.2A, di/dt = 100A/μs
		P-Ch	—	56	84		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	22	33	nC	
		P-Ch	—	71	110		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel $I_{SD} \le$ 2.6A, di/dt $\le$ 100A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C
P-Channel $I_{SD} \le$ -2.2A, di/dt $\le$ 50A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

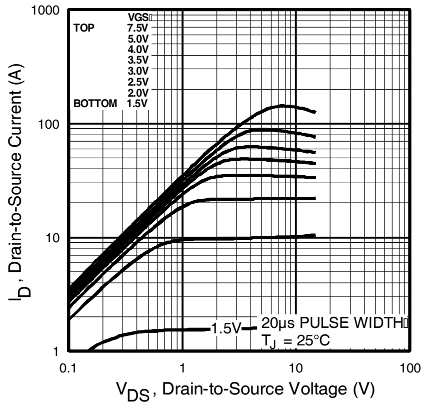


Fig 1. Typical Output Characteristics

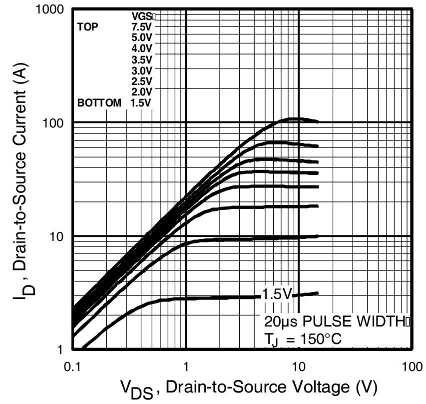


Fig 2. Typical Output Characteristics

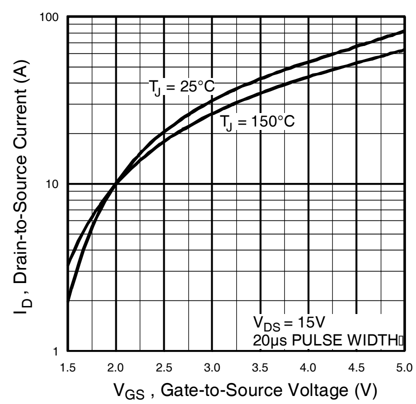


Fig 3. Typical Transfer Characteristics

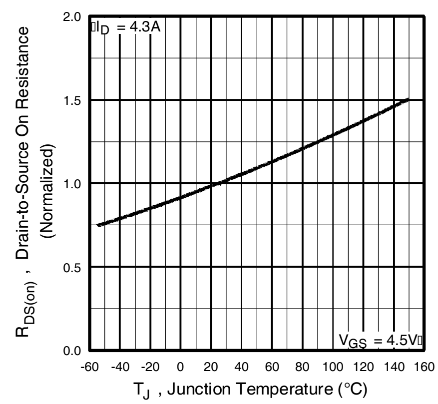


Fig 4. Normalized On-Resistance Vs. Temperature

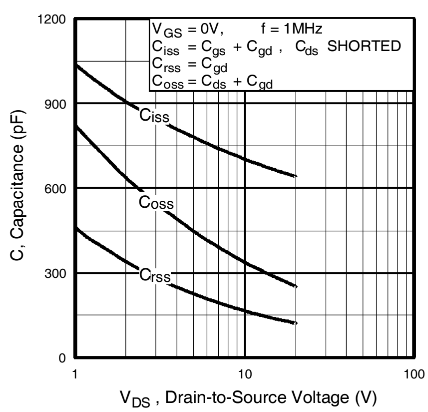


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

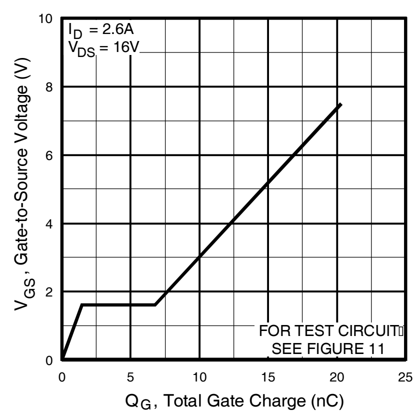


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

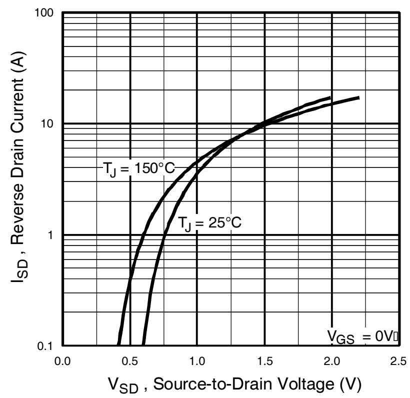


Fig 7. Typical Source-Drain Diode Forward Voltage

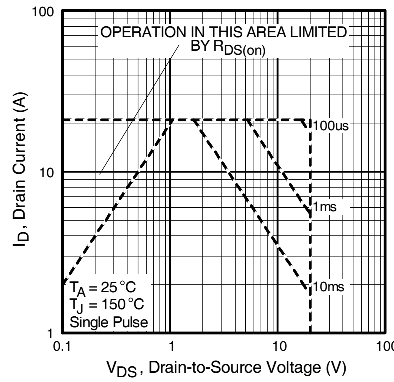


Fig 8. Maximum Safe Operating Area

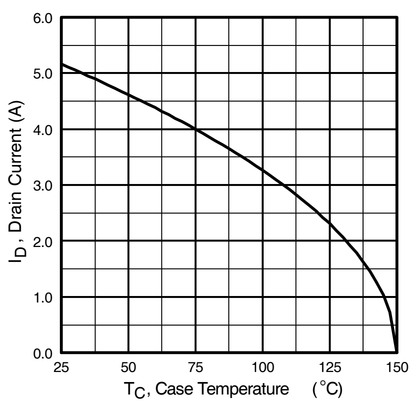


Fig 9. Maximum Drain Current Vs. Ambient Temperature

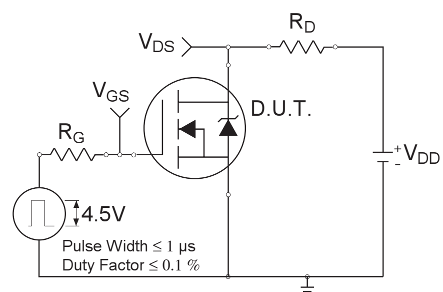


Fig 10a. Switching Time Test Circuit

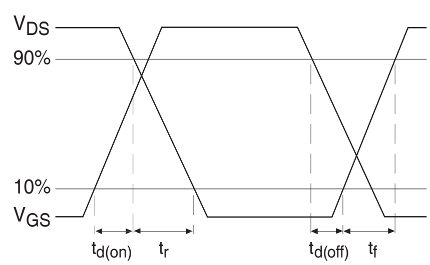


Fig 10b. Switching Time Waveforms

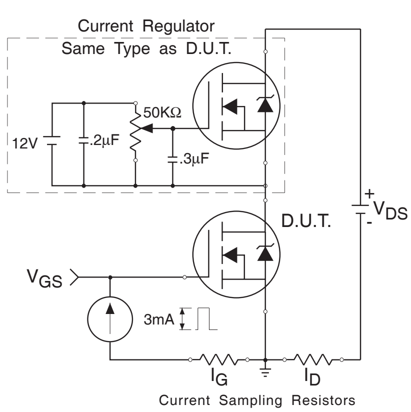


Fig 11a. Gate Charge Test Circuit

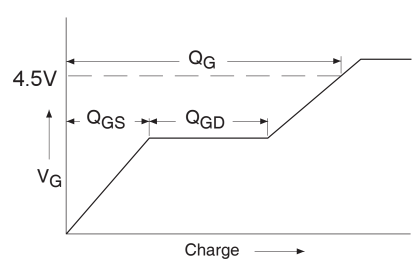


Fig 11b. Basic Gate Charge Waveform

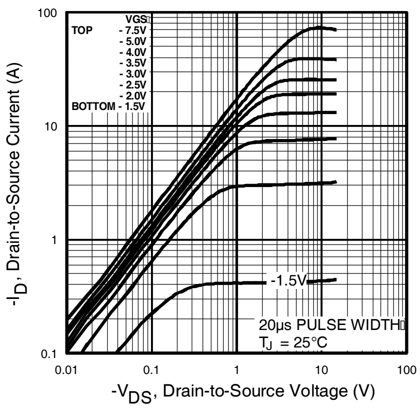


Fig 12. Typical Output Characteristics

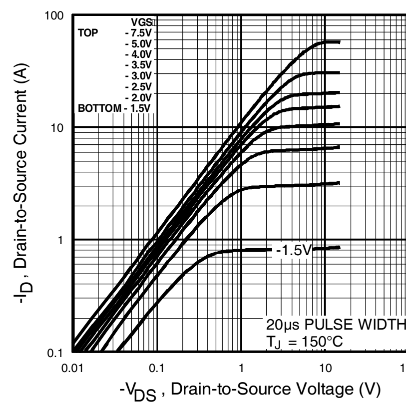


Fig 13. Typical Output Characteristics

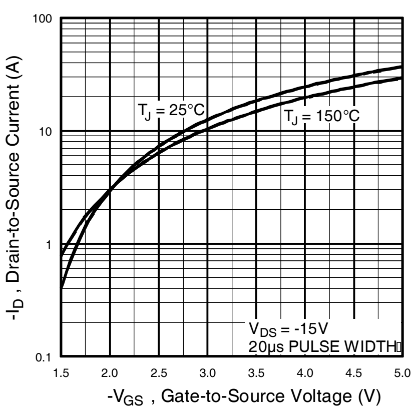


Fig 14. Typical Transfer Characteristics

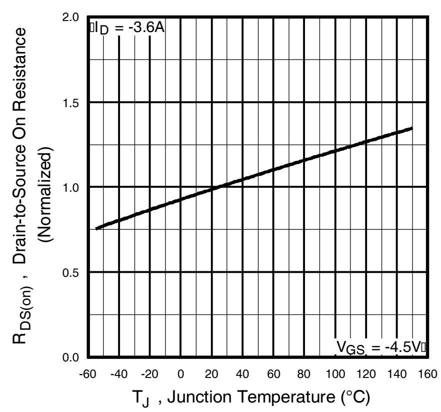


Fig 15. Normalized On-Resistance Vs. Temperature

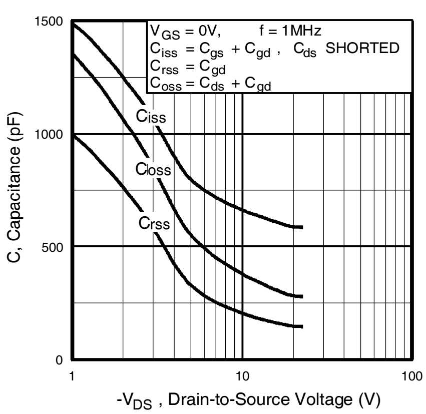


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

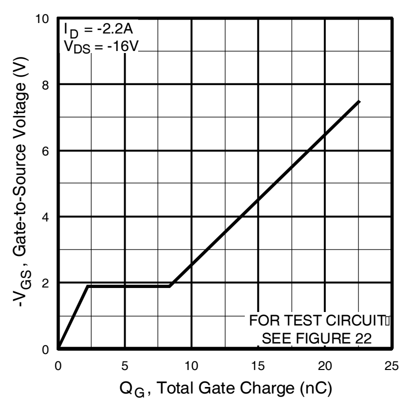


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

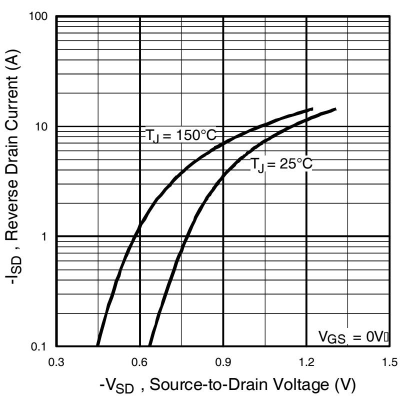


Fig 18. Typical Source-Drain Diode Forward Voltage

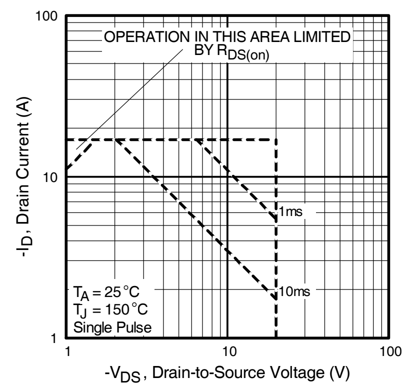


Fig 19. Maximum Safe Operating Area

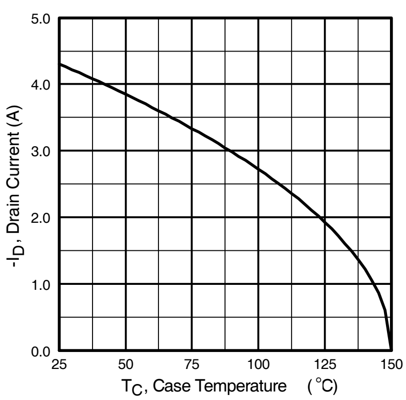


Fig 20. Maximum Drain Current Vs. Ambient Temperature

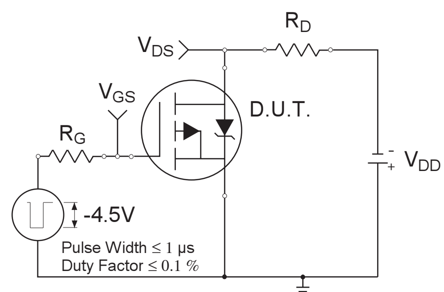


Fig 21a. Switching Time Test Circuit

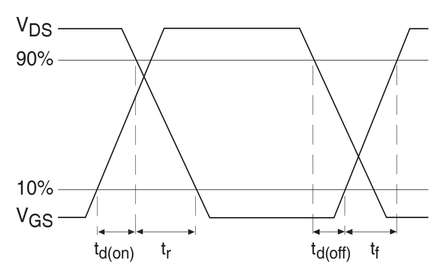


Fig 21b. Switching Time Waveforms

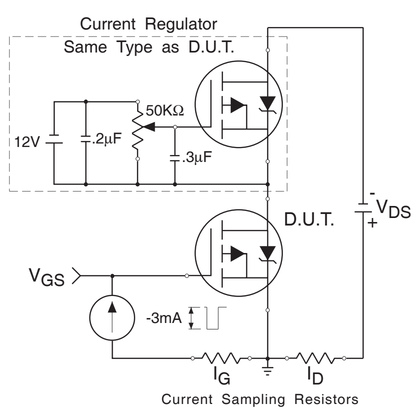


Fig 22a. Gate Charge Test Circuit

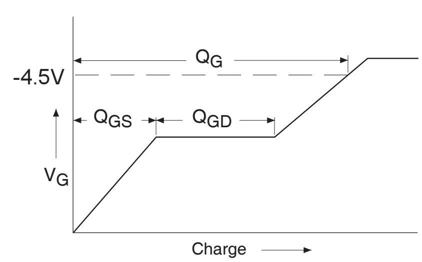


Fig 22b. Basic Gate Charge Waveform

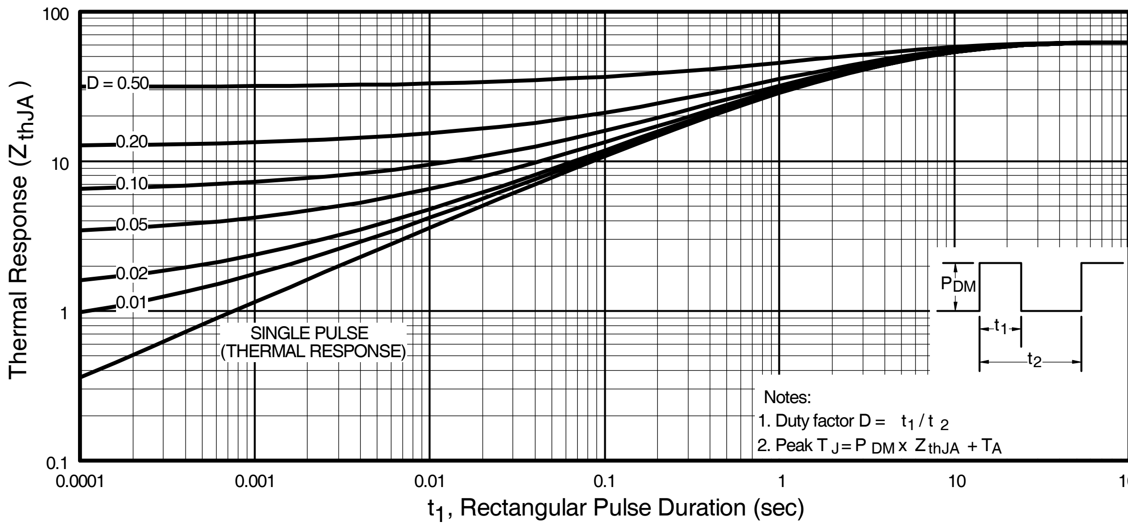
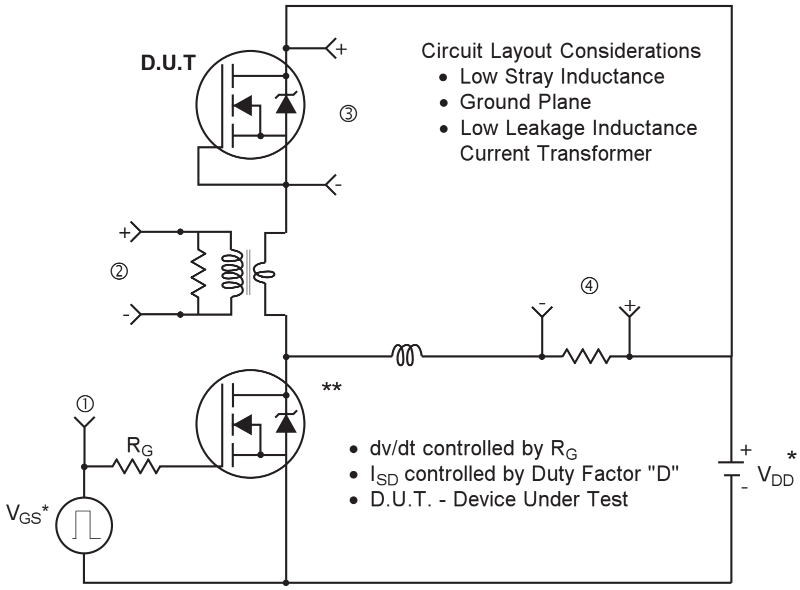


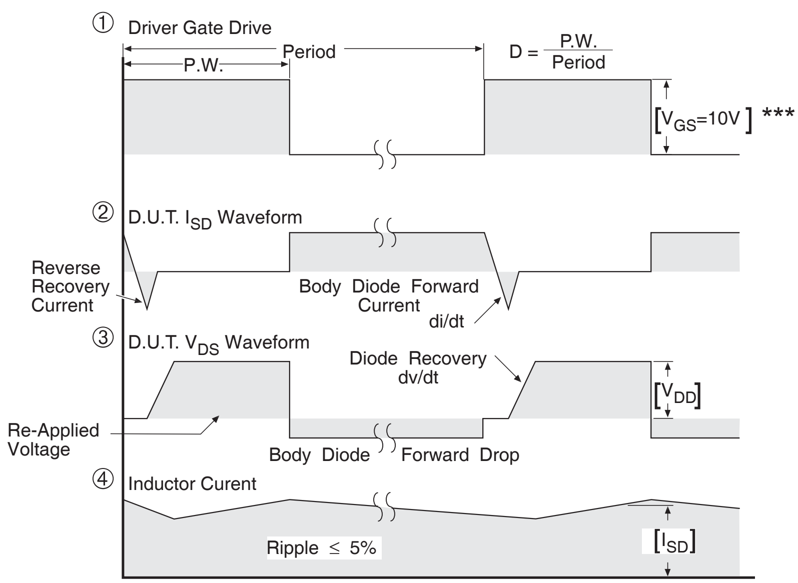
Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

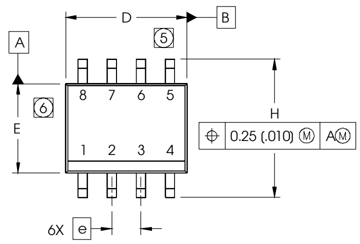


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

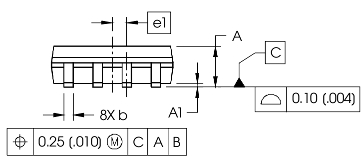
Fig 24. For N and P Channel HEXFETS

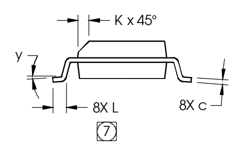
SO-8 Package Outline

Dimensions are shown in milimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

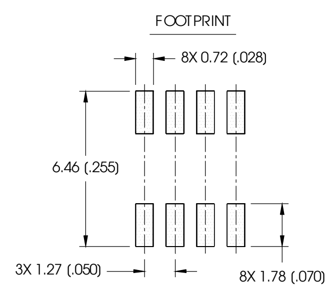




NOTES:

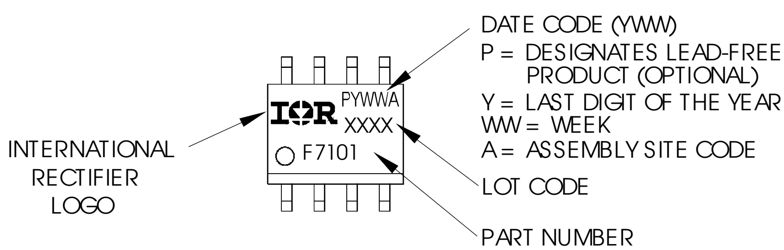
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



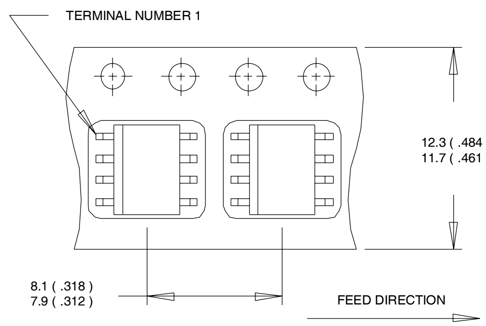
SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

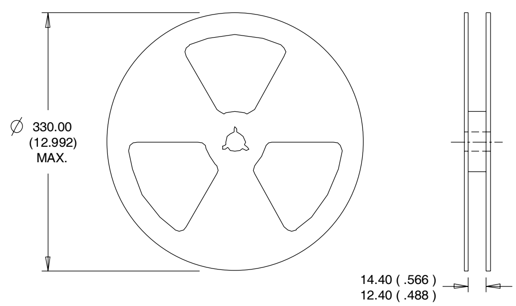


SO-8 Tape and Reel

Dimensions are shown in milimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.10/04