Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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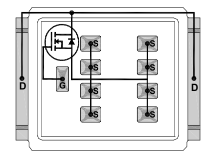
DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$
100V min	±20V max	2.8mΩ @ 10V
$Q_{g\ tot}$	Q_{gd}	$V_{gs(th)}$
200nC	110nC	2.7V



L8

DirectFET™ ISOMETRIC

Applications

- RoHS Compliant, Halogen Free ②
- Lead-Free (Qualified up to 260°C Reflow) ①
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①
- Industrial Qualified

Applicable DirectFET Outline and Substrate Outline ①

SB	SC			M2	M4		L4	L6	L8	

Description

The IRF7769L1TRPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has a footprint smaller than a D2PAK and only 0.7 mm profile. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET™ package allows dual sided cooling to maximize thermal transfer in power systems.
The IRF7769L1TRPbF is optimized for high frequency switching and synchronous rectification applications. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance power converters.

Ordering Information

Part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF7769L1TRPbF	DirectFET Large Can	Tape and Reel	4000	"TR" suffix

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)④	124	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)④	88	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)③	20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited) ④	375	
I_{DM}	Pulsed Drain Current⑤	500	
E_{AS}	Single Pulse Avalanche Energy ⑥	260	mJ
I_{AR}	Avalanche Current ⑤	74	A

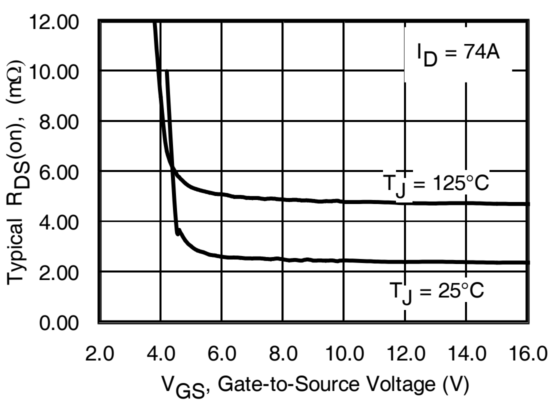


Fig 1. Typical On-Resistance vs. Gate Voltage

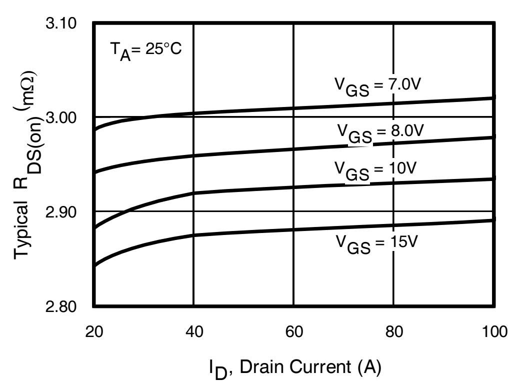


Fig 2. Typical On-Resistance vs. Drain Current

Notes
① Click on this section to link to the appropriate technical paper.
② Click on this section to link to the DirectFET Website.
③ Surface mounted on 1 in. square Cu board, steady state.
④ TC measured with thermocouple mounted to top (Drain) of part.
⑤ Repetitive rating; pulse width limited by max. junction temperature.
⑥ Starting T_J = 25°C, L = 0.09mH, R_G = 25Ω, I_{AS} = 74A.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.02	——	V/°C	Reference to 25°C, I_D = 2mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.8	3.5	mΩ	V_{GS} = 10V, I_D = 74A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.7	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	——	-10	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 100 V, V_{GS} = 0V
		——	——	250		V_{DS} = 80V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
gfs	Forward Transconductance	410	——	——	S	V_{DS} = 25V, I_D = 74A
Q_g	Total Gate Charge	——	200	300	nC	V_{DS} = 50V
Q_{gs1}	Pre– Vth Gate-to-Source Charge	——	30	——		V_{GS} = 10V
Q_{gs2}	Post– Vth Gate-to-Source Charge	——	9.0	——		I_D = 74A
Q_{gd}	Gate-to-Drain Charge	——	110	165		See Fig.9
Q_{godr}	Gate Charge Overdrive	——	51	——		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	——	119	——		
Q_{oss}	Output Charge	——	53	——	nC	V_{DS} = 16V,V_{GS} = 0V
R_G	Gate Resistance	——	1.5	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	44	——	ns	V_{DD} = 50V, V_{GS} = 10V ⑦
t_r	Rise Time	——	32	——		I_D = 74A
$t_{d(off)}$	Turn-Off Delay Time	——	92	——		R_G= 1.8Ω
t_f	Fall Time	——	41	——		
C_{iss}	Input Capacitance	——	11560	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1240	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	590	——		f = 1.0MHz
C_{oss}	Output Capacitance	——	6665	——		V_{GS}=0V, V_{DS} = 1.0V, f =1.0MHz
C_{oss}	Output Capacitance	——	690	——		V_{GS}=0V, V_{DS} = 80V, f =1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	124	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	——	——	500		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 74A,V_{GS} = 0V ⑦
t_{rr}	Reverse Recovery Time	——	75	112	ns	T_J = 25°C ,I_F = 74A,V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	——	220	330	nC	di/dt = 100A/μs ⑦

Notes:
⑤ Repetitive rating; pulse width limited by max. junction temperature.
⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
P_D @T_C = 25°C	Power Dissipation ④	125	W
P_D @T_C = 100°C	Power Dissipation ④	63	
P_D @T_A = 25°C	Power Dissipation ③	3.3	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R_{qJA}	Junction-to-Ambient ③	——	45	°C/W
R_{qJA}	Junction-to-Ambient ⑧	12.5	——	
R_{qJA}	Junction-to-Ambient ⑨	20	——	
R_{qJC}	Junction-to-Can ④⑩	——	1.2	
$R_{qJA-PCB}$	Junction-to-PCB Mounted	——	0.4	

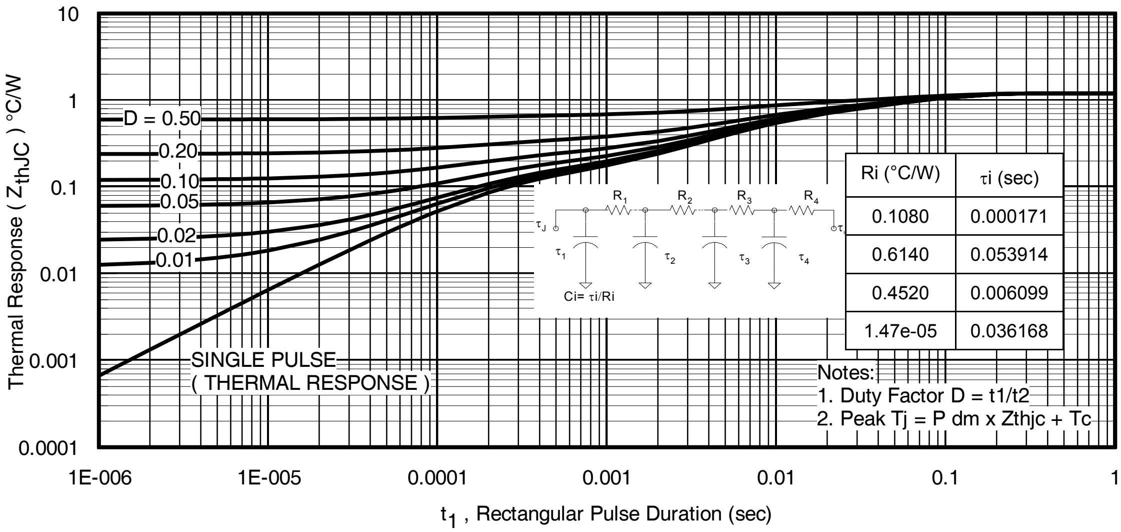
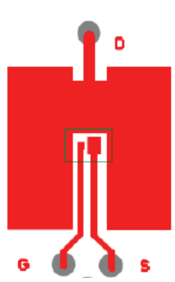


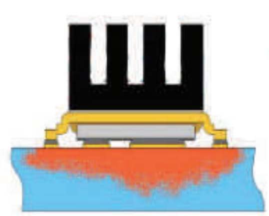
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case

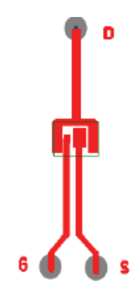
Notes:

③ Surface mounted on 1 in. square Cu board, steady state.
④ T_C measured with thermocouple incontact with top (Drain) of part.
⑤ Repetitive rating; pulse width limited by max. junction temperature.
⑧ Used double sided cooling, mounting pad with large heatsink.
⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
⑩ R_θ is measured at T_J of approximately 90°C.



③ Surface mounted on 1 in. square Cu board (still air).





⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

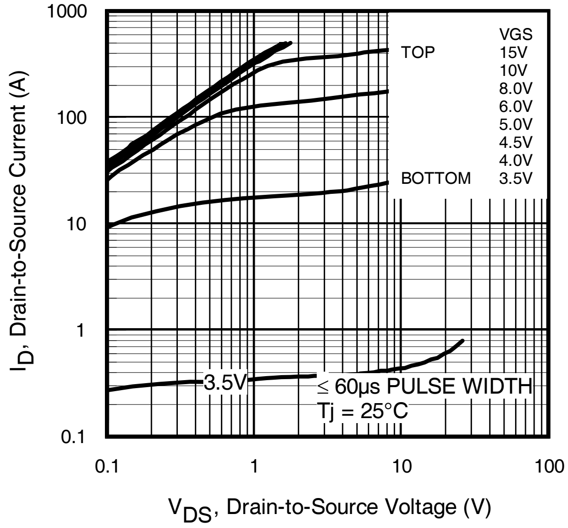


Fig 4. Typical Output Characteristics

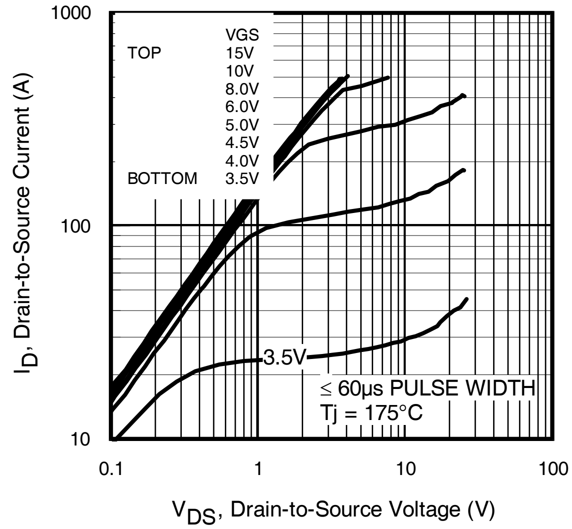


Fig 5. Typical Output Characteristics

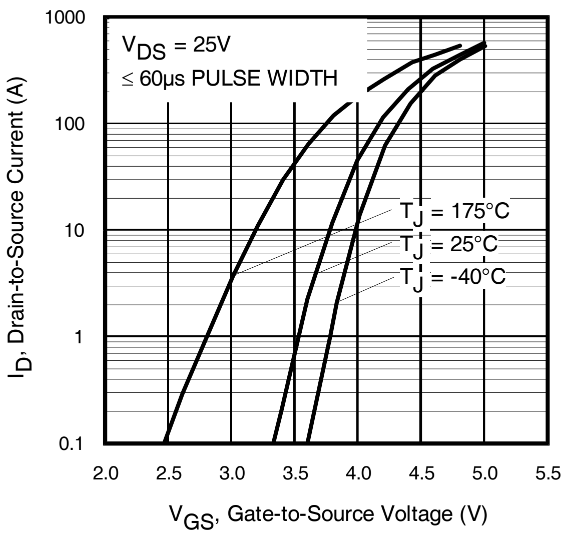


Fig 6. Typical Transfer Characteristics

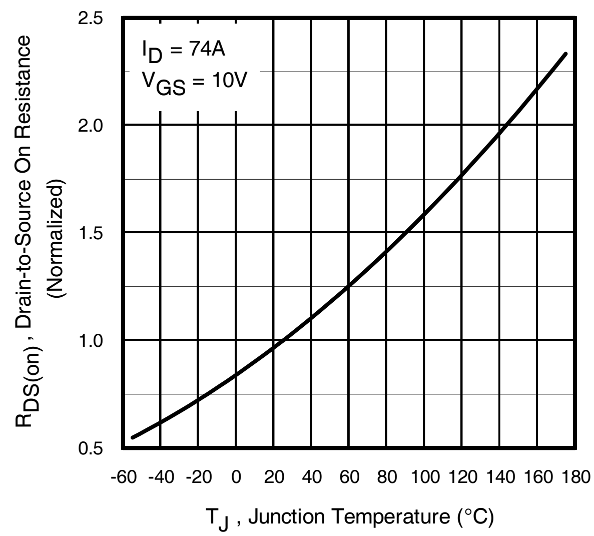


Fig 7. Normalized On-Resistance vs. Temperature

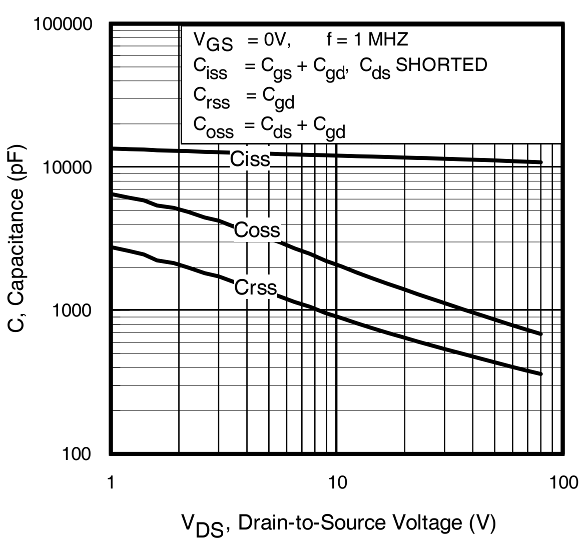


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

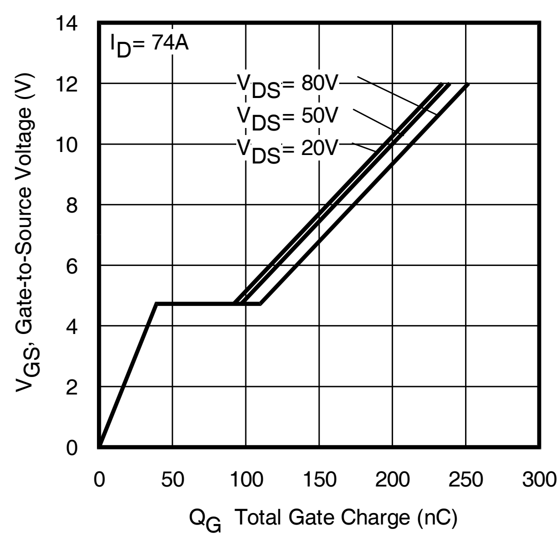


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

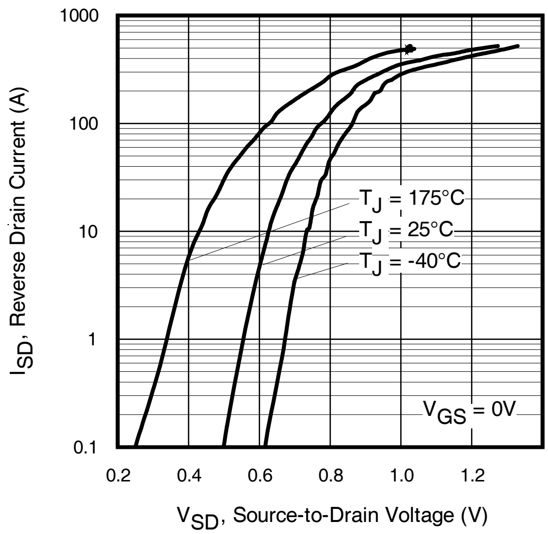


Fig 10. Typical Source-Drain Diode Forward Voltage

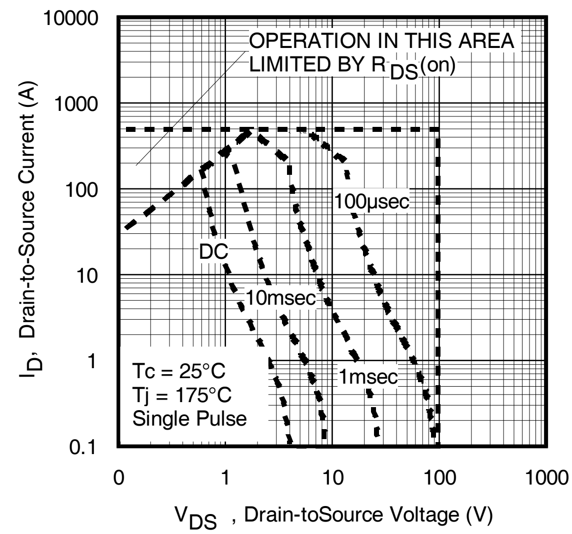


Fig 11. Maximum Safe Operating Area

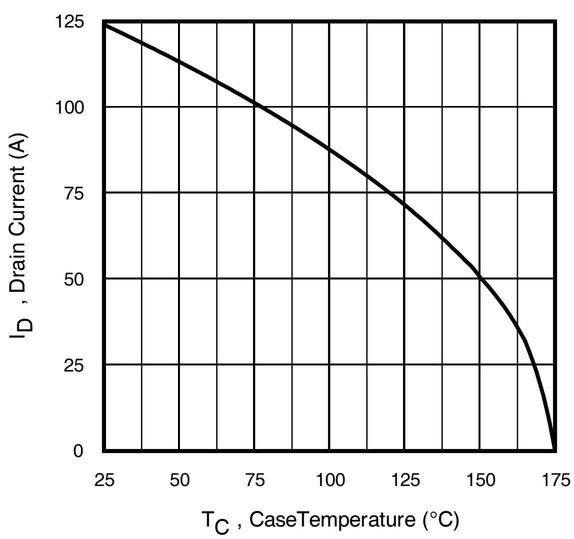


Fig 12. Maximum Drain Current vs. Case Temperature

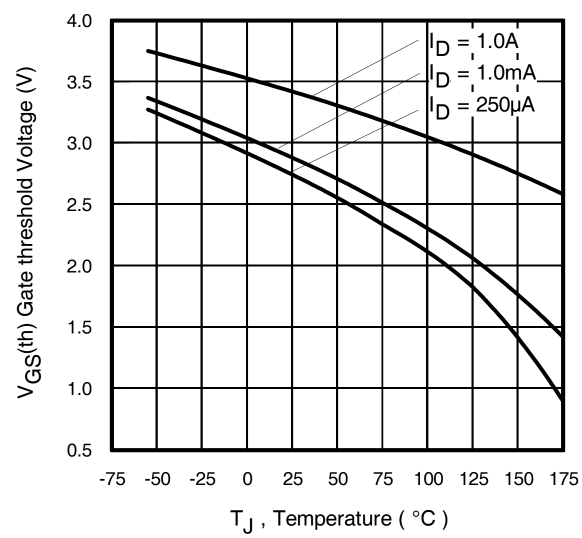


Fig 13. Typical Threshold Voltage vs. Junction Temperature

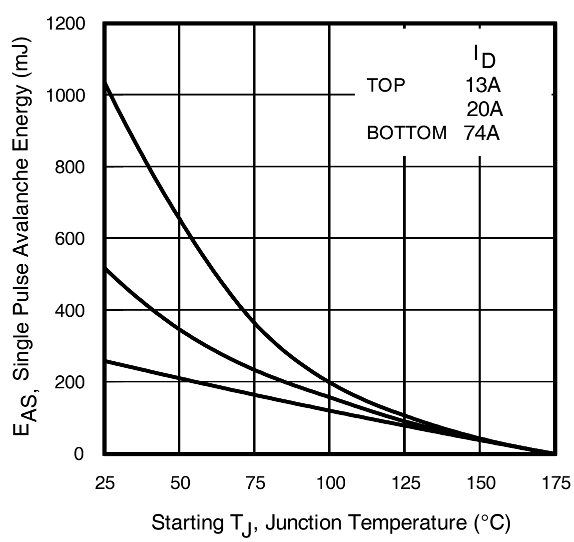


Fig 14. Maximum Avalanche Energy vs. Drain Current

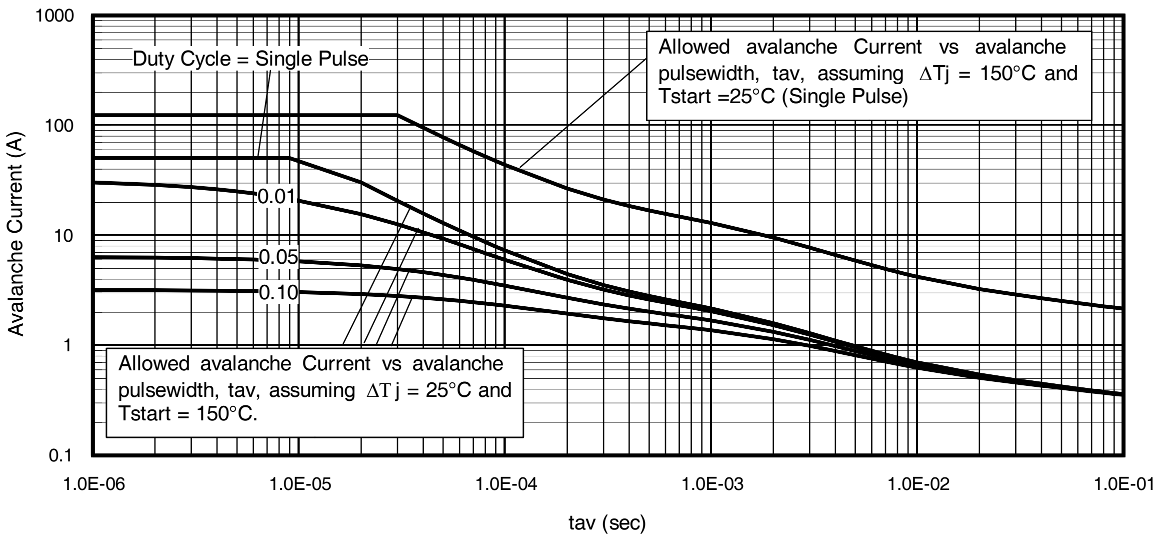


Fig 15. Typical Avalanche Current vs. Pulse width

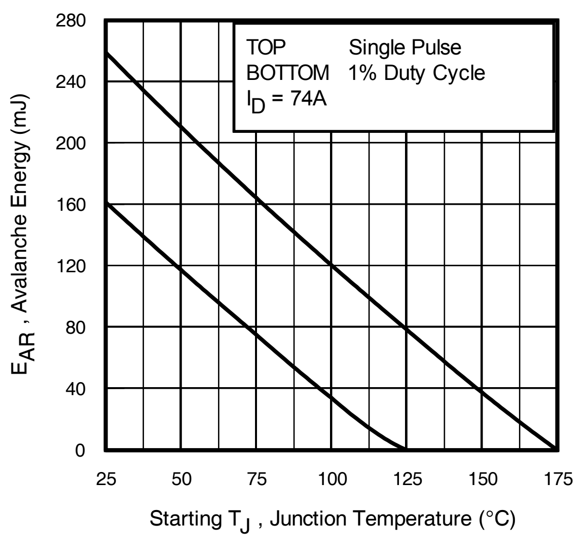
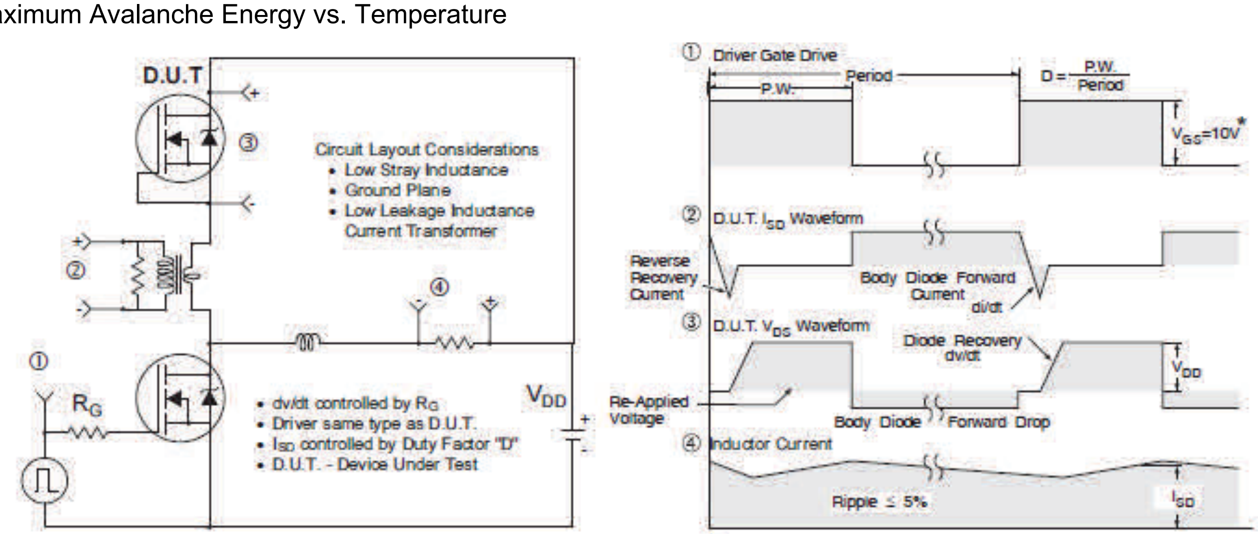


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005)

1.Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 3)

$$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$



* V_{GS} = 5V for Logic Level Devices

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

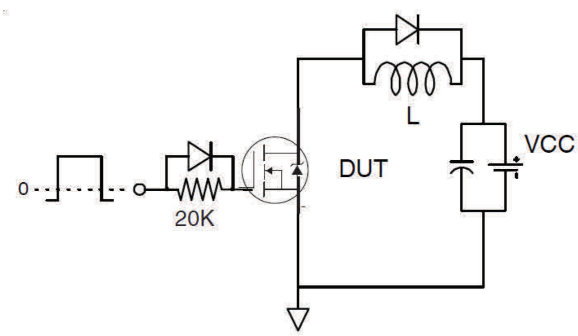


Fig 18a. Gate Charge Test Circuit

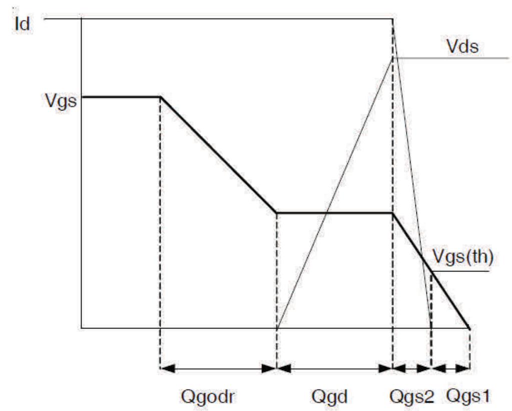


Fig 18b. Gate Charge Waveform

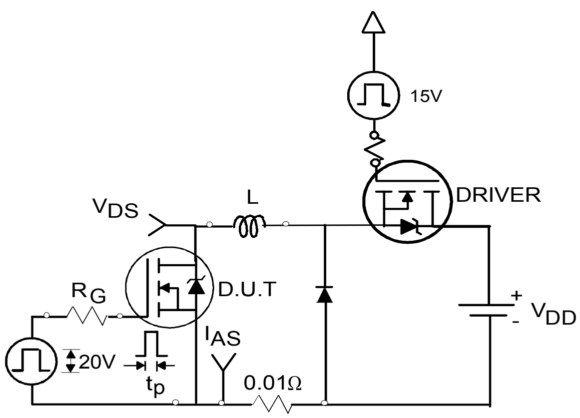


Fig 19a. Unclamped Inductive Test Circuit

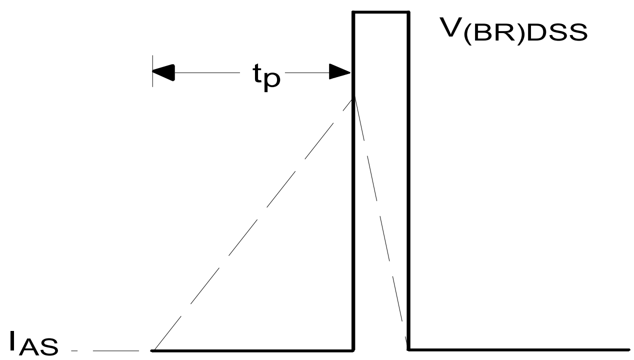


Fig 19b. Unclamped Inductive Waveforms

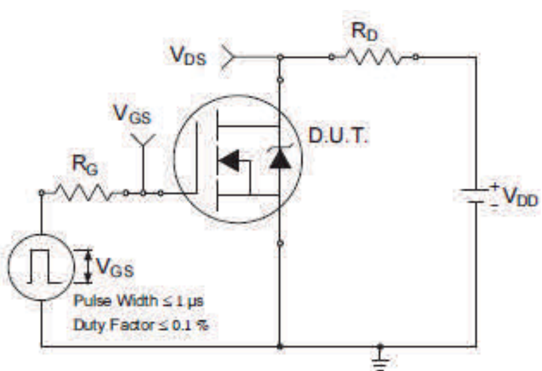


Fig 20a. Switching Time Test Circuit

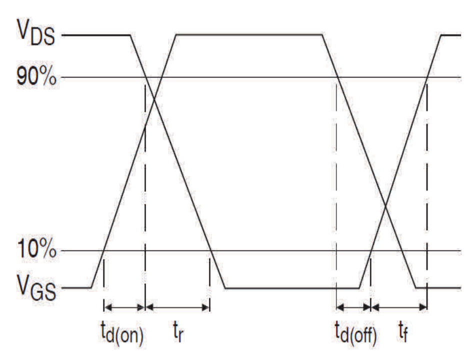
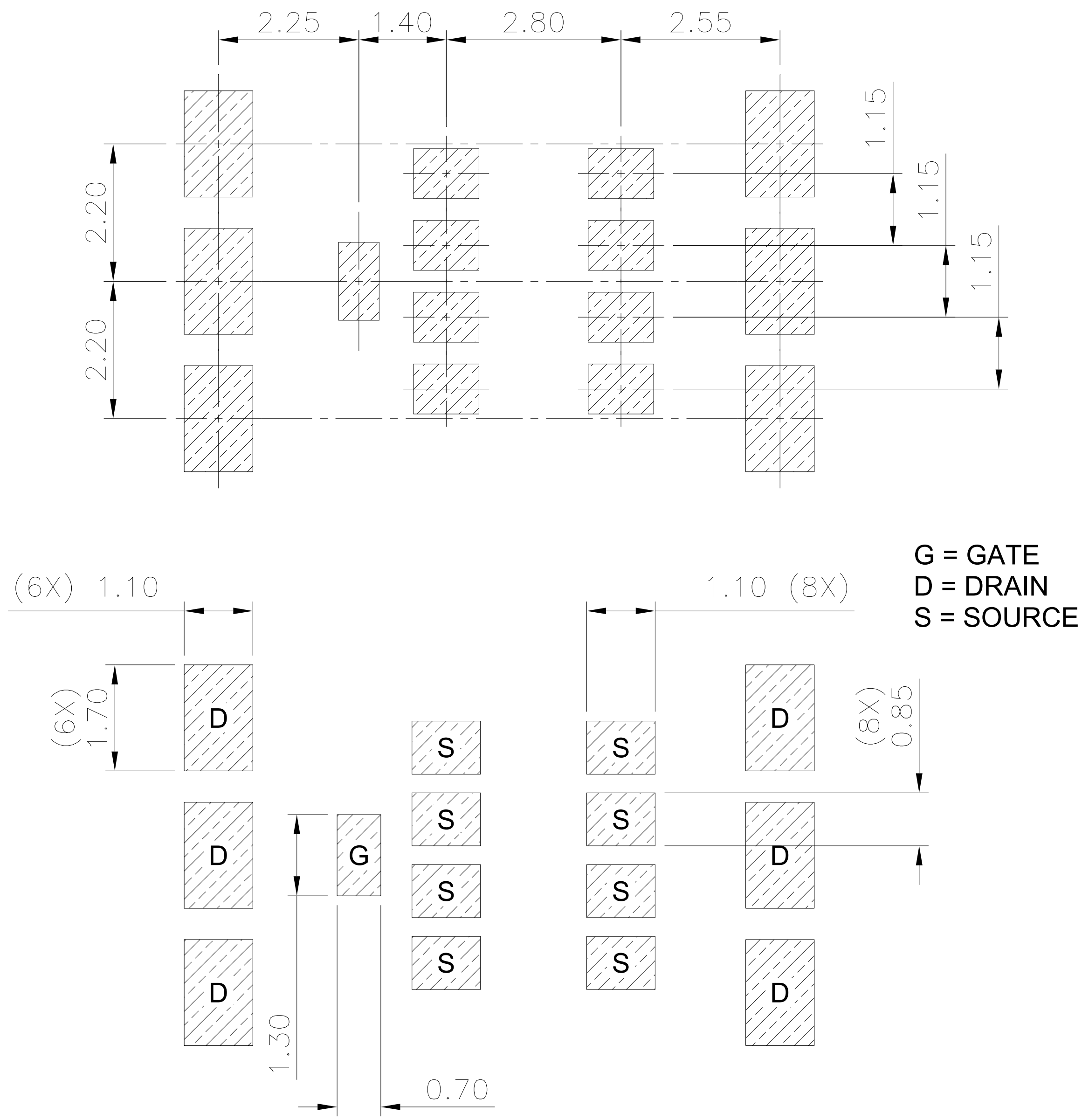


Fig 20b. Switching Time Waveforms

DirectFET™ Board Footprint, L8 Outline
(Large Size Can, 8-Source Pads)

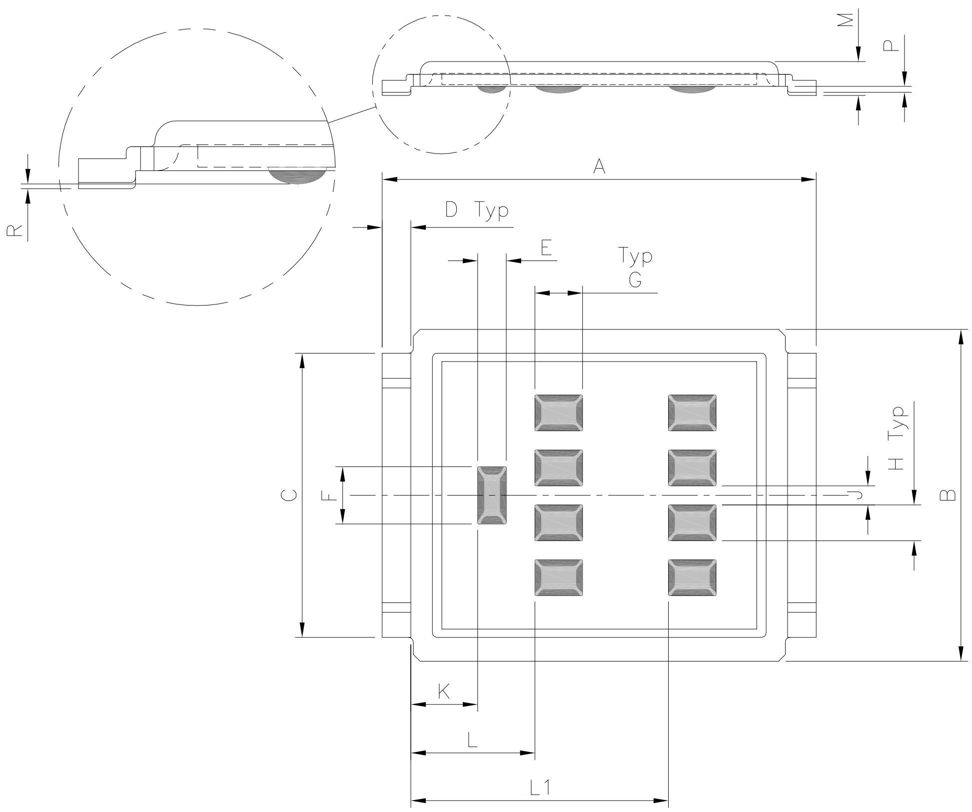
Please see DirectFET™ application note AN-1035 for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



Note: For the most current drawing please refer to website at http://www.irf.com/package/

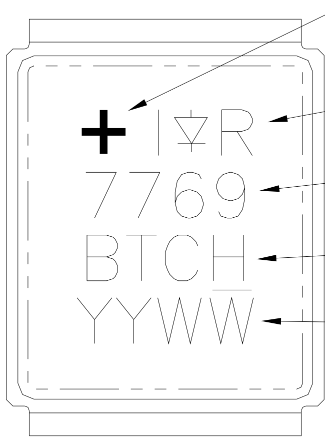
DirectFET® Outline Dimension, L8 Outline (Large Size Can, 8-Source Pads)

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



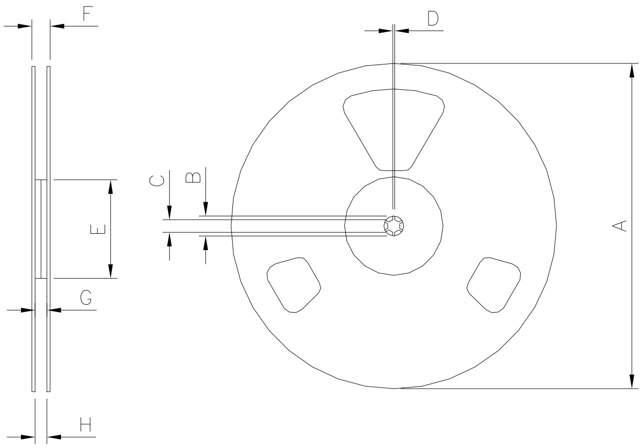
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.039	0.040
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.35	1.45	0.053	0.057
L	2.55	2.65	0.100	0.104
L1	5.35	5.45	0.211	0.215
M	0.68	0.74	0.027	0.029
P	0.09	0.17	0.003	0.007
R	0.02	0.08	0.001	0.003

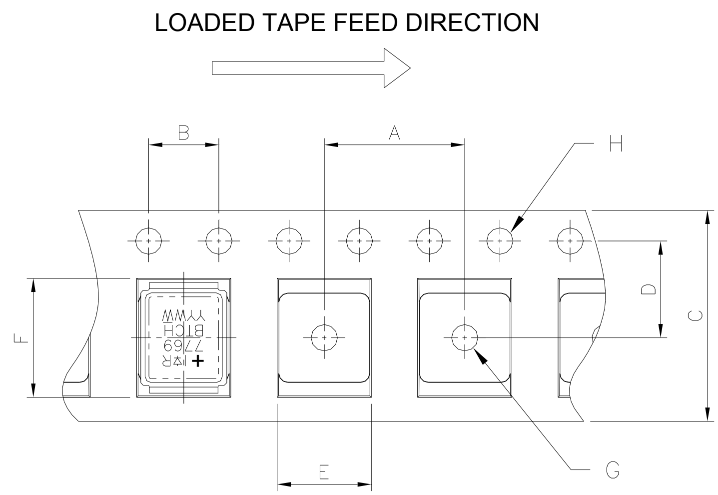
DirectFET™ Part Marking



Note: For the most current drawing please refer to website at http://www.irf.com/package/

DirectFET™ Tape & Reel Dimension (Showing component orientation).





NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts. (ordered as IRF7769L1TRPBF).

REEL DIMENSIONS				
STANDARD OPTION **(QTY 4000)**				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.00	N.C	12.992	N.C
B	20.20	N.C	0.795	N.C
C	12.80	13.20	0.504	0.520
D	1.50	N.C	0.059	N.C
E	99.00	100.00	3.900	3.940
F	N.C	22.40	N.C	0.880
G	16.40	18.40	0.650	0.720
H	15.90	19.40	0.630	0.760

NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	11.90	12.10	4.69	0.476
B	3.90	4.10	0.154	0.161
C	15.90	16.30	0.623	0.642
D	7.40	7.60	0.291	0.299
E	7.20	7.40	0.283	0.291
F	9.90	10.10	0.390	0.398
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to website at http://www.irf.com/package/

Qualification Information

Qualification Level	Industrial * (per JEDEC JESD47F† guidelines)	
Moisture Sensitivity Level	DirectFET (Large -Can)	MSL1 (per JEDEC J-STD-020D†)
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

* Industrial qualification standards except autoclave test conditions.

Revision History

Date	Comments
2/13/2013	• TR1 option removed and Tape & Reel Info updated accordingly. Hyperlinks added throw-out the document
10/14/2016	• Changed datasheet with "Infineon" logo –all pages. • Corrected Outline Dimension, L8 Outline on page 9. • Added disclaimer on last page.

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