Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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International
IOR Rectifier

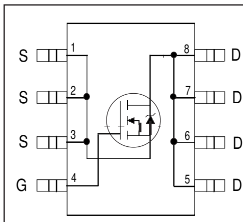
PD – 95290

IRF7807PbF
IRF7807APbF

HEXFET® Chip-Set for DC-DC Converters

- N Channel Application Specific MOSFETs
- Ideal for Mobile DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Lead-Free


SO-8



Top View

Description

These new devices employ advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make them ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

A pair of IRF7807 devices provides the best cost/ performance solution for system voltages, such as 3.3V and 5V.

Device Features

	IRF7807	IRF7807A
Vds	30V	30V
Rds(on)	25mΩ	25mΩ
Qg	17nC	17nC
Qsw	5.2nC	
Qoss	16.8nC	16.8nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7807	IRF7807A	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain or Source	25°C	I_D	8.3	8.3	A
Current ($V_{GS} \geq 4.5V$)	70°C		6.6	6.6	
Pulsed Drain Current①		I_{DM}	66	66	
Power Dissipation	25°C	P_D	2.5		W
	70°C		1.6		
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150		°C
Continuous Source Current (Body Diode)①		I_S	2.5	2.5	A
Pulsed source Current		I_{SM}	66	66	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	50	°C/W

Electrical Characteristics

Parameter		IRF7807 Min	IRF7807 Typ	IRF7807 Max	IRF7807A Min	IRF7807A Typ	IRF7807A Max	Units	Conditions
Drain-to-Source Breakdown Voltage*	$V_{(BR)DSS}$	30	–	–	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance*	$R_{DS}(on)$		17	25		17	25	mΩ	V_{GS} = 4.5V, I_D = 7A②
Gate Threshold Voltage*	$V_{GS}(th)$	1.0			1.0			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current*	I_{DSS}			30			30	µA	V_{DS} = 24V, V_{GS} = 0
				150			150		V_{DS} = 24V, V_{GS} = 0, Tj = 100°C
Gate-Source Leakage Current*	I_{GSS}			±100			±100	nA	V_{GS} = ±12V
Total Gate Charge*	Q_g		12	17		12	17	nC	V_{GS} = 5V, I_D = 7A
Pre-Vth Gate-Source Charge	Q_{gs1}		2.1			2.1			V_{DS} = 16V, I_D = 7A
Post-Vth Gate-Source Charge	Q_{gs2}		0.76			0.76			
Gate to Drain Charge	Q_{gd}		2.9			2.9			
Switch Charge* (Q_{gs2} + Q_{gd})	Q_{SW}		3.66	5.2		3.66			
Output Charge*	Q_{oss}		14	16.8		14	16.8		V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_g		1.2			1.2		Ω	
Turn-on Delay Time	$t_d(on)$		12			12		ns	V_{DD} = 16V
Rise Time	t_r		17			17			I_D = 7A
Turn-off Delay Time	t_d (off)		25			25			R_g = 2Ω
Fall Time	t_f		6			6			V_{GS} = 4.5V Resistive Load

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.2			1.2	V	I_S = 7A②, V_{GS} = 0V
Reverse Recovery Charge④	Q_{rr}		80			80		nC	di/dt = 700A/µs V_{DS} = 16V, V_{GS} = 0V, I_S = 7A
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		50			50			di/dt = 700A/µs (with 10BQ040) V_{DS} = 16V, V_{GS} = 0V, I_S = 7A

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 300 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Typ = measured - Q_{oss}
* Devices are 100% tested to these parameters.

Power MOSFET Selection for DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 1.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to I_{dmax} (t2) at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

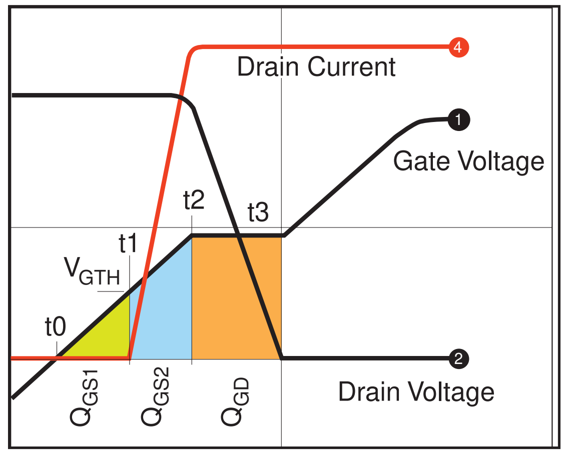


Figure 1: Typical MOSFET switching waveform

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^{*}_{output}$$

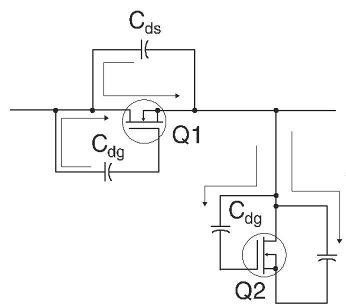
$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

Spice model for IRF7807 can be downloaded in machine readable format at www.irf.com.



$$C_{oss} = C_{dg} + C_{ds}$$
$$\Delta Q_{oss} = C_{oss} \times \Delta V_{in}$$

Figure 2: Q_{oss} Characteristic

Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 3 and Fig 4). In these applications the same MOSFET IRF7807 was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution.

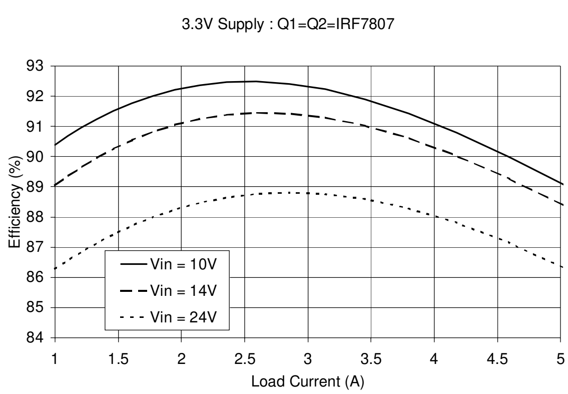


Figure 3

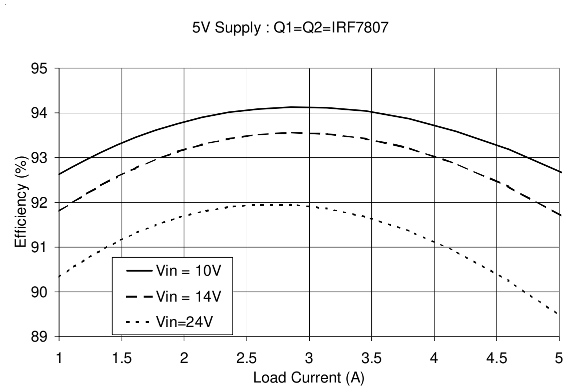


Figure 4

Typical Characteristics

IRF7807

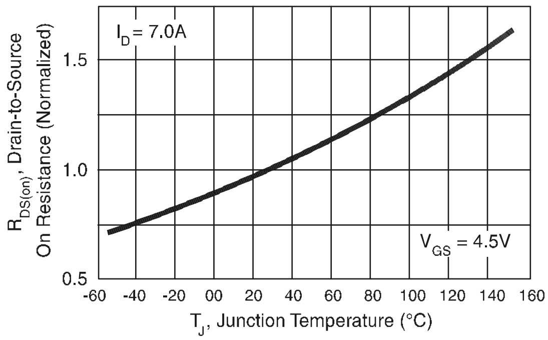


Figure 5. Normalized On-Resistance vs. Temperature

IRF7807A

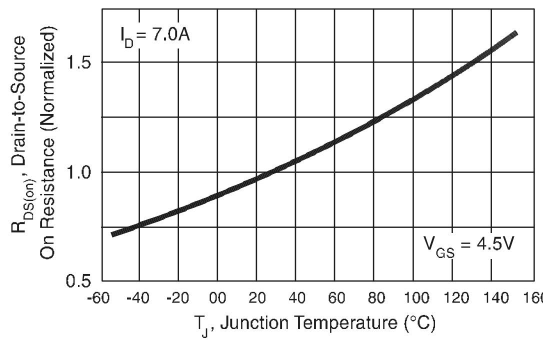


Figure 6. Normalized On-Resistance vs. Temperature

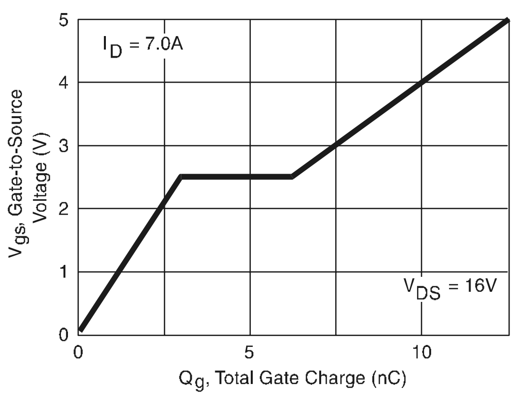


Figure 7. Typical Gate Charge vs. Gate-to-Source Voltage

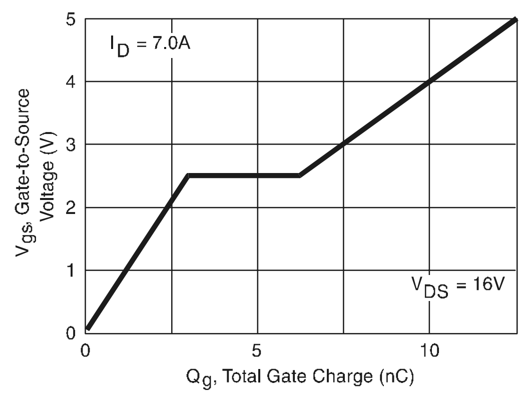


Figure 8. Typical Gate Charge vs. Gate-to-Source Voltage

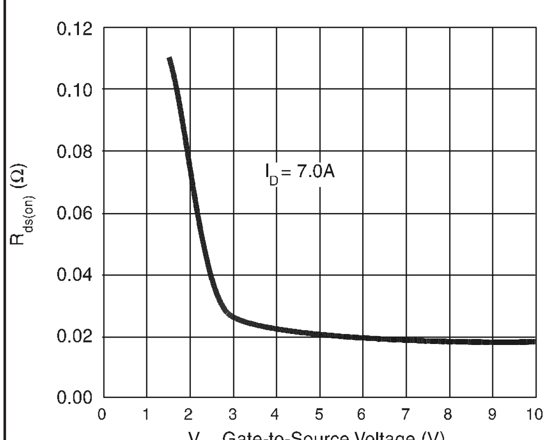


Figure 9. Typical Rds(on) vs. Gate-to-Source Voltage

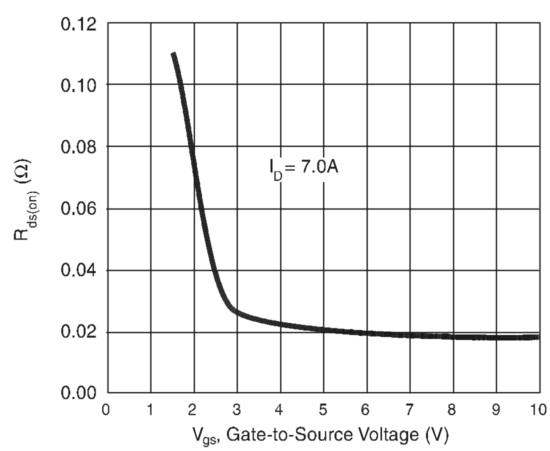


Figure 10. Typical Rds(on) vs. Gate-to-Source Voltage

IRF7807

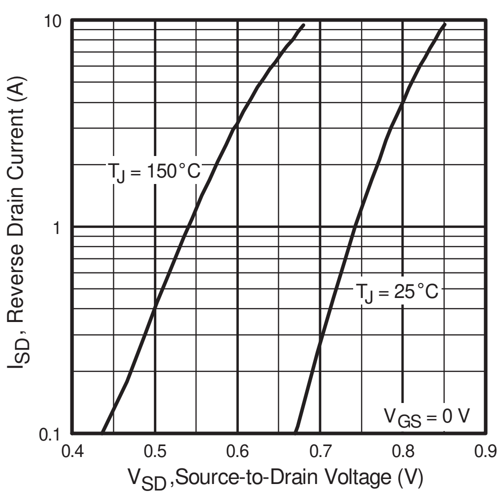


Figure 11. Typical Source-Drain Diode Forward Voltage

IRF7807A

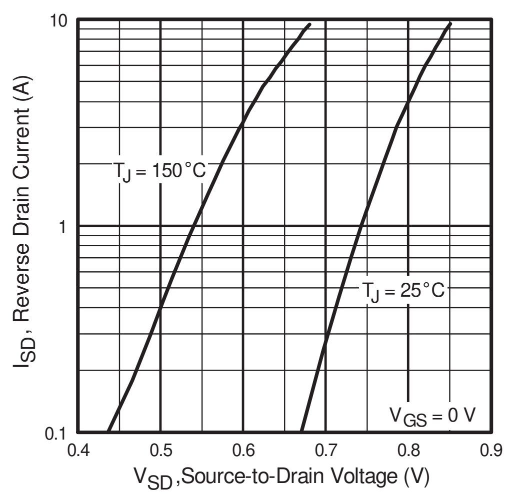


Figure 12. Typical Source-Drain Diode Forward Voltage

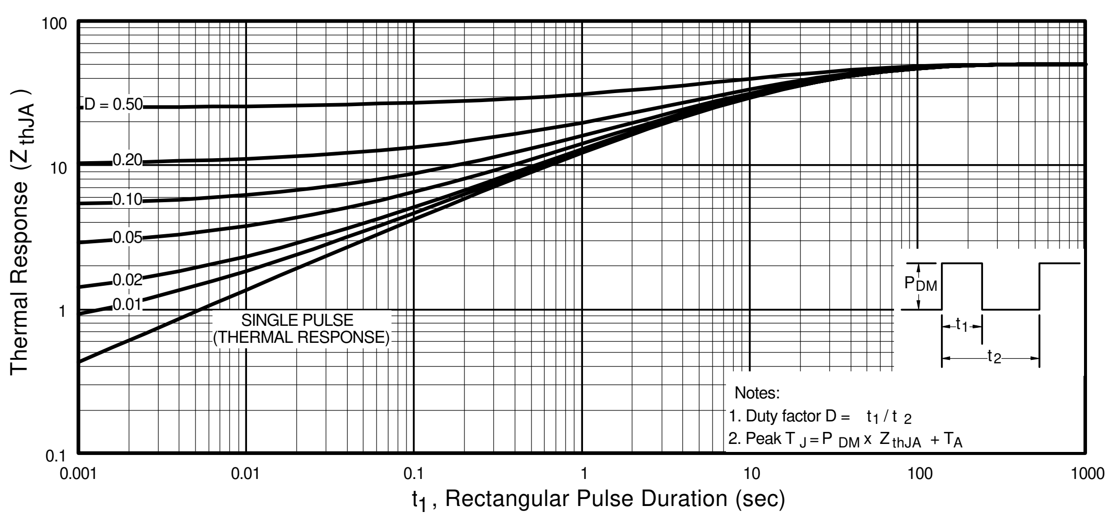
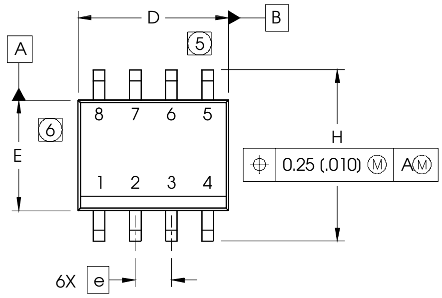


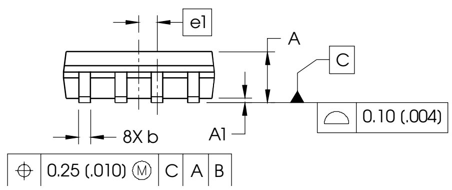
Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

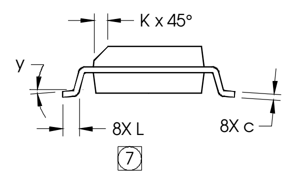
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°





NOTES:

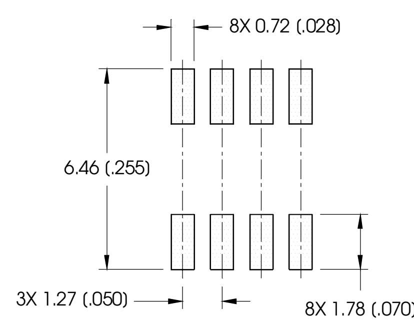
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

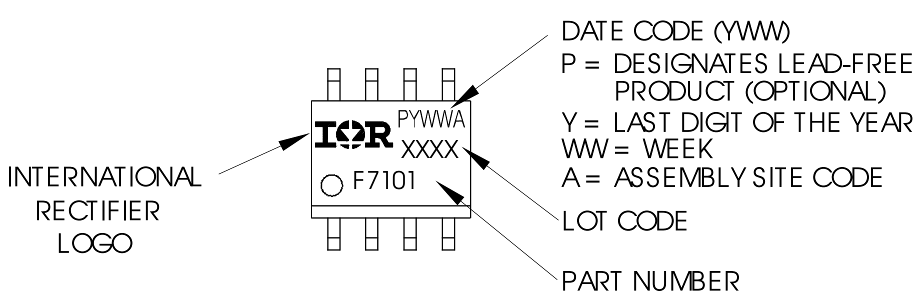
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



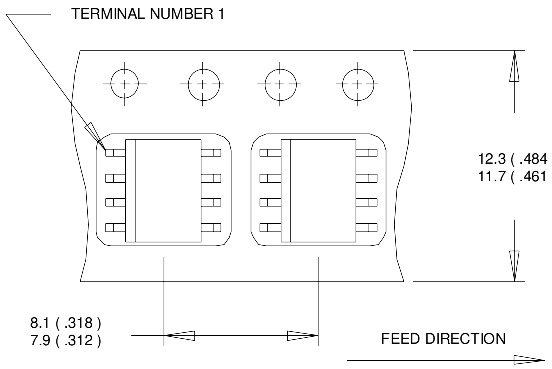
SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

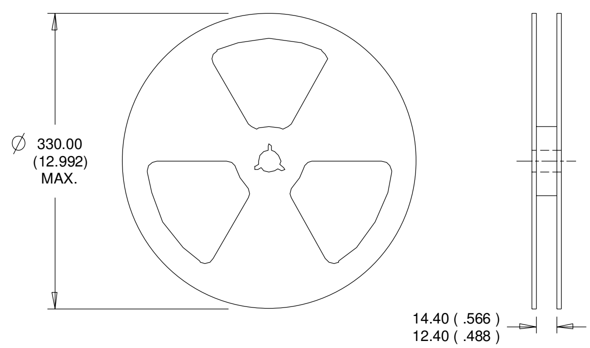


SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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