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# IRF8513PbF

HEXFET® Power MOSFET

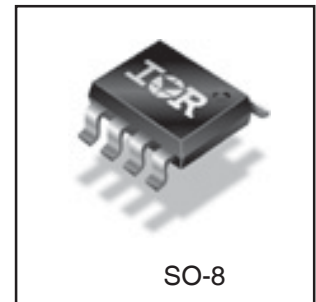
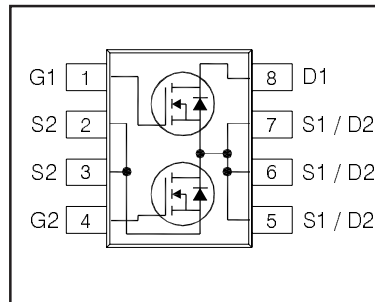
## Applications

- Dual SO-8 MOSFET for POL Converters in Notebook Computers, Servers, Graphics Cards, Game Consoles and Set-Top Box

$V_{DS}$	$R_{DS(on)}$ max	$I_D$
30V	Q1 15.5mΩ @ $V_{GS} = 10V$	8.0A
	Q2 12.7mΩ @ $V_{GS} = 10V$	11A

## Benefits

- Low Gate Charge and Low  $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current
- 20V  $V_{GS}$  Max. Gate Rating
- 100% Tested for  $R_G$
- Lead-Free (Qualified to 260°C Reflow)
- RoHS Compliant (Halogen Free)



## Description

The IRF8513PbF incorporates the latest HEXFET Power MOSFET Silicon Technology into the industry standard SO-8 package. The IRF8513PbF has been optimized for parameters that are critical in synchronous buck operation including  $R_{ds(on)}$  and gate charge to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors for notebook and Netcom applications.

## Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30		V
$V_{GS}$	Gate-to-Source Voltage	± 20		
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.0	11	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6.2	9.0	
$I_{DM}$	Pulsed Drain Current ①	64	88	
$P_D @ T_A = 25^\circ C$	Power Dissipation	1.5	2.4	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	1.05	1.68	
	Linear Derating Factor	0.01	0.02	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175		°C

## Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	42	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	100	62.5	

Notes ① through ⑤ are on page 11

## ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.


Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
B <sub>V</sub> DSS	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔB <sub>V</sub> DSS/ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	Q1	—	0.021	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
		Q2	—	0.021	—		
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	Q1	—	12.5	15.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8.0A ③
			—	18.1	22.2		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.4A ③
		Q2	—	10.2	12.7		V <sub>GS</sub> = 10V, I <sub>D</sub> = 11A ③
			—	14.2	16.9		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 8.6A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1&Q2	1.35	1.8	2.35	V	Q1: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA Q2: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	Q1	—	-6.5	—	mV/°C	
		Q2	—	-6.9	—		
I <sub>DSS</sub>	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		Q1&Q2	—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	Q1	19	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 6.4A
		Q2	24	—	—		V <sub>DS</sub> = 15V, I <sub>D</sub> = 8.6A
Q <sub>g</sub>	Total Gate Charge	Q1	—	5.7	8.6	nC	Q1 V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.4A  Q2 V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 8.6A  See Fig. 31a & 31b
		Q2	—	7.6	11.4		
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	Q1	—	1.2	—		
		Q2	—	1.7	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	Q1	—	0.68	—		
		Q2	—	1.0	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	Q1	—	2.2	—		
		Q2	—	3.1	—		
Q <sub>aodr</sub>	Gate Charge Overdrive	Q1	—	1.6	—		
		Q2	—	1.9	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	Q1	—	2.9	—	nC	See Fig. 31a & 31b
		Q2	—	4.0	—		
Q <sub>oss</sub>	Output Charge	Q1	—	3.9	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
		Q2	—	5.2	—		
R <sub>G</sub>	Gate Resistance	Q1	—	2.1	3.2	Ω	
		Q2	—	1.4	3.1		
t <sub>d(on)</sub>	Turn-On Delay Time	Q1	—	8.0	—	ns	Q1 V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 6.4A R <sub>G</sub> = 1.8Ω See Fig.30a & 30b Q2 V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 8.6A R <sub>G</sub> = 1.8W
		Q2	—	8.9	—		
t <sub>r</sub>	Rise Time	Q1	—	8.5	—		
		Q2	—	10.7	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	Q1	—	8.8	—		
		Q2	—	9.3	—		
t <sub>f</sub>	Fall Time	Q1	—	5.7	—		
		Q2	—	5.0	—		
C <sub>iss</sub>	Input Capacitance	Q1	—	766	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
		Q2	—	1024	—		
C <sub>oss</sub>	Output Capacitance	Q1	—	172	—		
		Q2	—	238	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	—	83	—		
		Q2	—	116	—		

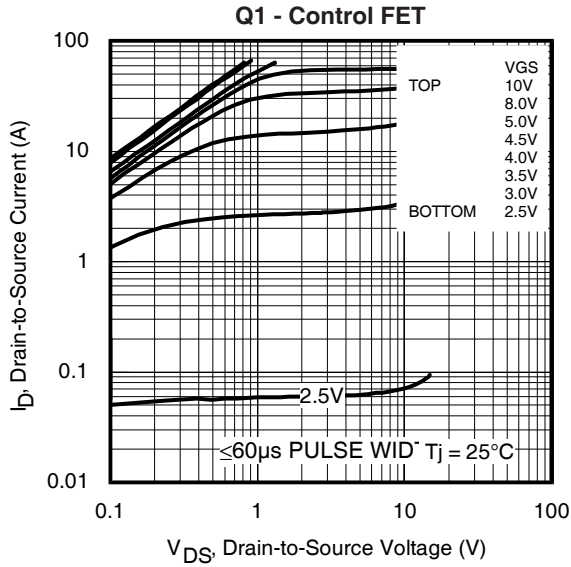
### Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	49	70	mJ
I <sub>AR</sub>	Avalanche Current ①	—	6.4	8.6	A

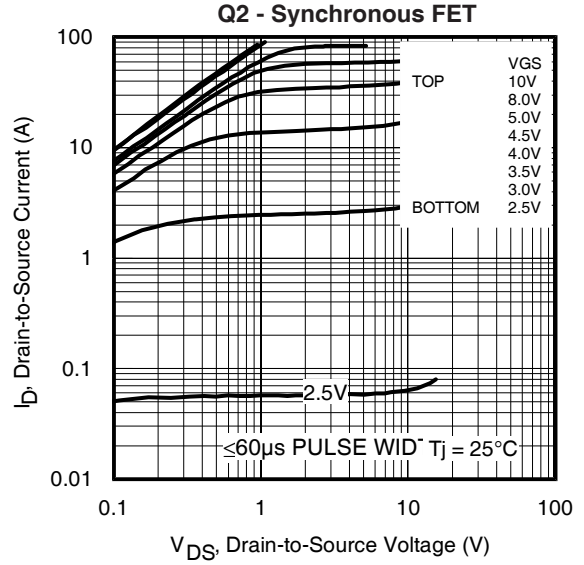
### Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions	
I <sub>S</sub>	Continuous Source Current (Body Diode)	Q1	—	—	1.9	A	MOSFET symbol showing the integral reverse p-n junction diode. 	
		Q2	—	—	3.0			
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	Q1	—	—	64	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.4A, V <sub>GS</sub> = 0V ③	
		Q2	—	—	88			
V <sub>SD</sub>	Diode Forward Voltage	Q1	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 8.6A, V <sub>GS</sub> = 0V ③	
		Q2	—	—	1.0			
t <sub>rr</sub>	Reverse Recovery Time	Q1	—	15	23	ns	Q1 T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.4A, V <sub>DD</sub> = 15V, di/dt = 100A/μs ③	
		Q2	—	17	26			
Q <sub>rr</sub>	Reverse Recovery Charge	Q1	—	7.2	11	nC	Q2 T <sub>J</sub> = 25°C, I <sub>F</sub> = 8.6A, V <sub>DD</sub> = 15V, di/dt = 100A/μs ③	
		Q2	—	9.3	14			
t <sub>on</sub>	Forward Trun-On Time	Intrinsic turn -on time is negligible (turn -on is dominated by LS+LD)						

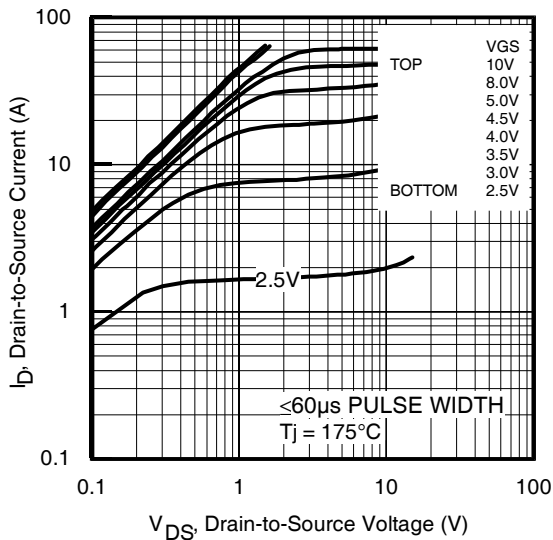
## Typical Characteristics



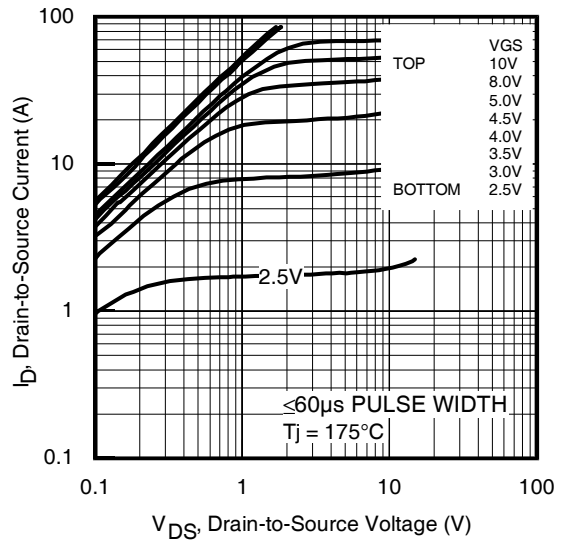
**Fig 1.** Typical Output Characteristics



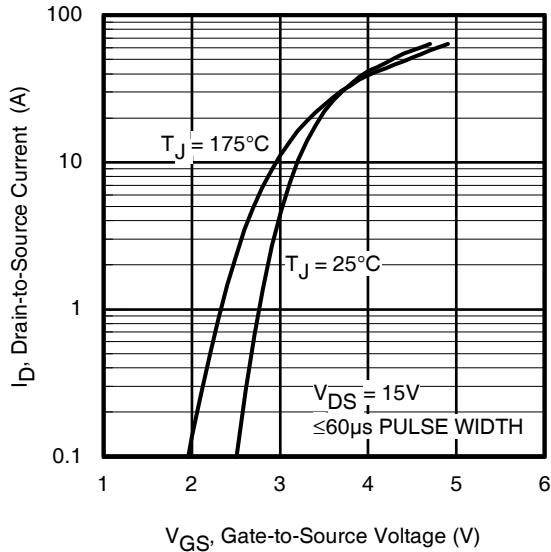
**Fig 2.** Typical Output Characteristics



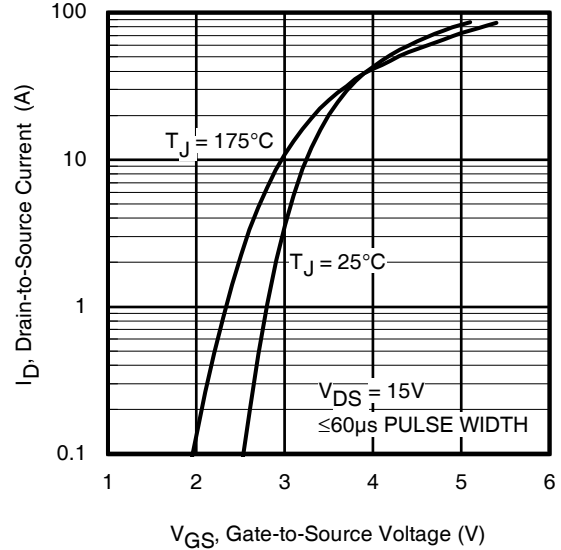
**Fig 3.** Typical Output Characteristics



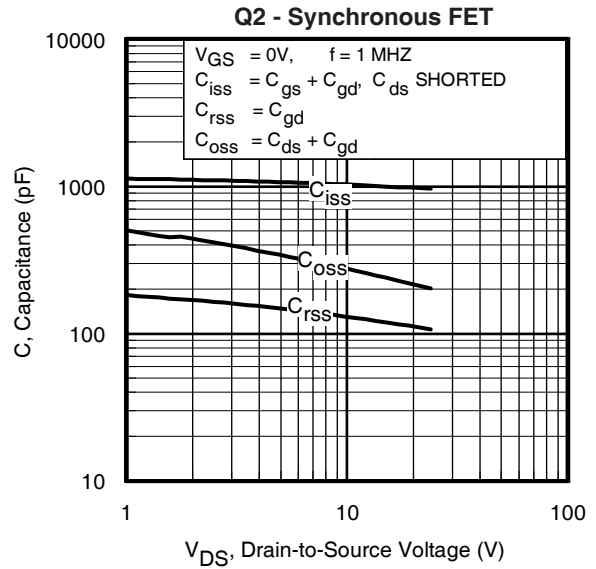
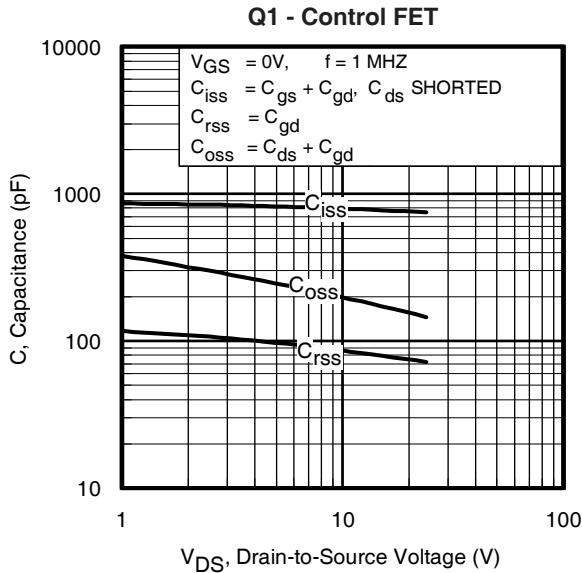
**Fig 4.** Typical Output Characteristics



**Fig 5.** Typical Transfer Characteristics

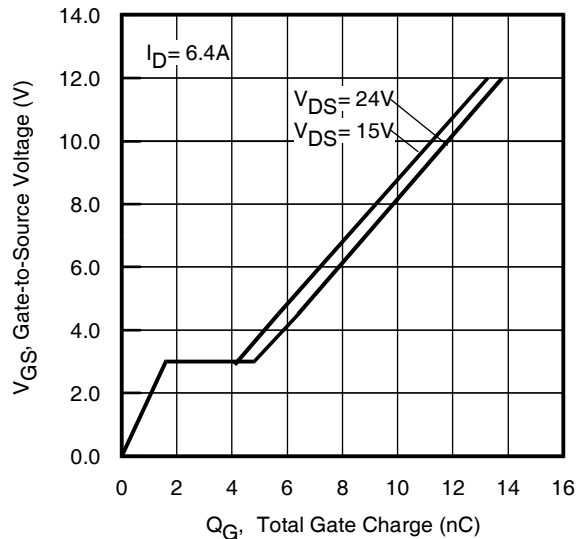


**Fig 6.** Typical Transfer Characteristics

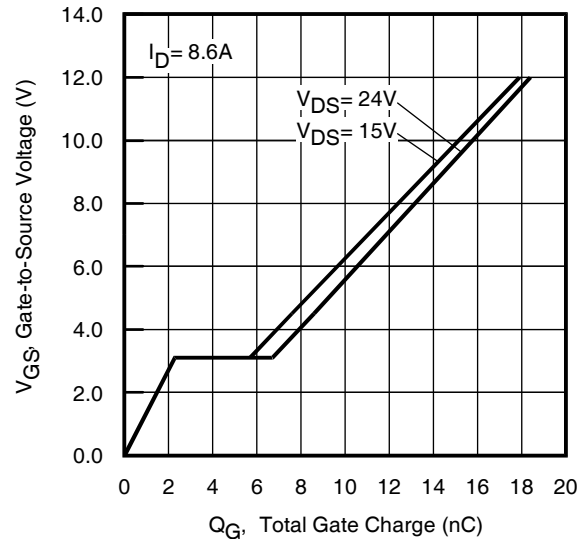


**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

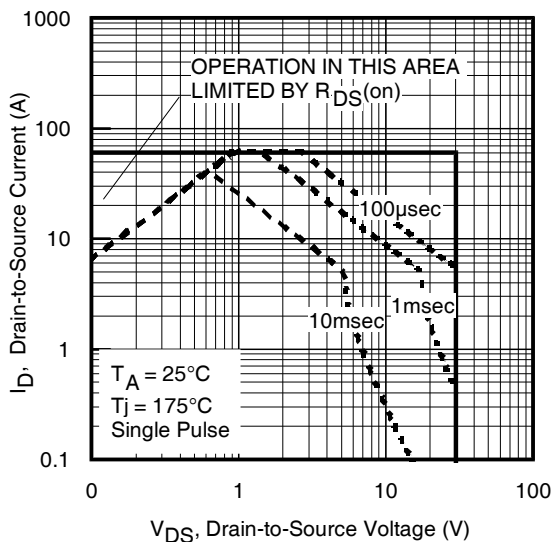
**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage



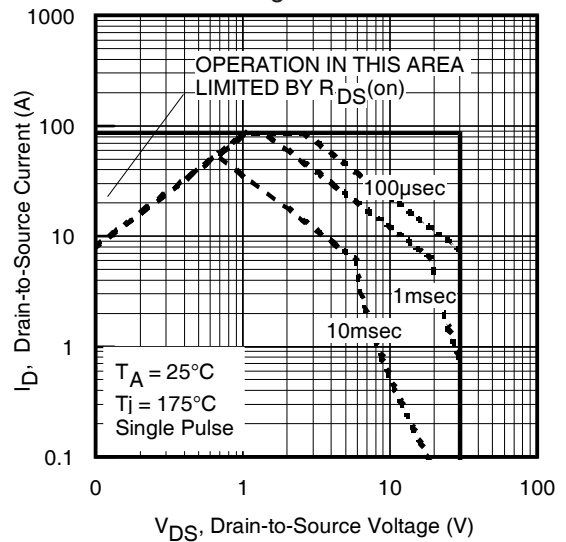
**Fig 9.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 11.** Maximum Safe Operating Area



**Fig 12.** Maximum Safe Operating Area

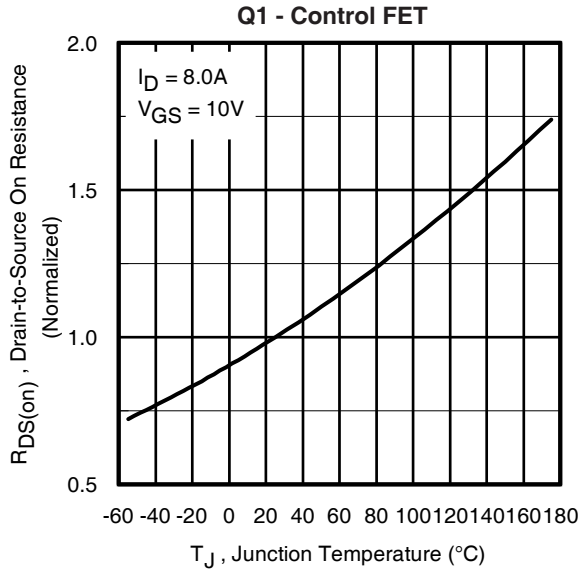


Fig 13. Normalized On-Resistance vs. Temperature

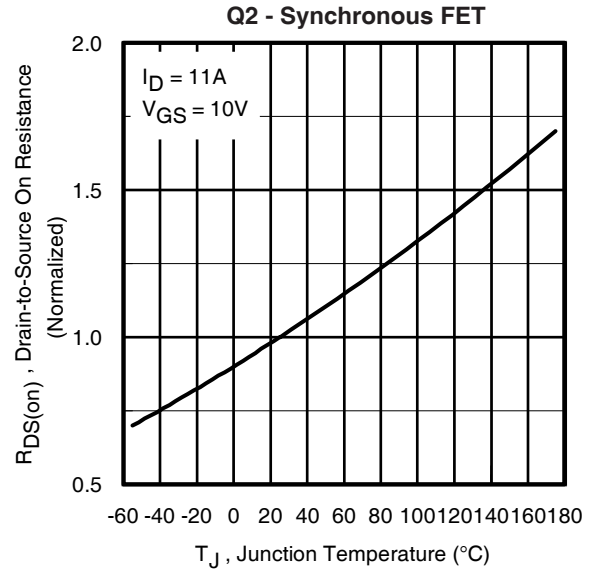


Fig 14. Normalized On-Resistance vs. Temperature

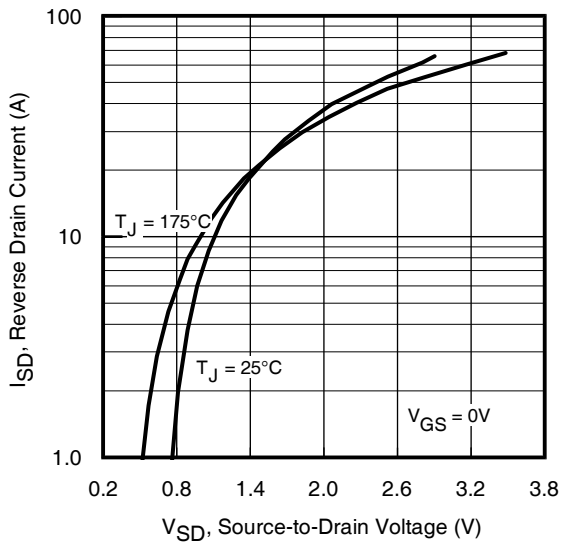


Fig 15. Typical Source-Drain Diode Forward Voltage

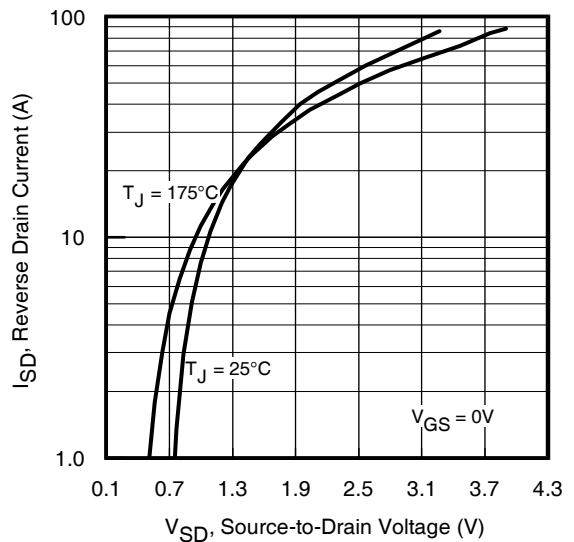


Fig 16. Typical Source-Drain Diode Forward Voltage

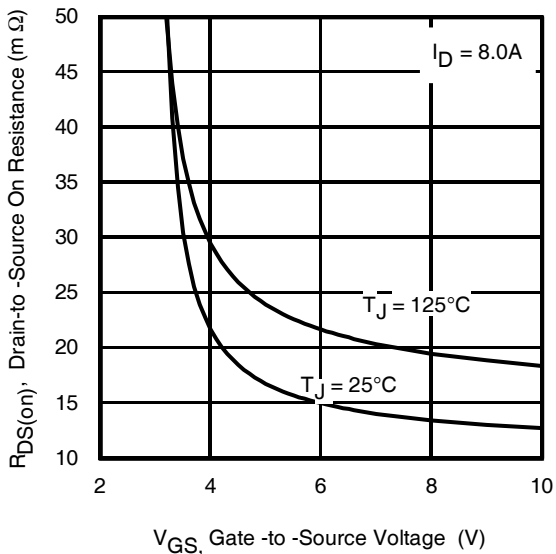


Fig 17. Typical On-Resistance vs. Gate Voltage

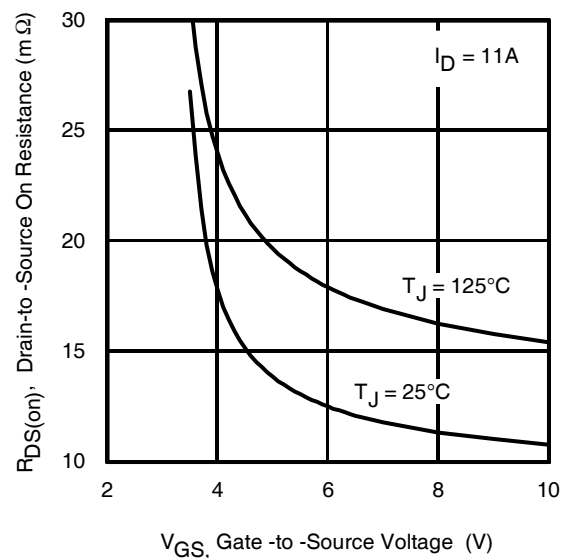
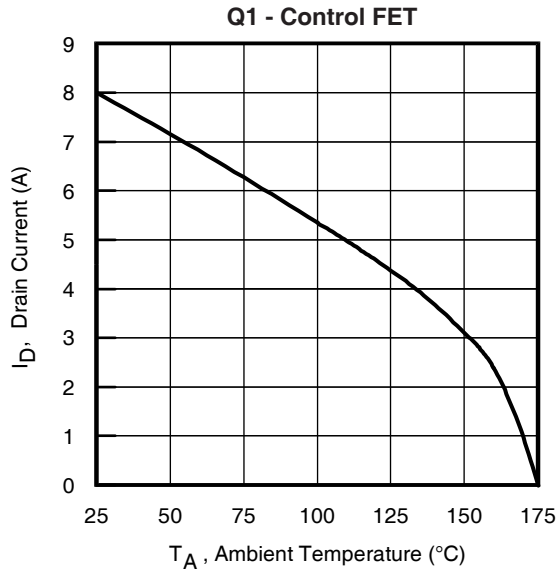
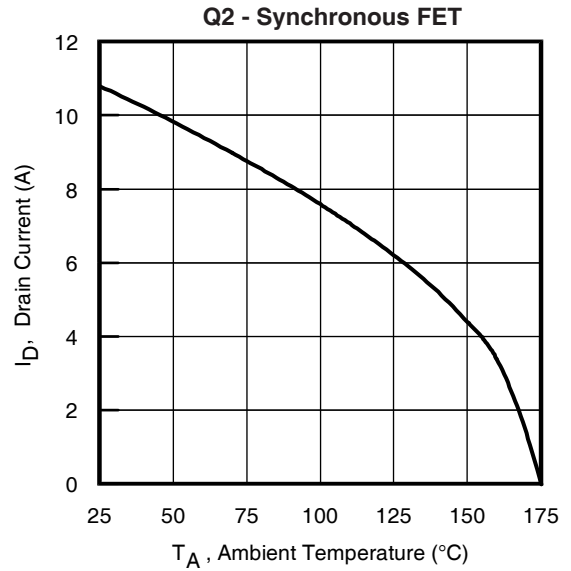


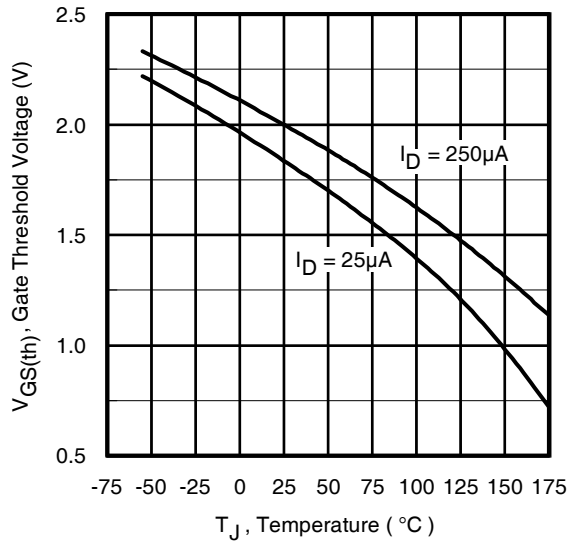
Fig 18. Typical On-Resistance vs. Gate Voltage



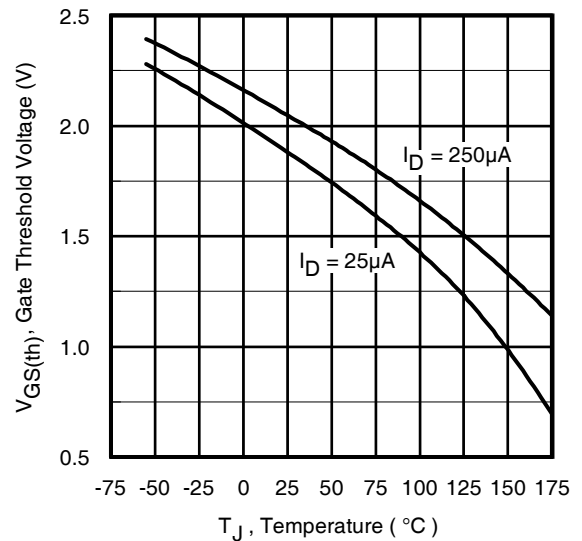
**Fig 19.** Maximum Drain Current vs. Ambient Temp.



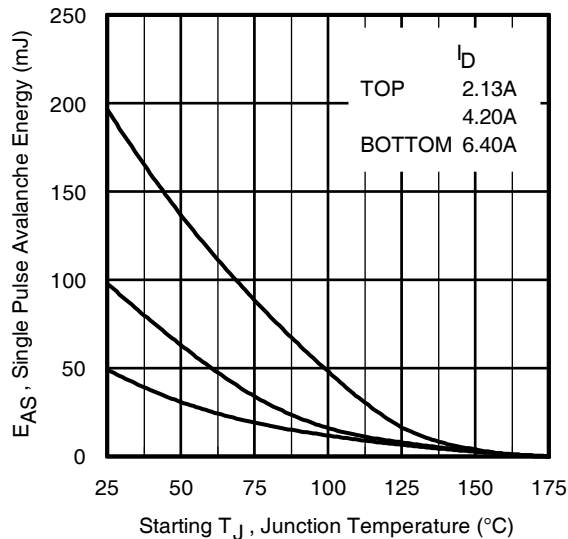
**Fig 20.** Maximum Drain Current vs. Ambient Temp.



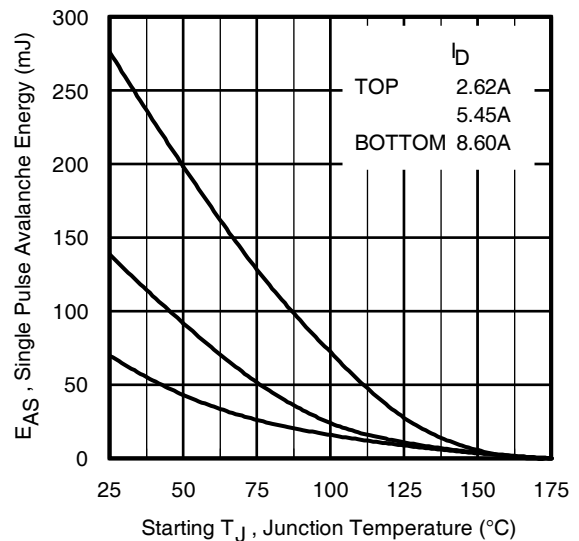
**Fig 21.** Threshold Voltage vs. Temperature



**Fig 22.** Threshold Voltage vs. Temperature



**Fig 23.** Maximum Avalanche Energy vs. Drain Current



**Fig 24.** Maximum Avalanche Energy vs. Drain Current

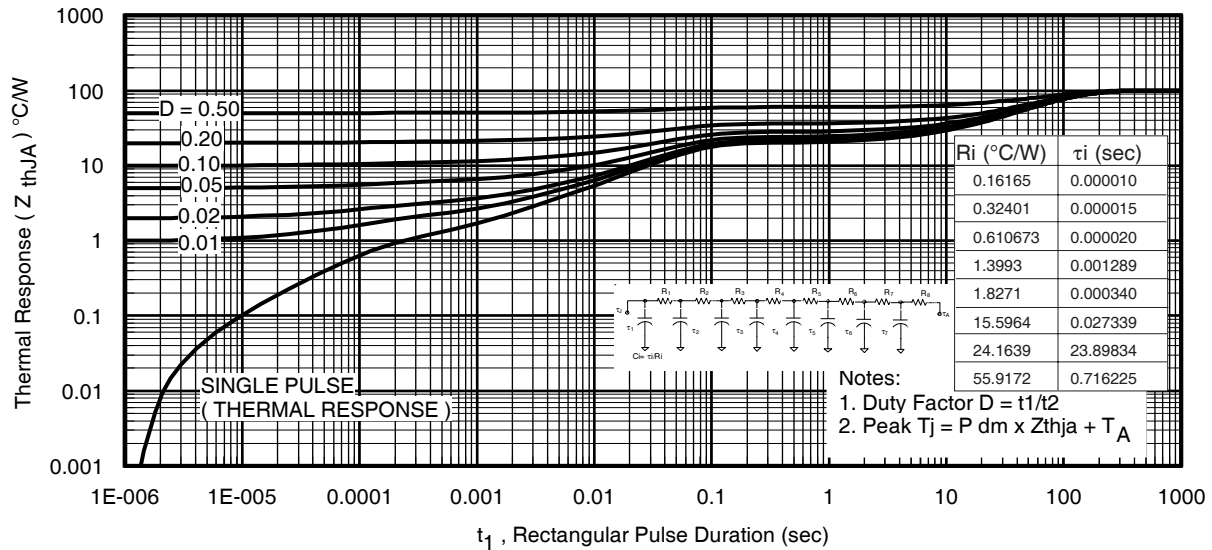


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

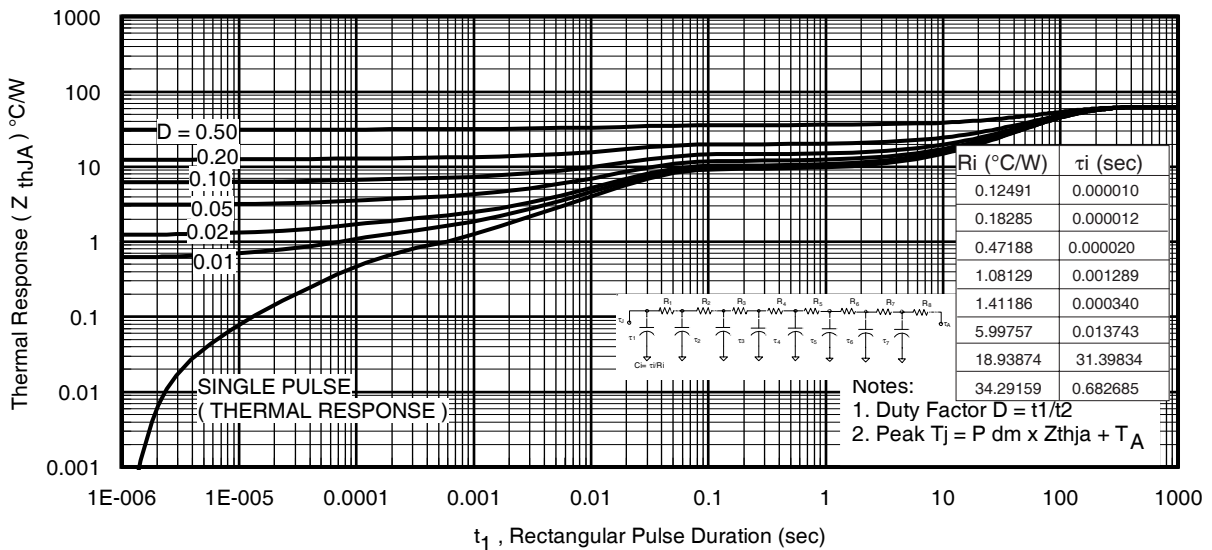


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

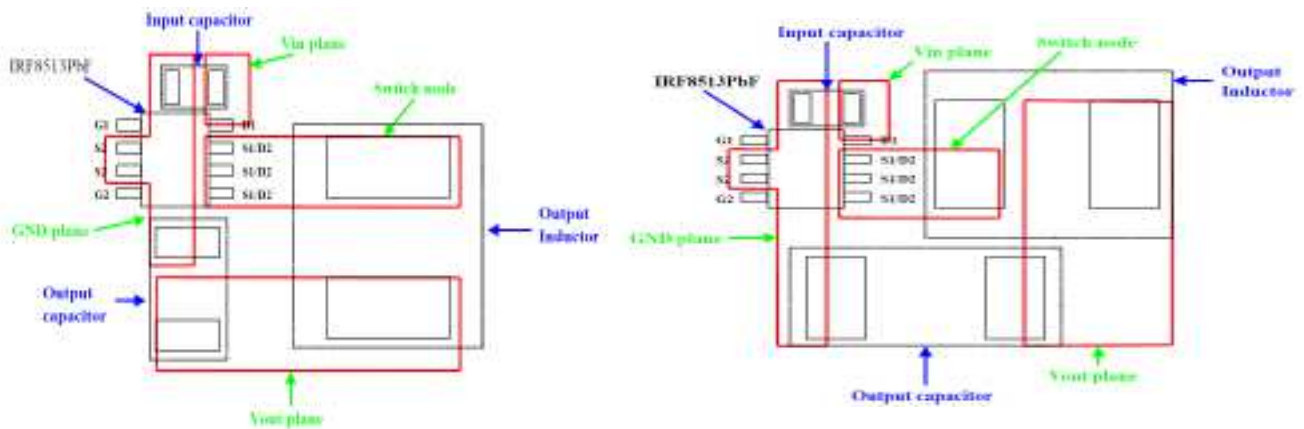
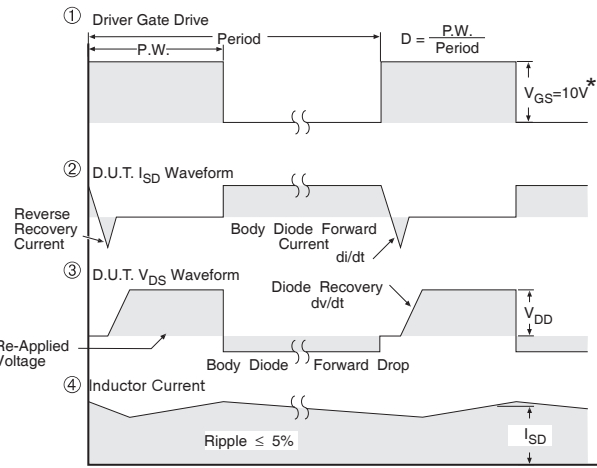
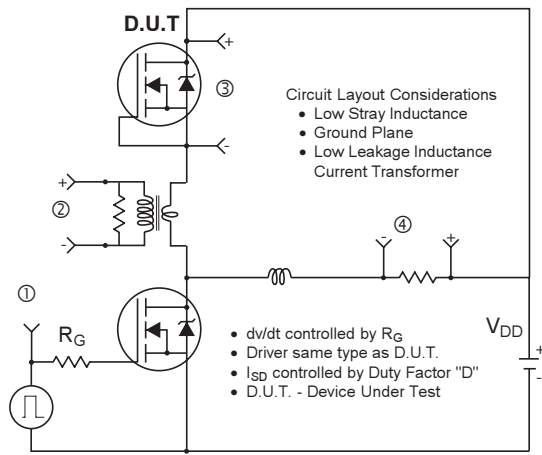


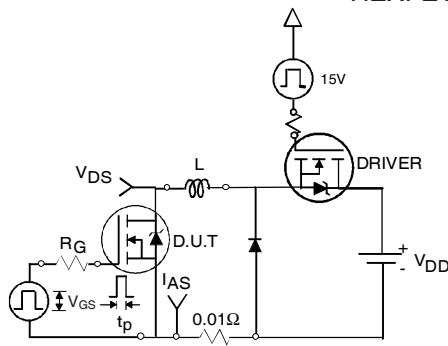
Fig 27. Layout Diagram



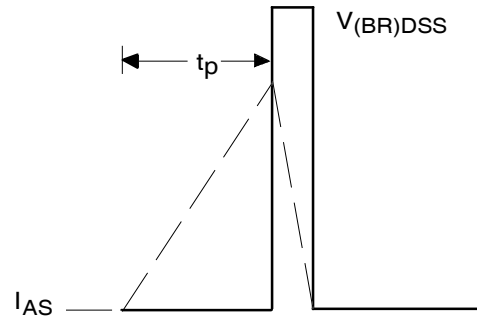


\*  $V_{GS} = 5V$  for Logic Level Devices

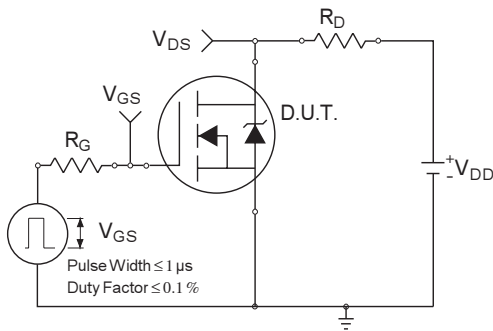
**Fig 28. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



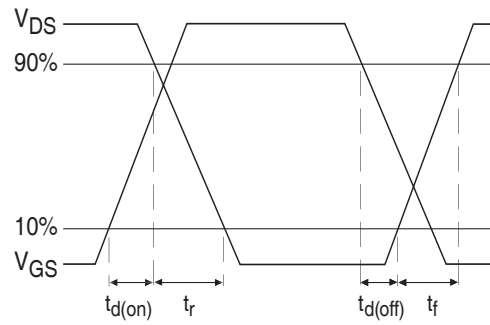
**Fig 29a. Unclamped Inductive Test Circuit**



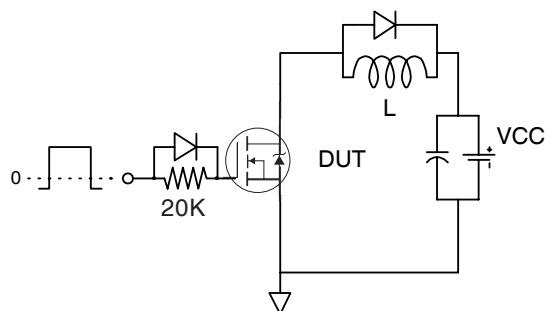
**Fig 29b. Unclamped Inductive Waveforms**



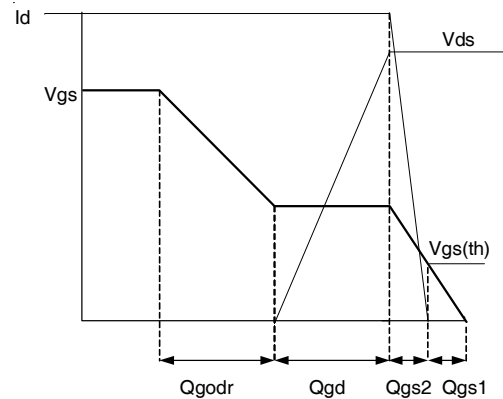
**Fig 30a. Switching Time Test Circuit**



**Fig 30b. Switching Time Waveforms**



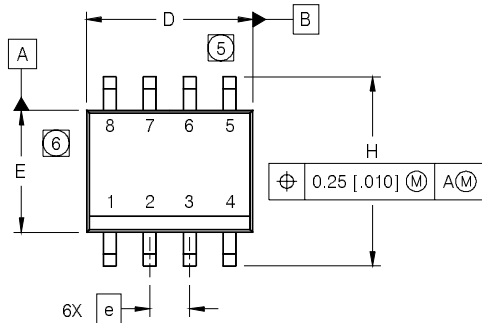
**Fig 31a. Gate Charge Test Circuit**



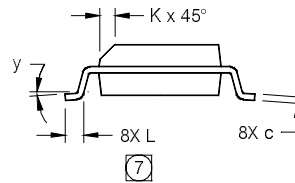
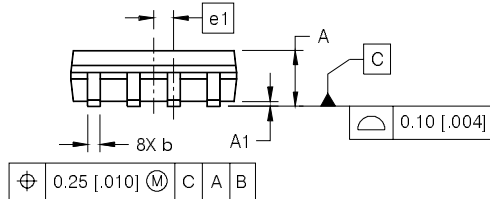
**Fig 31b. Gate Charge Waveform**

## SO-8 Package Outline (MOSFET & Fetky)

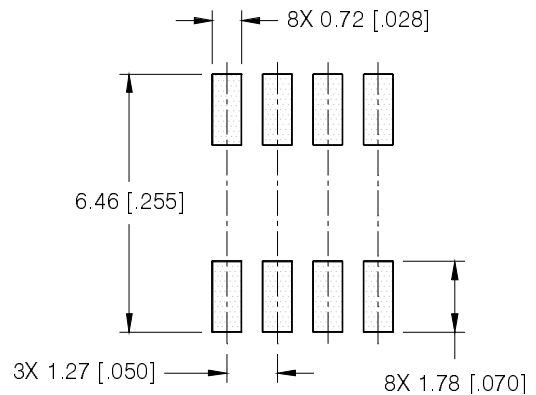
Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



### FOOTPRINT

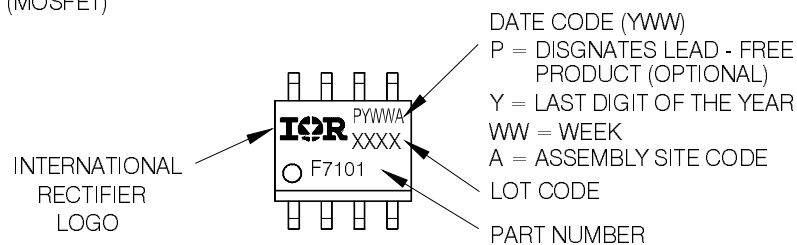


### NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

## SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

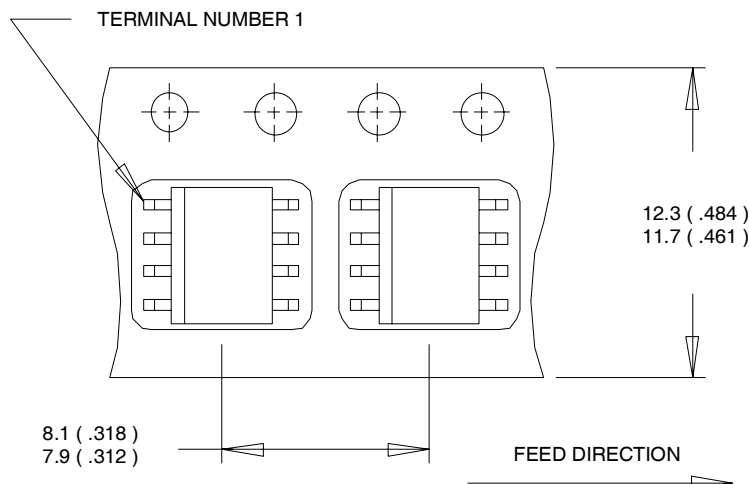


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRF8513PbF

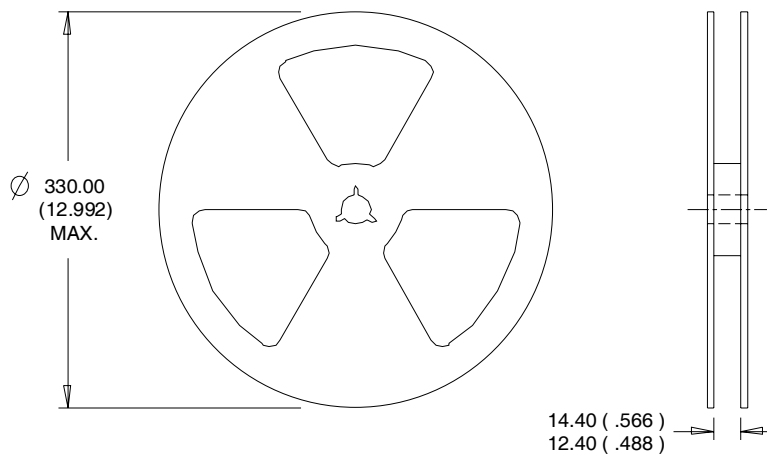
## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



### NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF8513PbF	SO-8	Tube/Bulk	95	
IRF8513TRPbF	SO-8	Tape and Reel	4000	

### Qualification Information<sup>†</sup>

Qualification level	Consumer <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines)		
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )	
RoHS Compliant	Yes		

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 2.4\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 6.4\text{A}$  (Q1) &  
 $L = 1.87\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 8.6\text{A}$  (Q2)
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ When mounted on 1 inch square copper board.
- ⑤  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.