Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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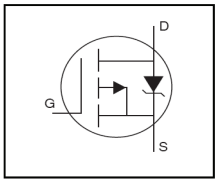
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

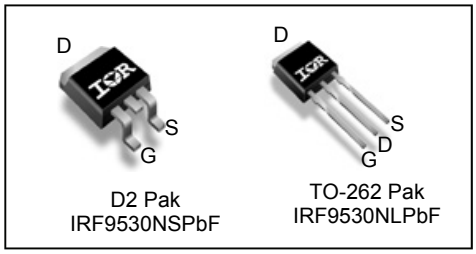
HEXFET® Power MOSFET

Benefits

- Advanced Process Technology
- Surface Mount (IRF9530NS)
- Low-profile through-hole(IRF9530NL)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead-Free



V_{DSS}	-100V
$R_{DS(on)}$	0.20Ω
I_D	-14A



G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF9530NL) is available for low-profile applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
~~IRF9530NLPbF~~	~~TO-262~~	~~Tube~~	~~50~~	~~IRF9530NLPbF~~ **(Obsolete)**
IRF9530NSPbF	D2-Pak	Tape and Reel Left	800	IRF9530NSTRLPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V ⑤	-14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V ⑤	-10	
I_{DM}	Pulsed Drain Current ①⑤	-56	
P_D @T_A = 25°C	Maximum Power Dissipation	3.8	W
P_D @T_C = 25°C	Maximum Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②⑤	250	mJ
I_{AR}	Avalanche Current ①	-8.4	A
E_{AR}	Repetitive Avalanche Energy ①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt③⑤	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑥	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I_D = -1mA ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	V_{GS} = -10V, I_D = -8.4A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
gfs	Forward Trans conductance	3.2	—	—	S	V_{DS} = -50V, I_D = -8.4A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	µA	V_{DS} = -100V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	58	nC	I_D = -8.4A
Q_{gs}	Gate-to-Source Charge	—	—	8.3		V_{DS} = -80V
Q_{gd}	Gate-to-Drain Charge	—	—	32		V_{GS} = -10V See Fig.6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = -50V
t_r	Rise Time	—	58	—		I_D = -8.4A
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		R_G= 9.1Ω
t_f	Fall Time	—	46	—		R_D= 6.2Ω See Fig.6 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	760	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	260	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	170	—		f = 1.0MHz, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-56		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	T_J = 25°C,I_S = -8.4A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	130	190	ns	T_J = 25°C ,I_F = -8.4A
Q_{rr}	Reverse Recovery Charge	—	650	970	nC	di/dt = -100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② starting T_J = 25°C, L = 7.0mH, R_G = 25Ω, I_{AS} = -8.4A. (See fig. 12)

③ I_{SD} ≤ -8.4A, di/dt ≤ -490A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF9530N data and test conditions.

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

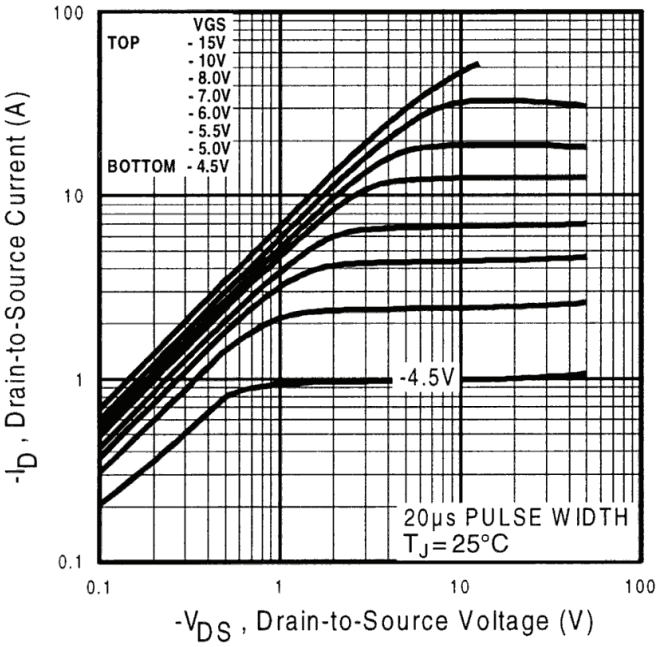


Fig. 1 Typical Output Characteristics

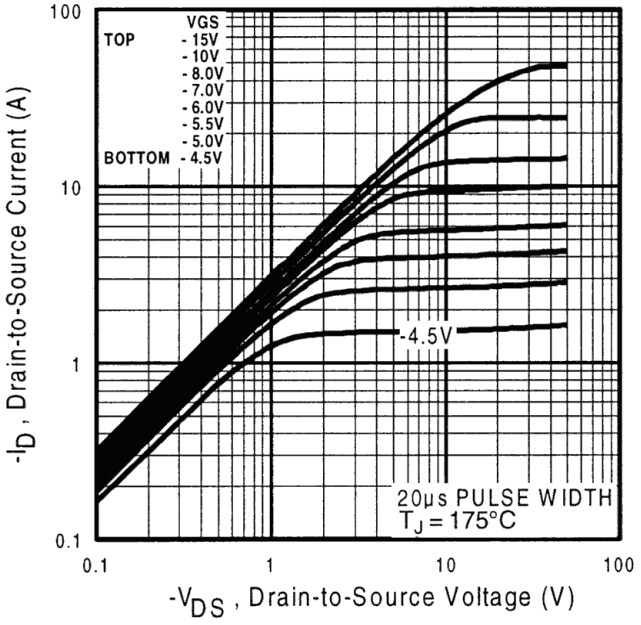


Fig. 2 Typical Output Characteristics

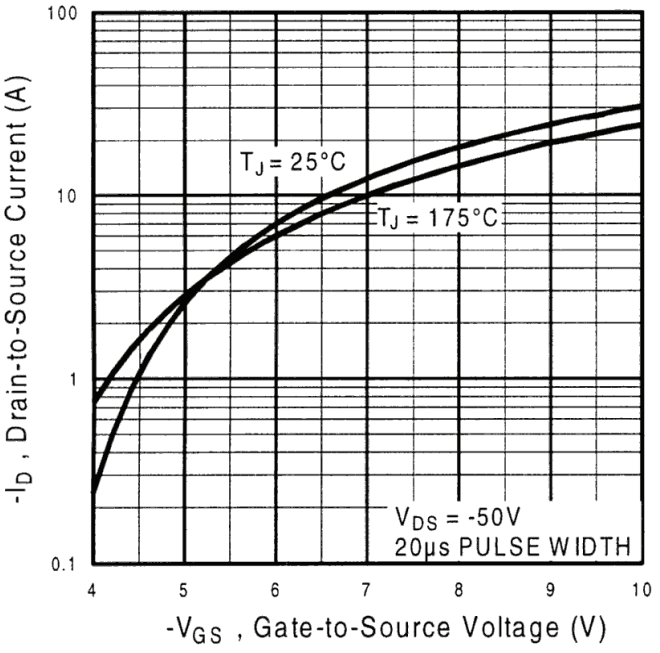


Fig. 3 Typical Transfer Characteristics

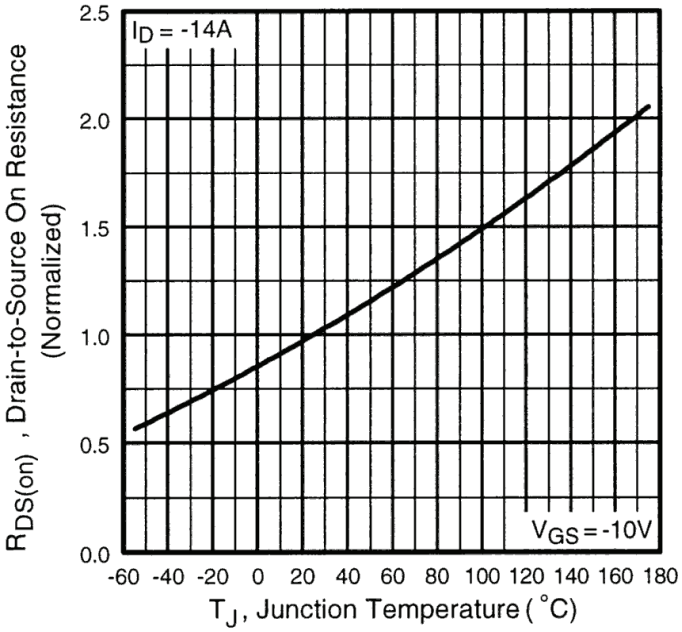


Fig. 4 Normalized On-Resistance vs. Temperature

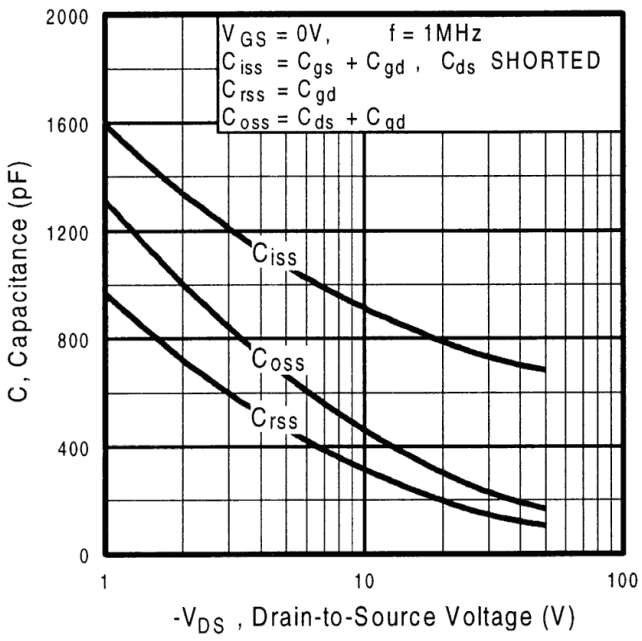


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

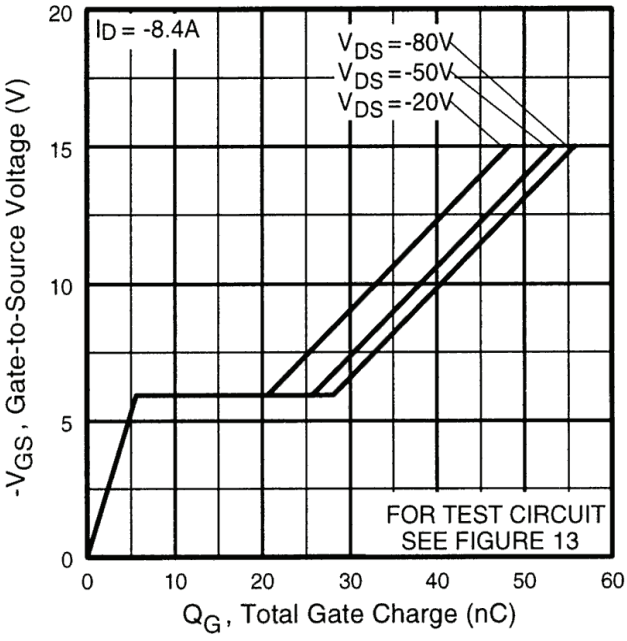


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

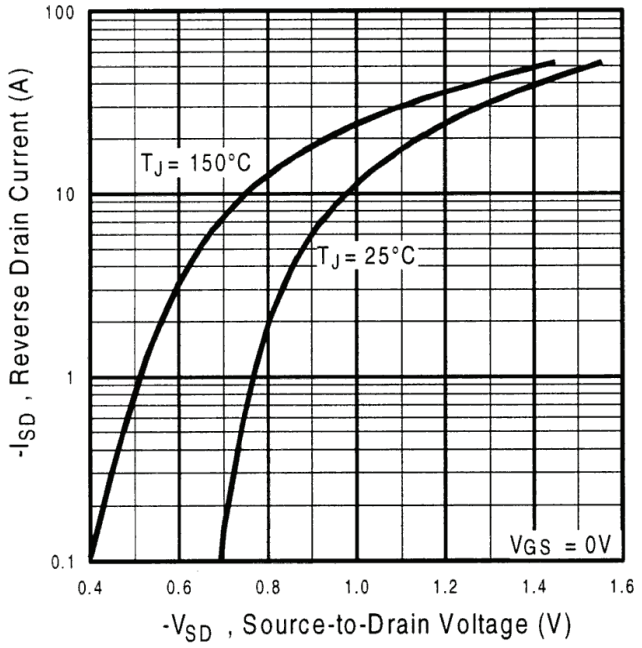


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

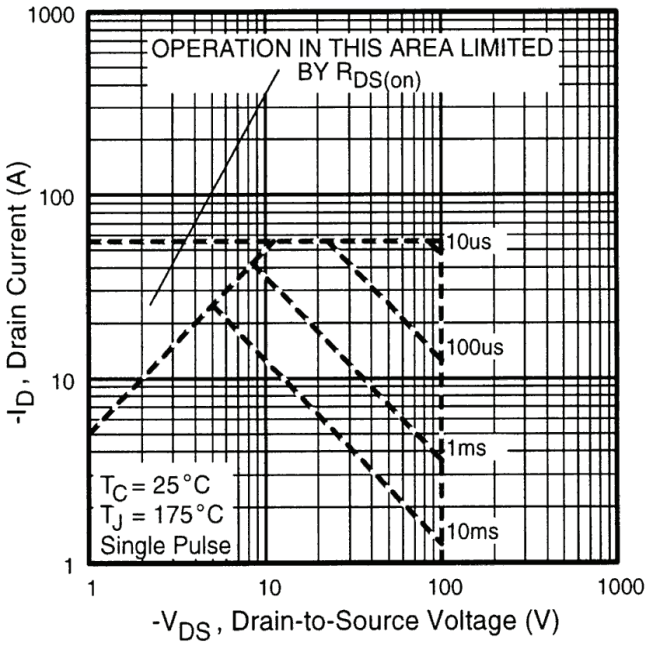


Fig 8. Maximum Safe Operating Area

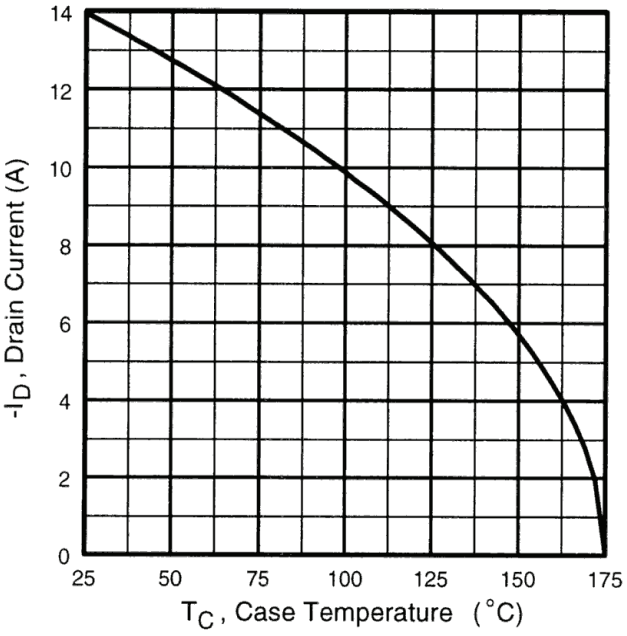


Fig 9. Maximum Drain Current vs. Case Temperature

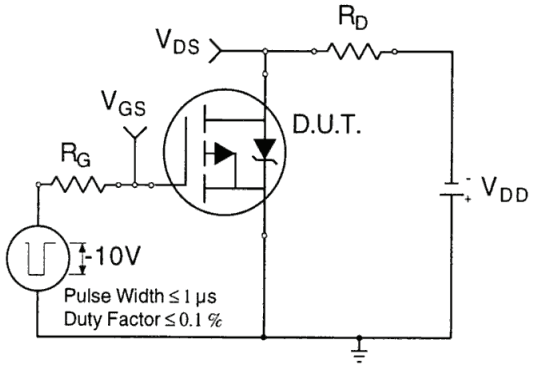


Fig 10a. Switching Time Test Circuit

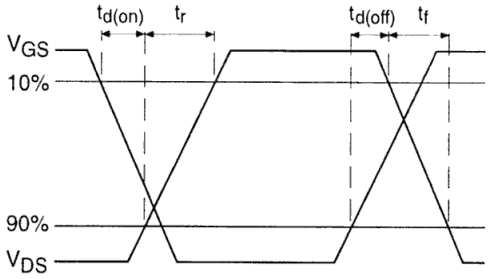


Fig 10b. Switching Time Waveforms

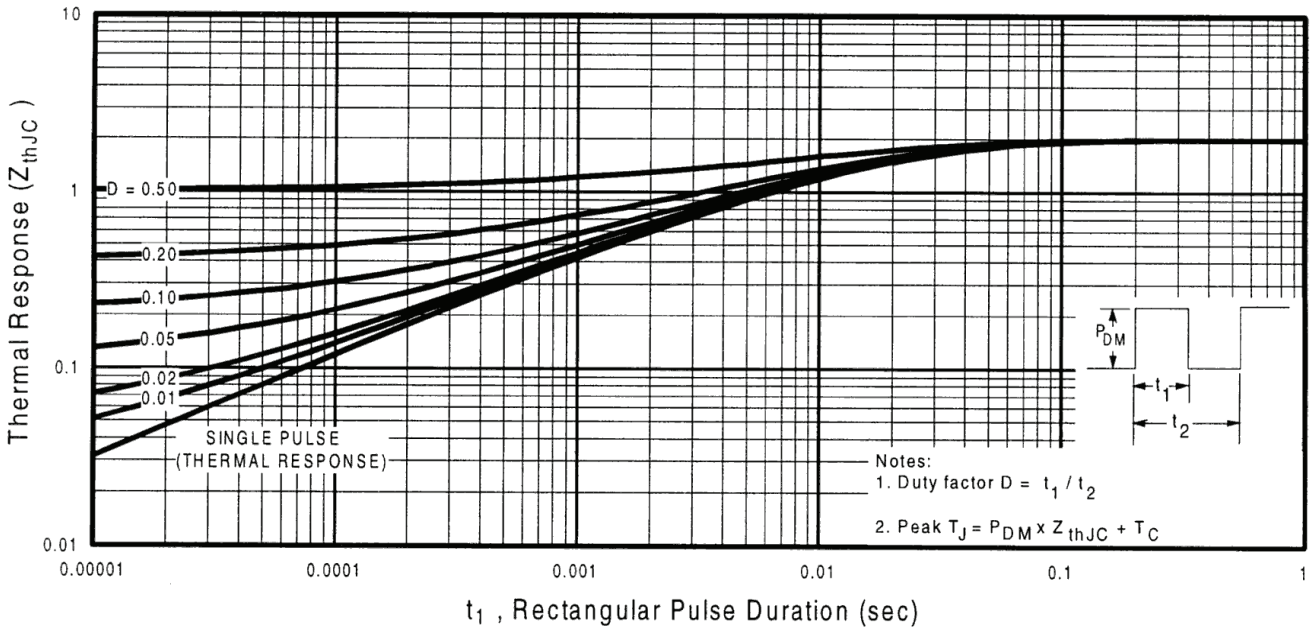


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

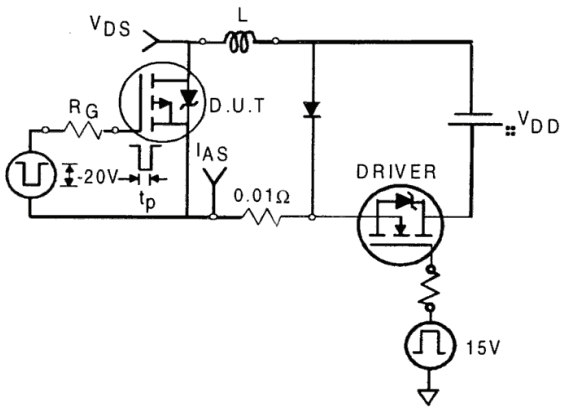


Fig 12a. Unclamped Inductive Test Circuit

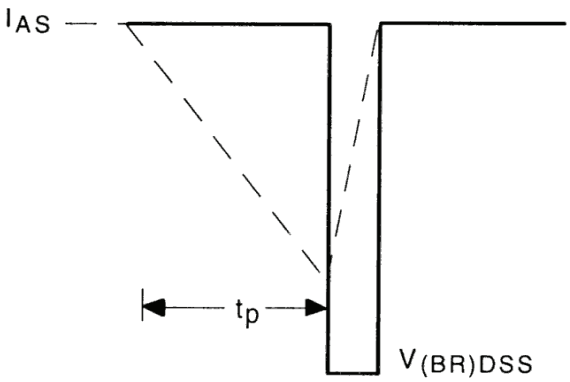


Fig 12b. Unclamped Inductive Waveforms

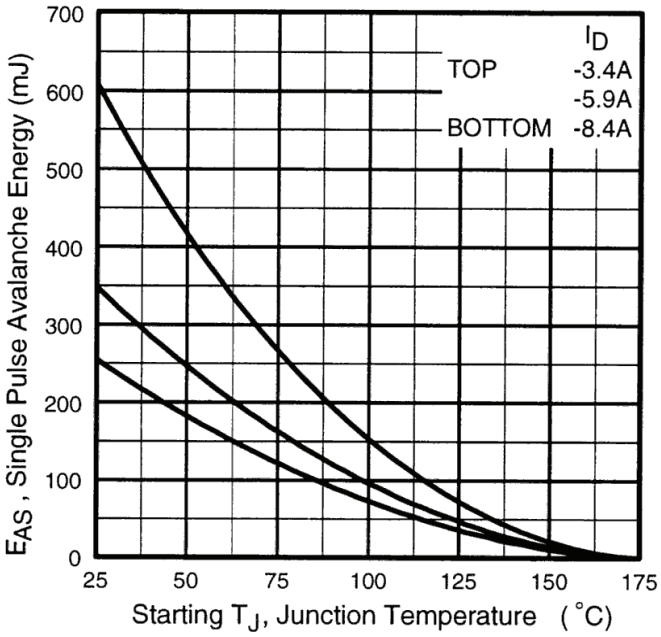


Fig 12c. Maximum Avalanche Energy vs. Drain Current

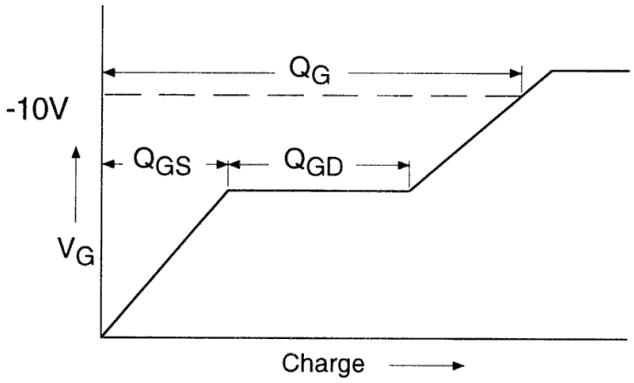


Fig 13a. Gate Charge Waveform

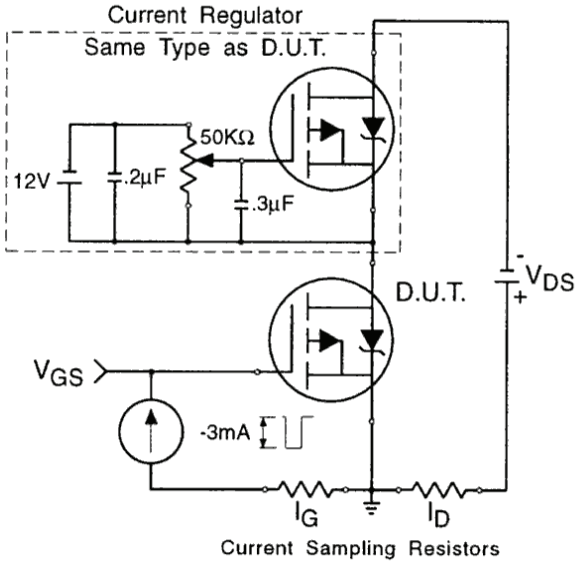


Fig 13b. Gate Charge Test Circuit

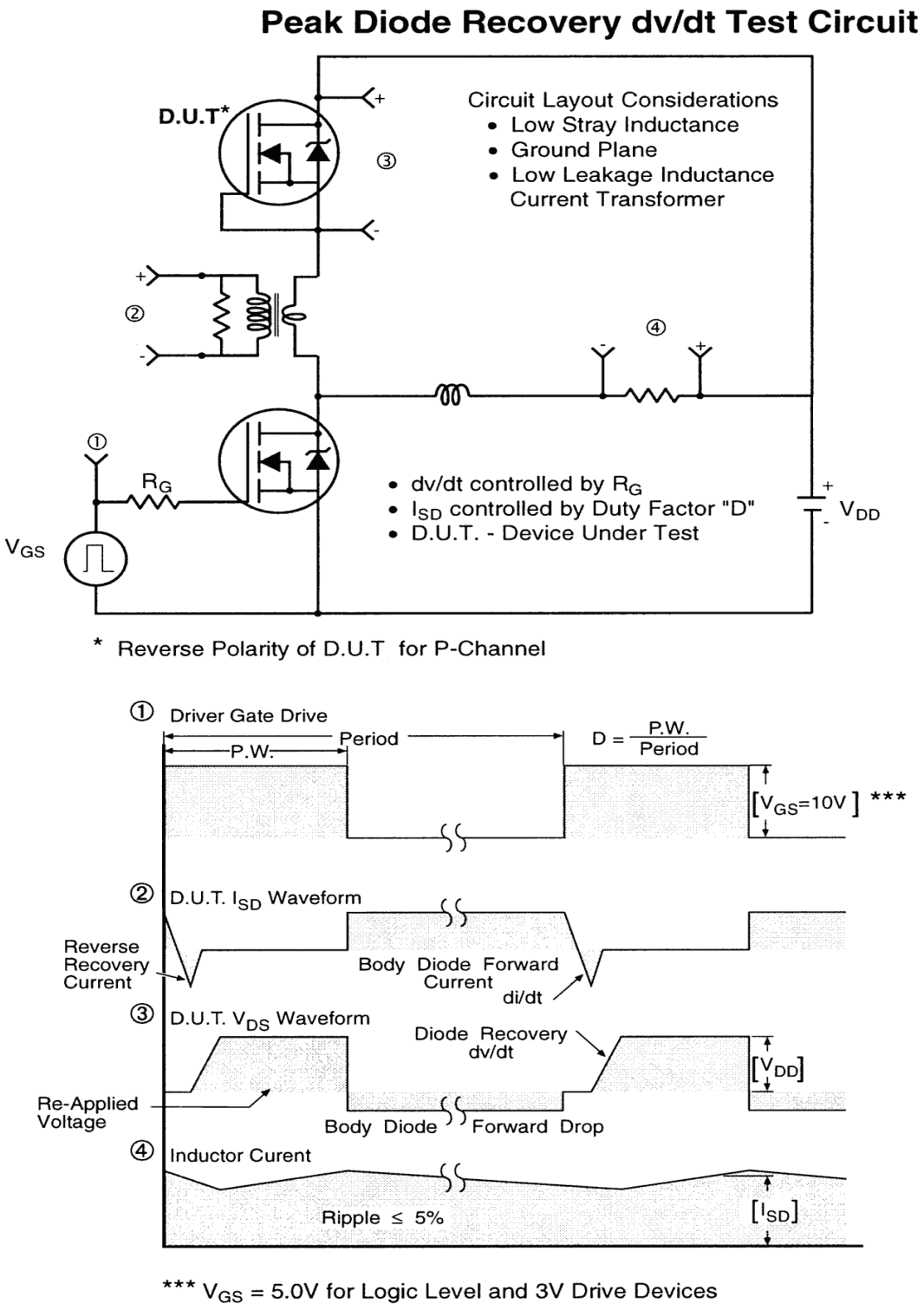
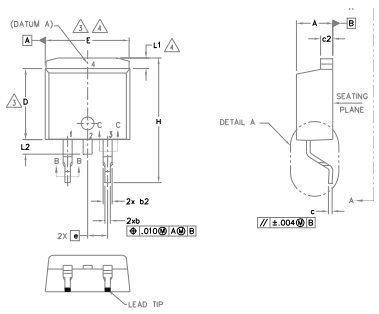


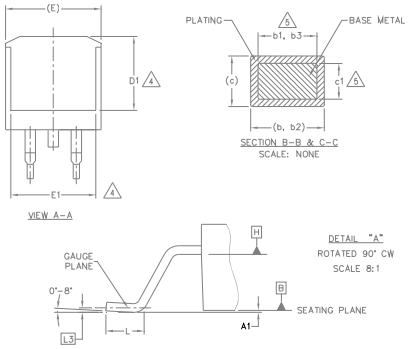
Fig 14. Peak Diode Recovery dv/dt Test Circuit for PChannel HEXFET® Power MOSFETs

D2-Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

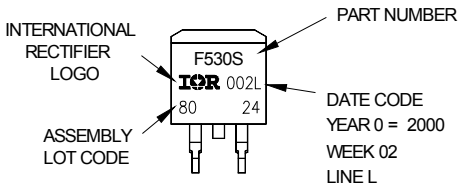
IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

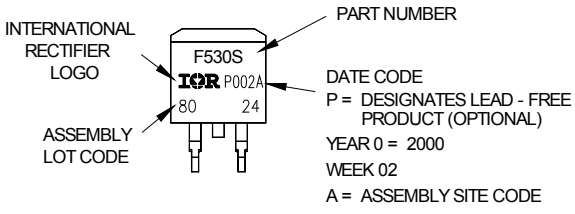
D2-Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead – Free"

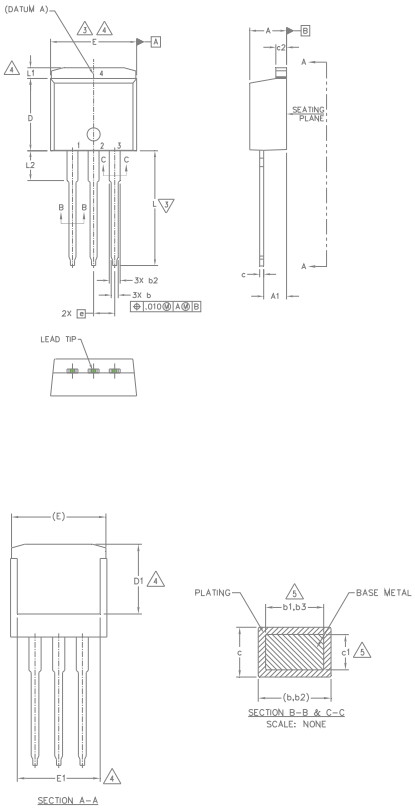


OR



Note: For the most current drawing please refer to Infineon's web site www.infineon.com

TO-262 Package Outline (Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

DIODES

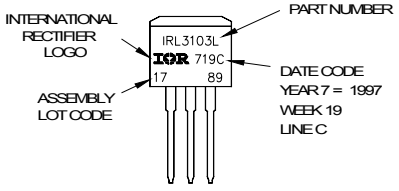
1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.- CATHODE
3.- ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

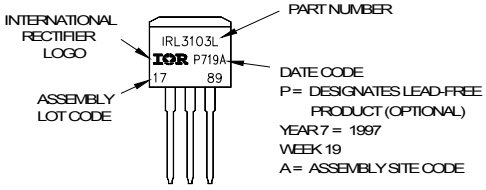
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead – Free"

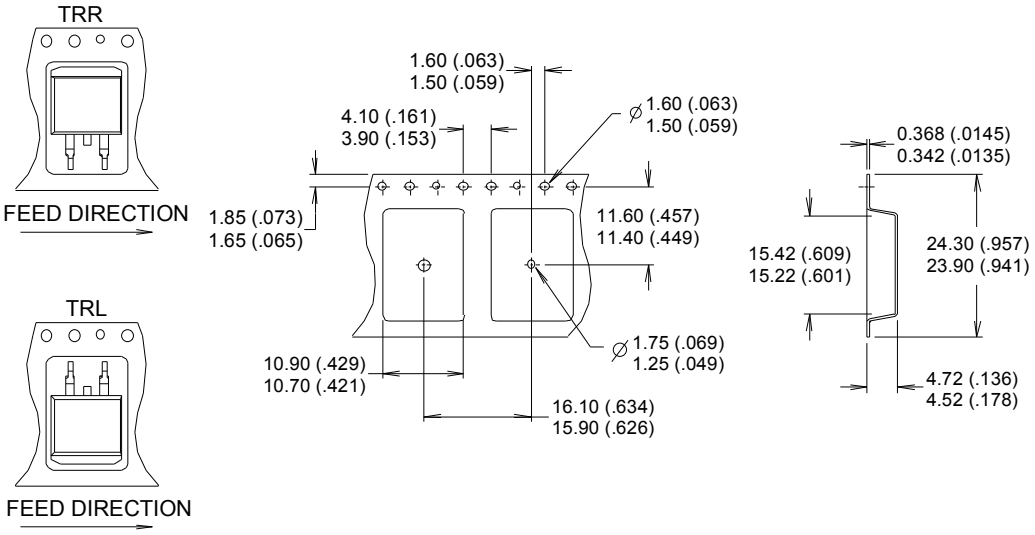


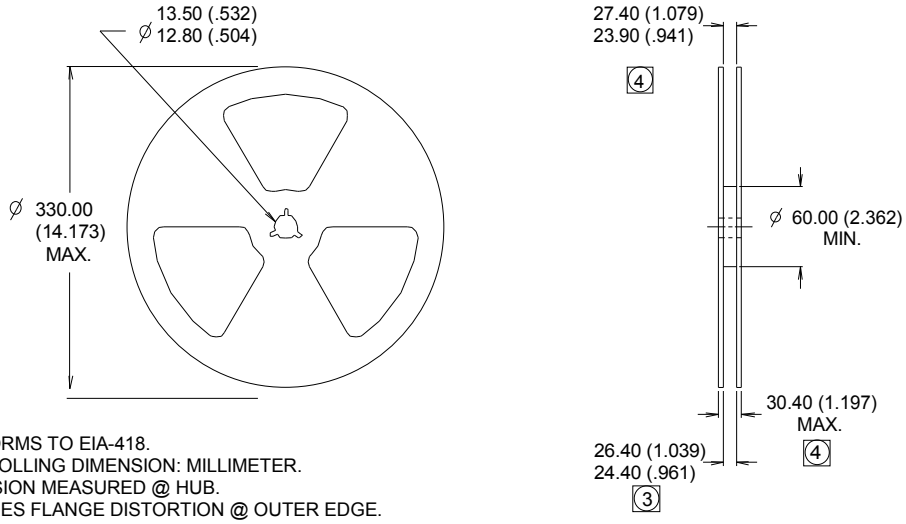
OR



Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D2-Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D2-Pak	MSL1 (per JEDEC J-STD-020D) ††
	TO-262	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at Infineon's web site www.infineon.com

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
5/27/2016	• Updated datasheet with corporate template. • Added disclaimer on last page. • TO-262 package was removed from ordering information since it is EOL on page 1.

Edition 2016-04-19
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
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Document reference
ifx1