Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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PD - 95473

International
IOR Rectifier

SMPS MOSFET

IRFB260NPbF

HEXFET® Power MOSFET

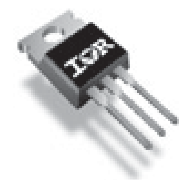
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	**0.040Ω**	**56A**

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	56	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	40	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	10	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

Notes ① through ⑤ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	V_{GS} = 10V, I_D = 34A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V

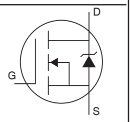
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	29	—	—	S	V_{DS} = 50V, I_D = 34A
Q_g	Total Gate Charge	—	150	220	nC	I_D = 34A
Q_{gs}	Gate-to-Source Charge	—	24	37		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	67	100		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 100V
t_r	Rise Time	—	64	—		I_D = 34A
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		R_G = 1.8Ω
t_f	Fall Time	—	50	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	4220	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	580	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	140	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	5080	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	230	—		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	500	—		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	450	mJ
I_{AR}	Avalanche Current①	—	34	A
E_{AR}	Repetitive Avalanche Energy①	—	38	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 34A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	240	360	ns	T_J = 25°C, I_F = 34A
Q_{rr}	Reverse RecoveryCharge	—	2.1	3.2	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

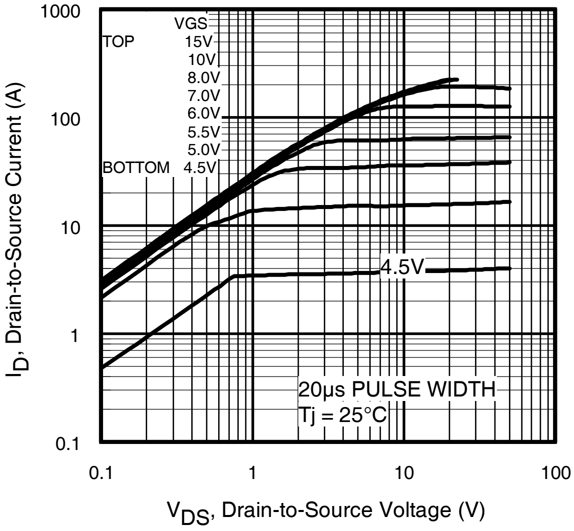


Fig 1. Typical Output Characteristics

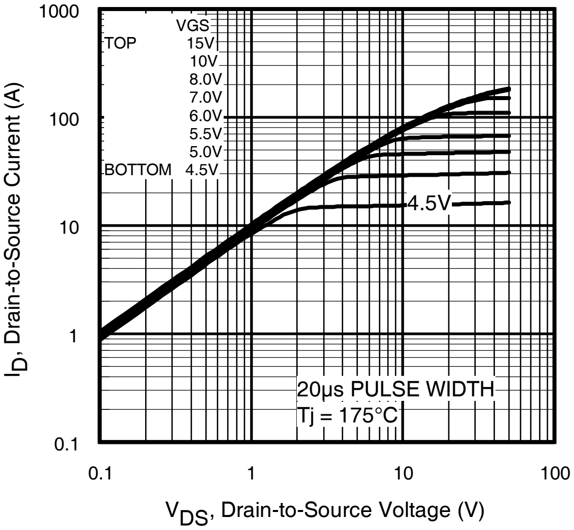


Fig 2. Typical Output Characteristics

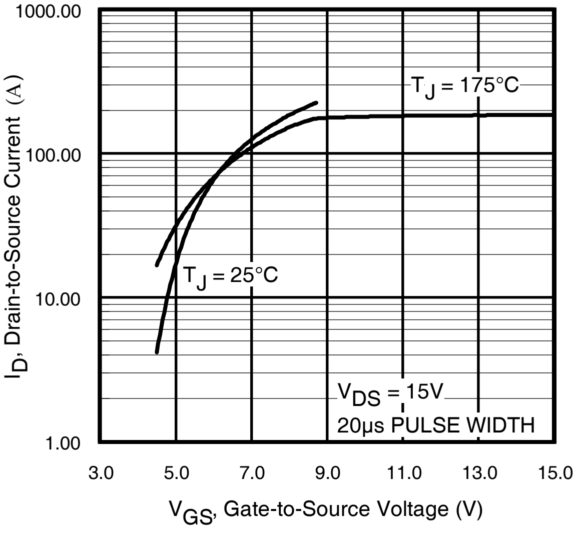


Fig 3. Typical Transfer Characteristics

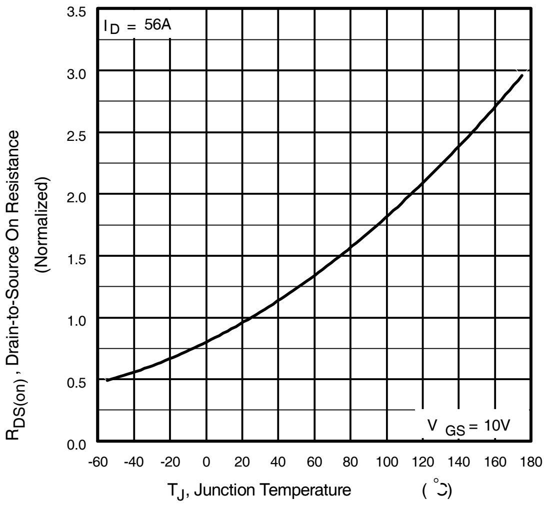


Fig 4. Normalized On-Resistance
Vs. Temperature

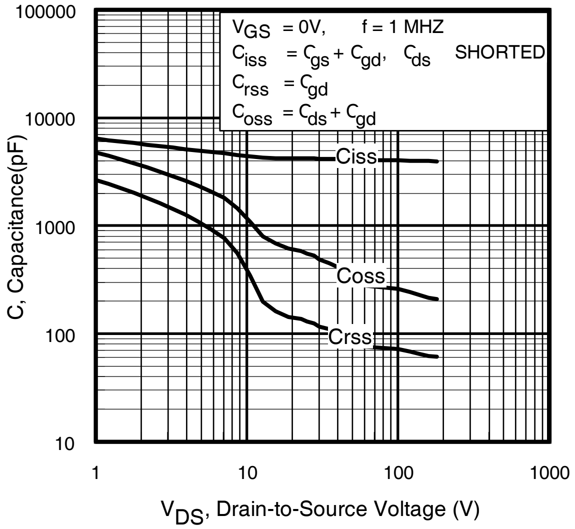


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

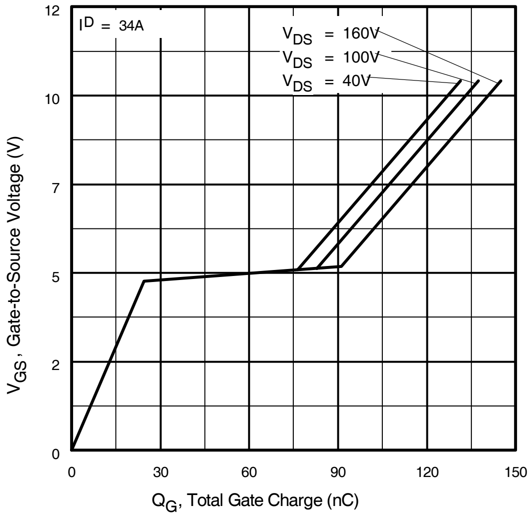


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

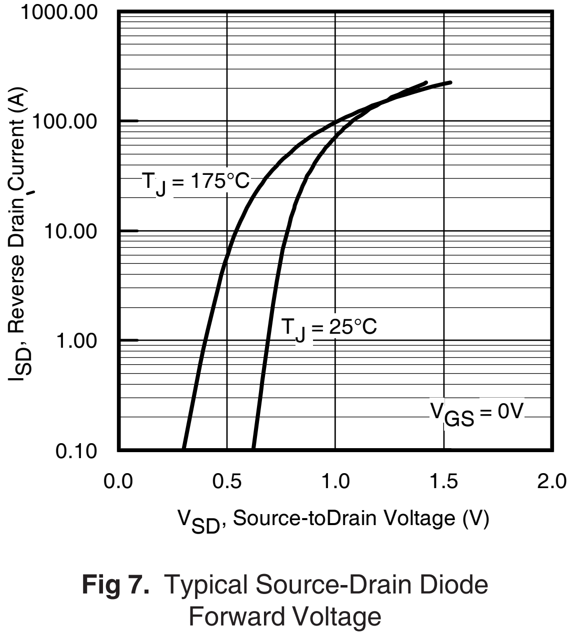


Fig 7. Typical Source-Drain Diode Forward Voltage

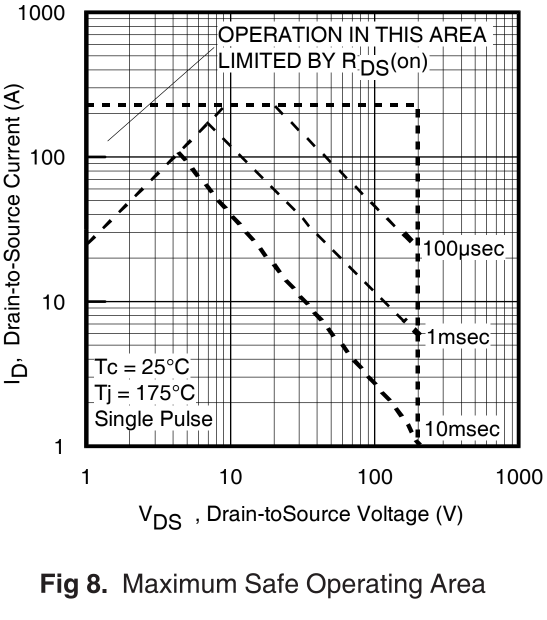


Fig 8. Maximum Safe Operating Area

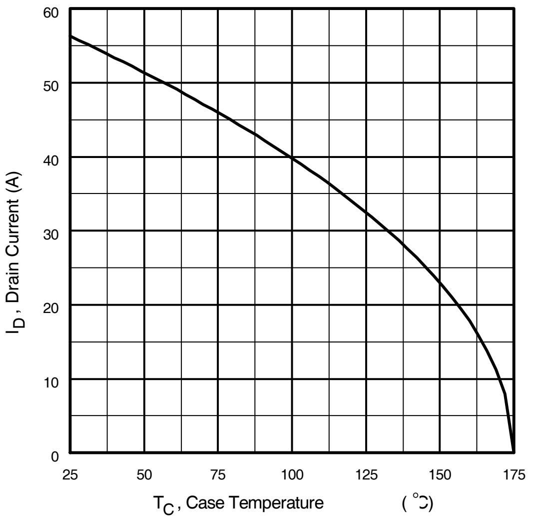


Fig 9. Maximum Drain Current Vs. Case Temperature

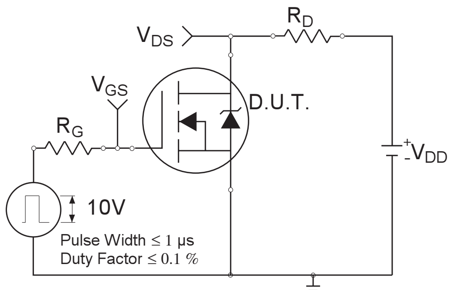


Fig 10a. Switching Time Test Circuit

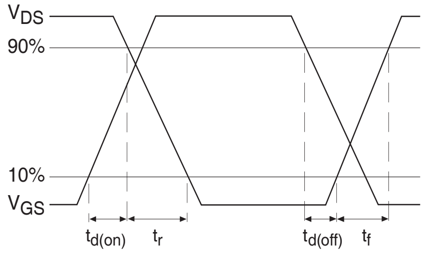


Fig 10b. Switching Time Waveforms

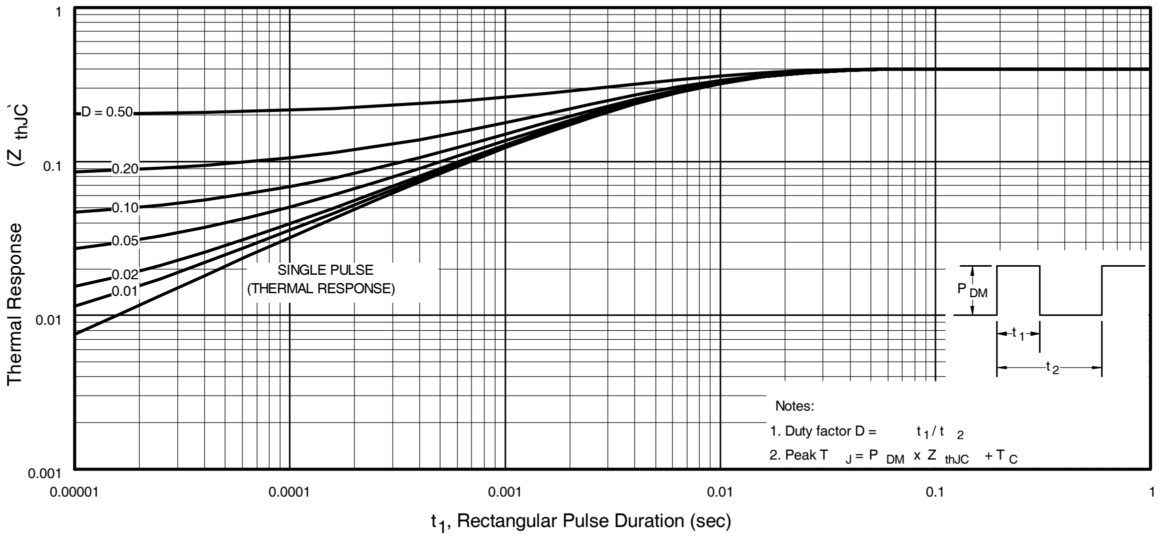


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

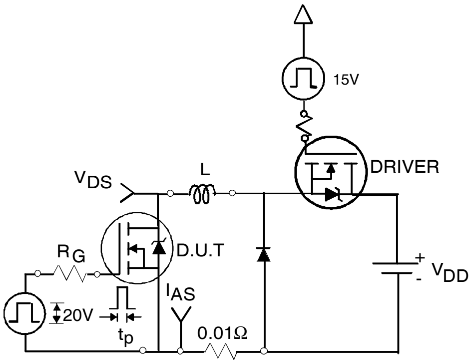


Fig 12a. Unclamped Inductive Test Circuit

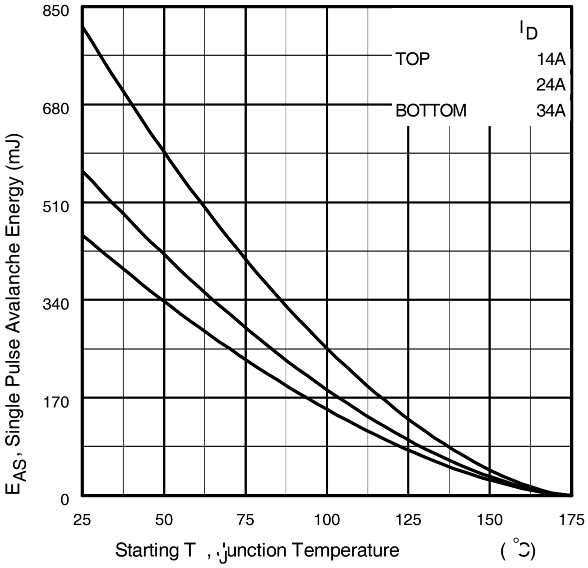


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

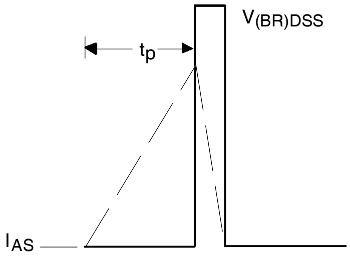


Fig 12b. Unclamped Inductive Waveforms

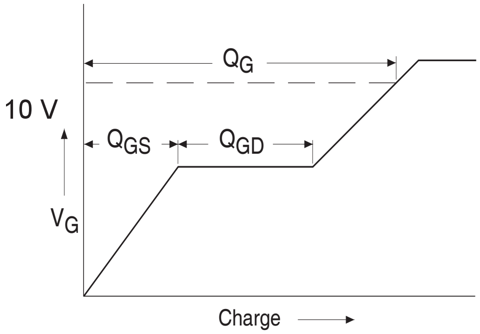


Fig 13a. Basic Gate Charge Waveform

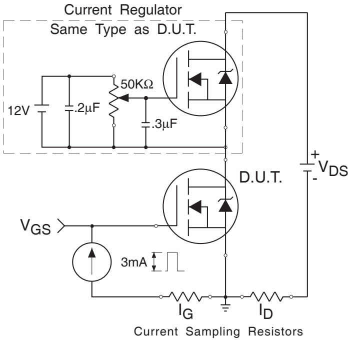
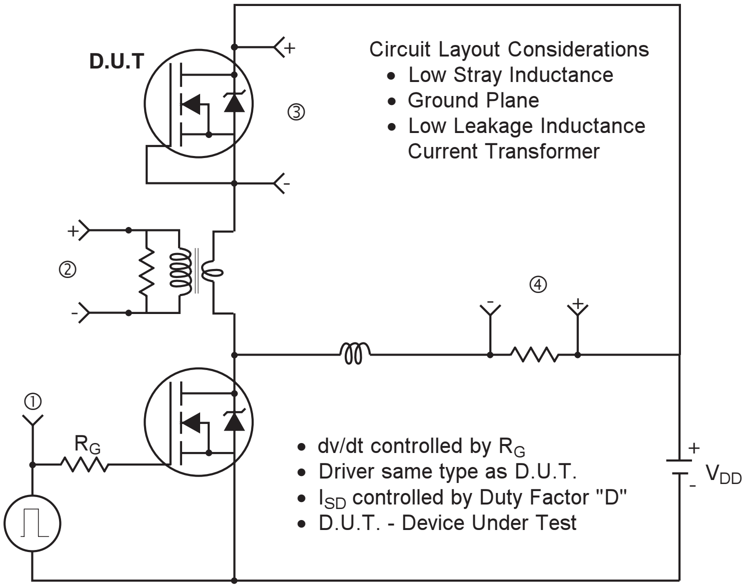


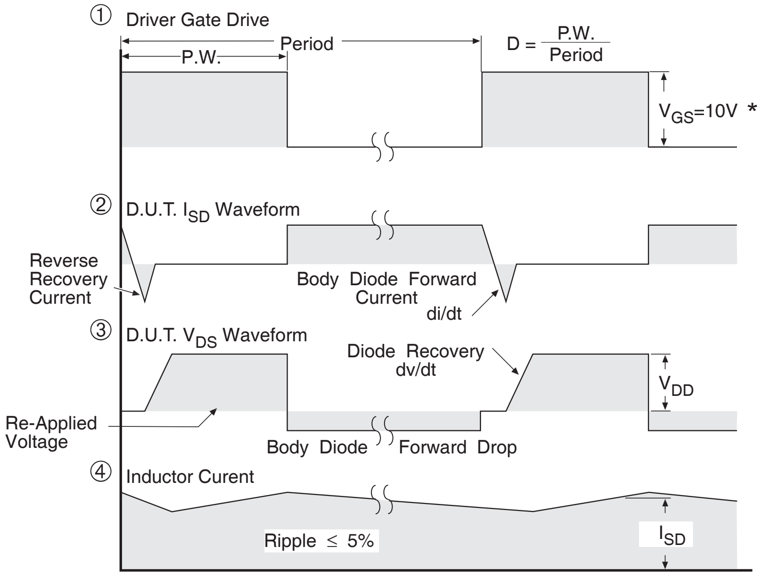
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

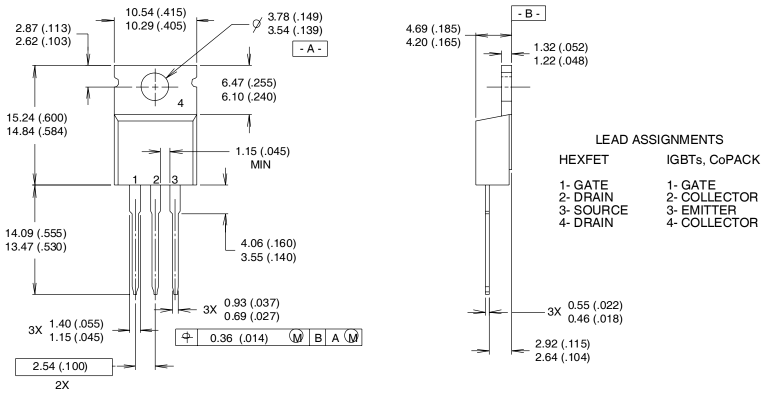
- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test



* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline



LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

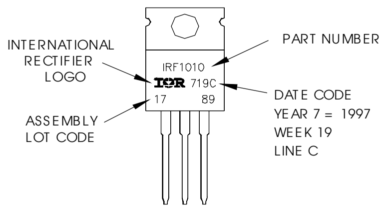
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, $L = 0.78mH$
$R_G = 25\Omega$, $I_{AS} = 34A$.

③ $I_{SD} \leq 34$, $di/dt \leq 480A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
$T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/