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## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.8
$Q_g$ (Max.) (nC)	7	
$Q_{gs}$ (nC)	2	
$Q_{gd}$ (nC)	7	
Configuration	Single	

### FEATURES

- For Automatic Insertion
- Compact Plastic Package
- End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
COMPLIANT

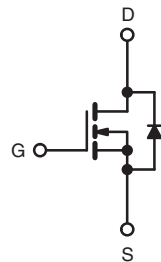
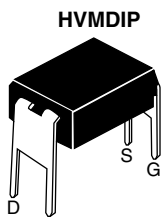
### Note

\* Pb containing terminations are not RoHS compliant, exemptions may apply

### DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the state-of-the-art in power device packaging.



N-Channel MOSFET

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD113PbF SiHFD113-E3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage <sup>a</sup>			$V_{DS}$	60	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	0.8	A
Pulsed Drain Current <sup>b</sup>			$I_{DM}$	6.4	
Linear Derating Factor				0.008	W/ $^\circ\text{C}$
Inductive Current, Clamped	L = 100 $\mu\text{H}$		$I_{LM}$	6.4	A
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	1.0	W
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 $^\circ\text{C}$	

### Notes

- $T_J = 25\text{ }^\circ\text{C}$  to 150  $^\circ\text{C}$
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{max. rating}, V_{GS} = 0\text{ V}$		-	-	250	$\mu\text{A}$
		$V_{DS} = \text{max. rating} \times 0.8, V_{GS} = 0\text{ V}, T_C = 125\text{ }^\circ\text{C}$		-	-	1000	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.	0.8	-	-	A
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 0.8\text{ A}$	-	0.6	0.8	$\Omega$
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $I_D = 0.8\text{ A}$		0.8	1.2	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$		-	135	200	pF
Output Capacitance	$C_{oss}$			-	80	100	
Reverse Transfer Capacitance	$C_{rss}$			-	20	25	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A},$ $V_{DS} = 0.8\text{ max. rating}$	-	5	7	nC
Gate-Source Charge	$Q_{gs}$			-	2	-	
Gate-Drain Charge	$Q_{gd}$			-	7	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 0.5 V_{DS}, I_D = 0.8\text{ A},$ $R_g = 50\text{ }\Omega$		-	10	20	ns
Rise Time	$t_r$			-	15	25	
Turn-Off Delay Time	$t_{d(off)}$			-	15	25	
Fall Time	$t_f$			-	10	20	
Internal Drain Inductance	$L_D$	Between lead, 2 mm (0.08") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	$L_S$			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	0.8	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	6.4	
Body Diode Voltage <sup>a</sup>	$V_{SD}$	$T_A = 25\text{ }^\circ\text{C}, I_S = 0.8\text{ A}, V_{GS} = 0\text{ V}$		-	-	2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 150\text{ }^\circ\text{C}, I_F = 1.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		-	100	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.2	-	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

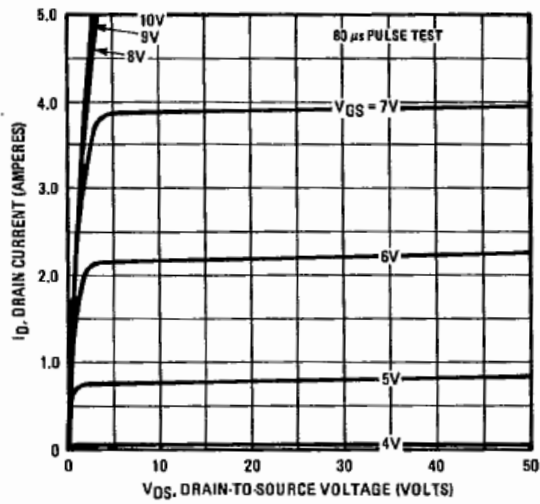


Fig. 1 - Typical Output Characteristics

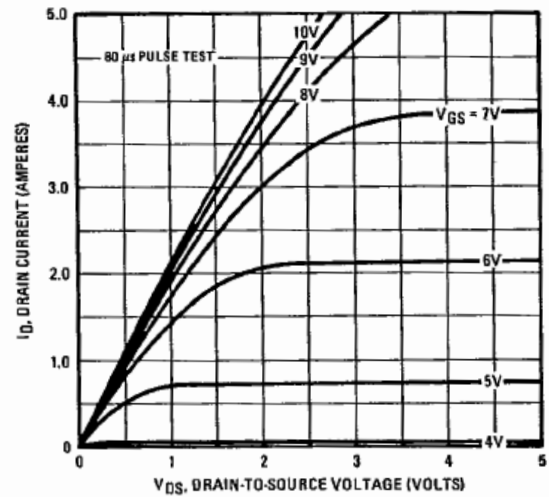


Fig. 3 - Typical Saturation Characteristics

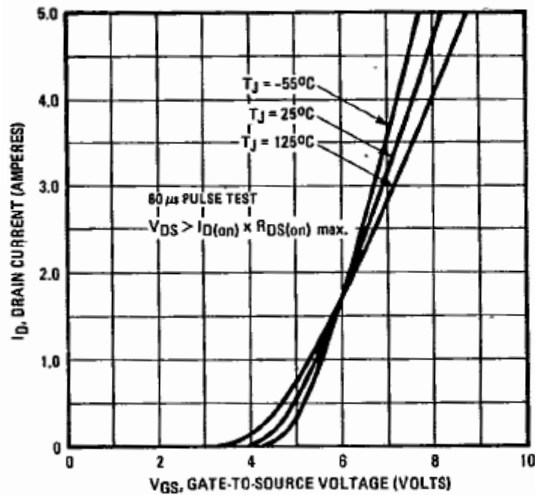


Fig. 2 - Typical Transfer Characteristics

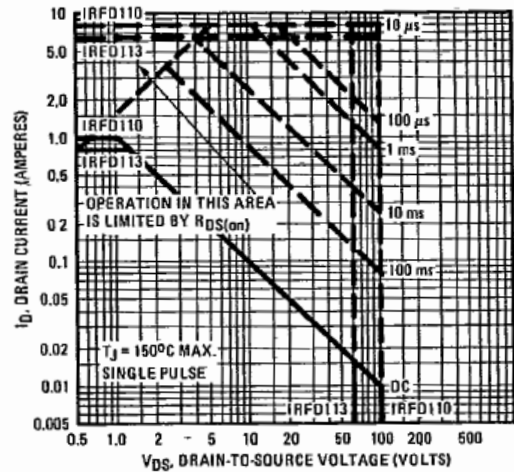


Fig. 4 - Maximum Safe Operating Area

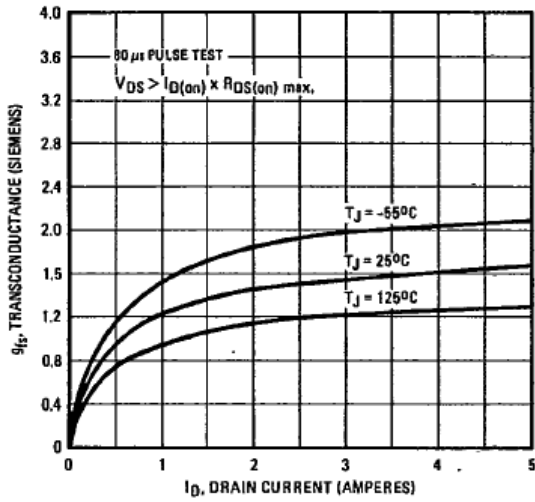


Fig. 5 - Typical Transconductance vs. Drain Current

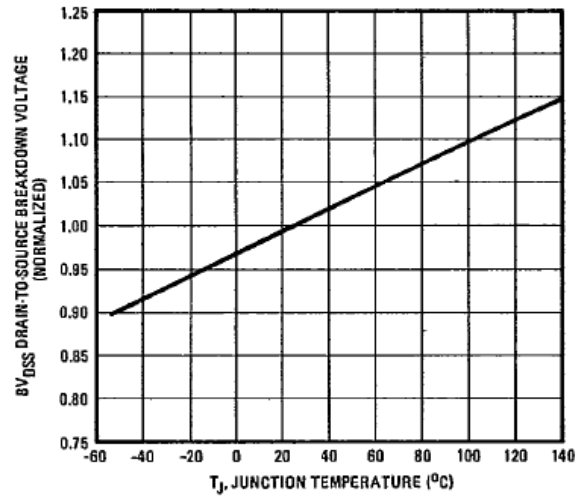


Fig. 7 - Breakdown Voltage vs. Temperature

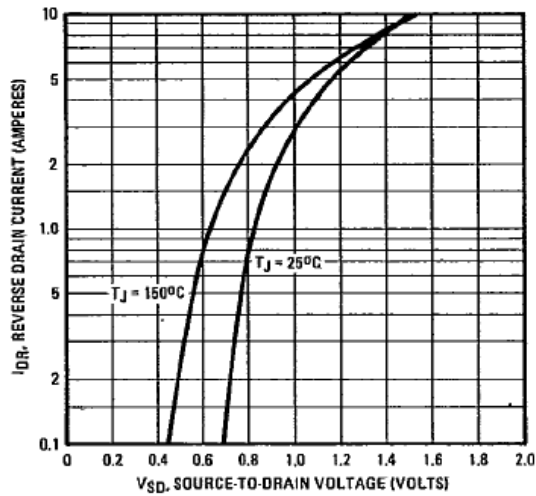


Fig. 6 - Typical Source-Drain Diode Forward Voltage

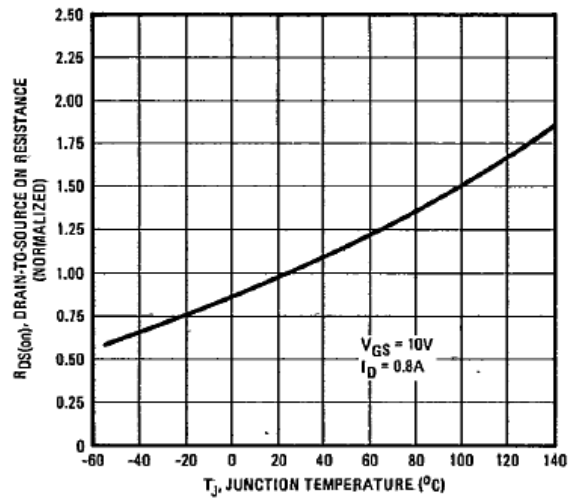


Fig. 8 - Normalized On-Resistance vs. Temperature

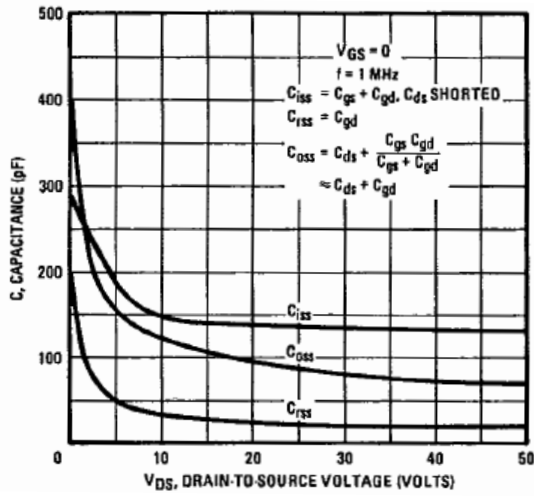


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

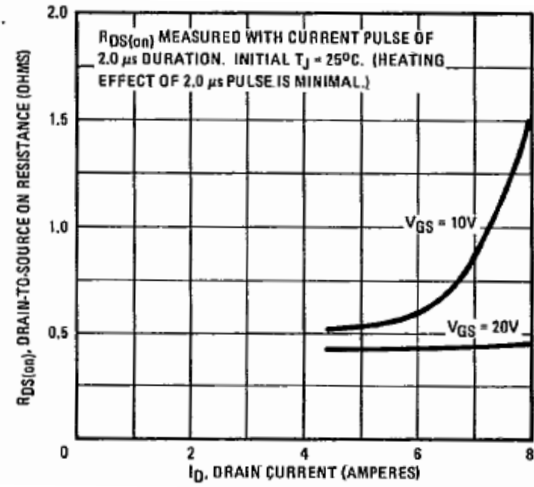


Fig. 11 - Typical On-Resistance vs. Drain Current

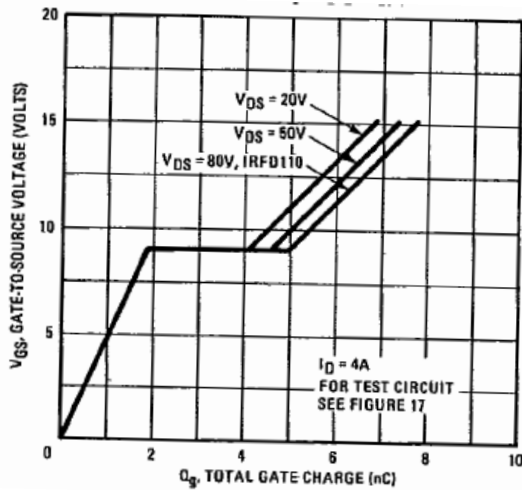


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

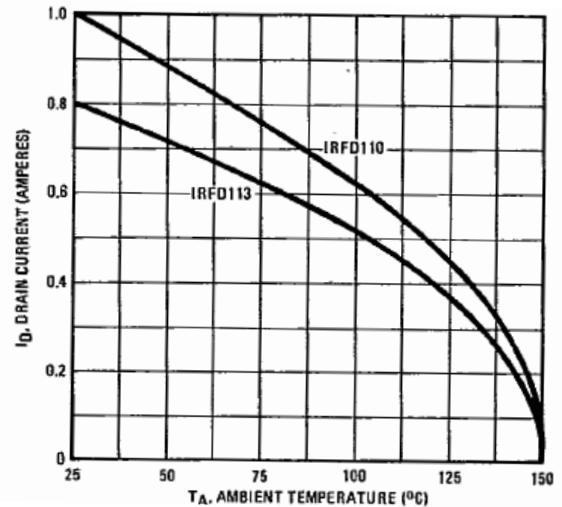


Fig. 12 - Maximum Drain Current vs. Case Temperature

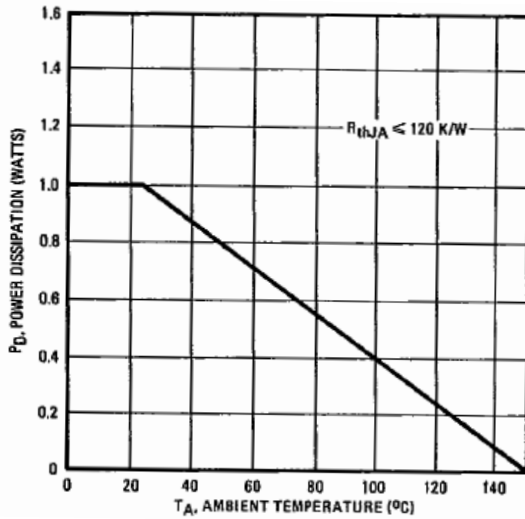


Fig. 13 - Power vs. Temperature Derating

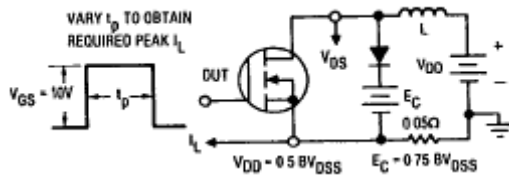


Fig. 14 - Clamped Inductive Test Circuit

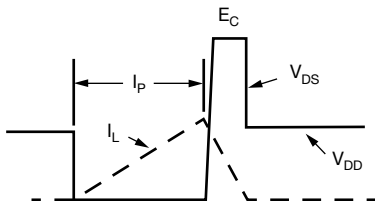


Fig. 15 - Clamped Inductive Waveforms

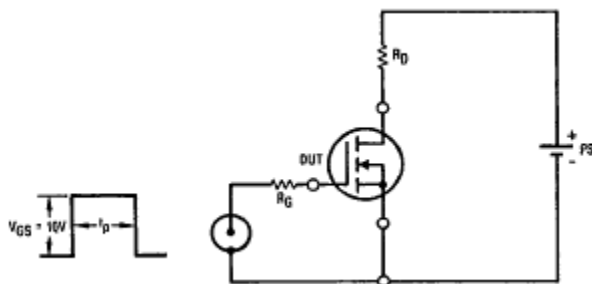


Fig. 16 - Switching Time Test Circuit

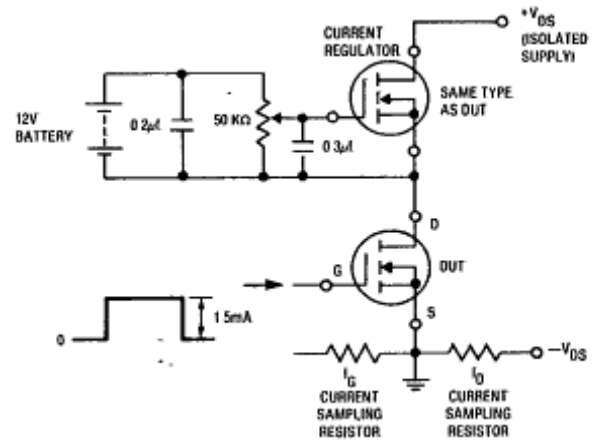


Fig. 17 - Gate Charge Test Circuit

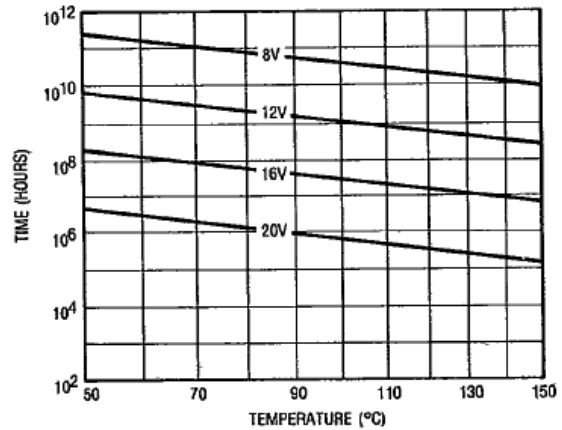


Fig. 18 - Typical Time to Accumulated 1% Gate Failure

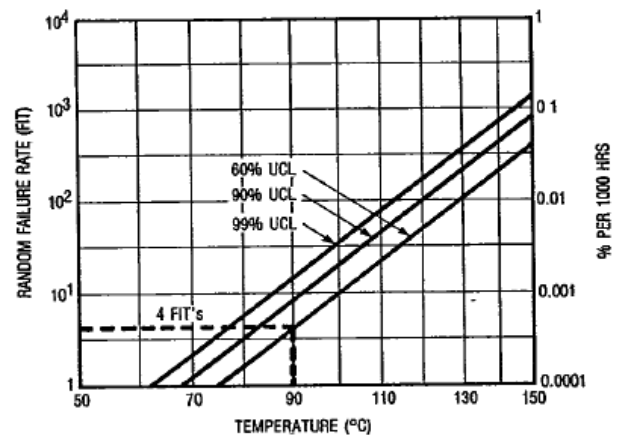
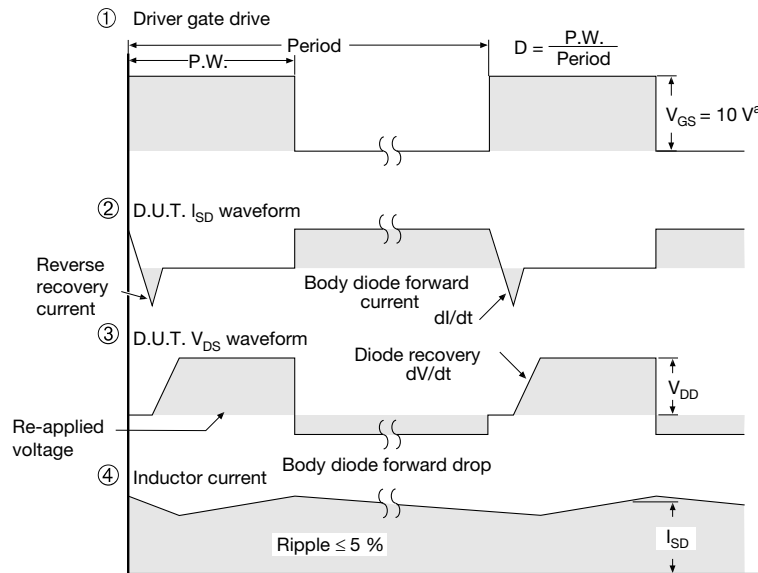
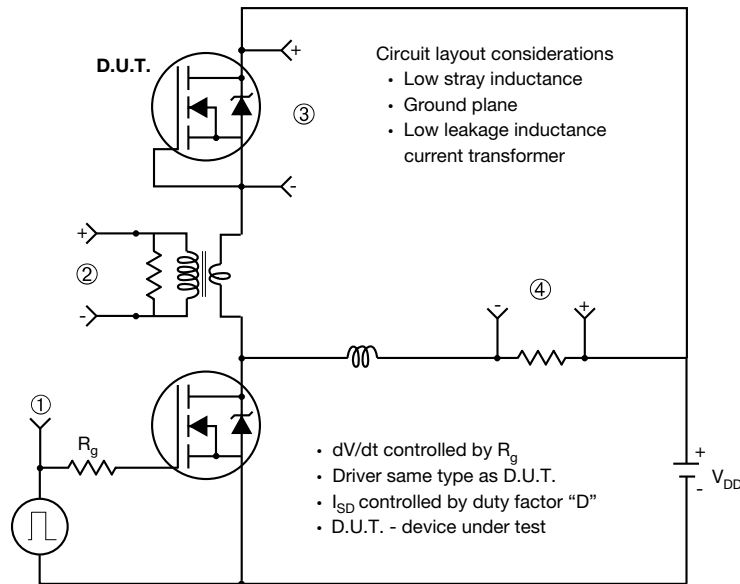


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 20 - For N-Channel**

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