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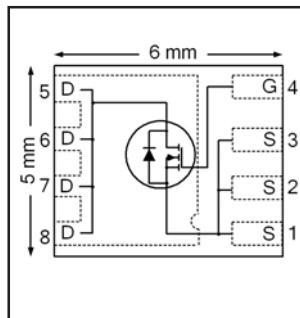
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



HEXFET® Power MOSFET

V_{DS}	100	V
$R_{DS(on)}$ max (@ $V_{GS} = 10V$)	9.0	mΩ
Q_g (typical)	67	nC
R_G (typical)	1.2	Ω
I_D (@ $T_{c(Bottom)} = 25^\circ C$)	100 ⑥	A



Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications

Features and Benefits

Features

Low $R_{DS(on)}$ (< 9 mΩ)
Low Thermal Resistance to PCB (<0.5°C/W)
100% R_g tested
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

Benefits

Lower Conduction Losses
Increased Power Density
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

results in
⇒

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH5010TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH5010TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	13	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	11	
I_D @ $T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	100⑥	
I_D @ $T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	70	
I_{DM}	Pulsed Drain Current ①	400	
P_D @ $T_A = 25^\circ C$	Power Dissipation ⑤	3.6	W
P_D @ $T_{c(Bottom)} = 25^\circ C$	Power Dissipation ⑤	250	
	Linear Derating Factor ⑤	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 9.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.5	9.0	m Ω	$V_{GS} = 10V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-8.3	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	206	—	—	S	$V_{DS} = 25V, I_D = 50A$
Q_g	Total Gate Charge	—	67	101	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 50A$
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	12	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	5.3	—		
Q_{gd}	Gate-to-Drain Charge	—	18	—		
Q_{godr}	Gate Charge Overdrive	—	32	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	23.3	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	18	—		
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	9	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ $I_D = 50A$ $R_G = 1.3\Omega$
t_r	Rise Time	—	12	—		
$t_{d(off)}$	Turn-Off Delay Time	—	27	—		
t_f	Fall Time	—	8.6	—		
C_{iss}	Input Capacitance	—	4340	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	425	—		
C_{rss}	Reverse Transfer Capacitance	—	162	—		

Avalanche Characteristics

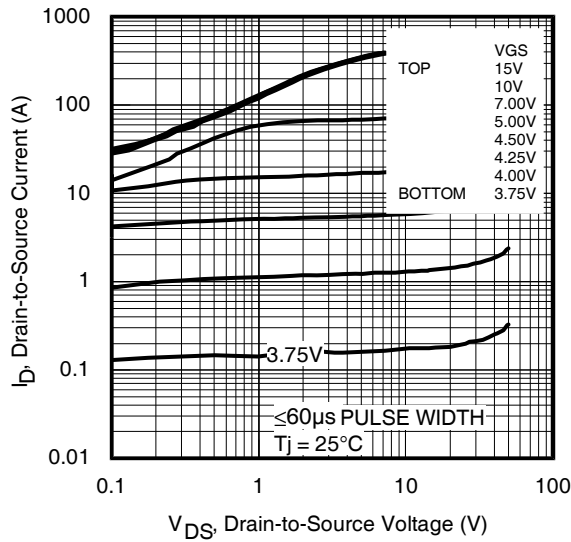
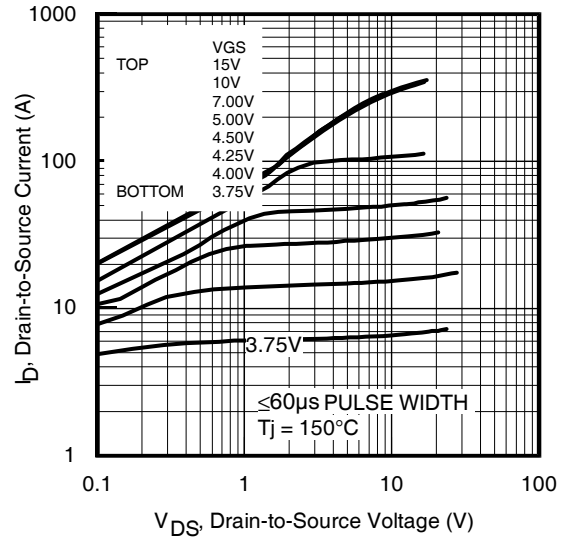
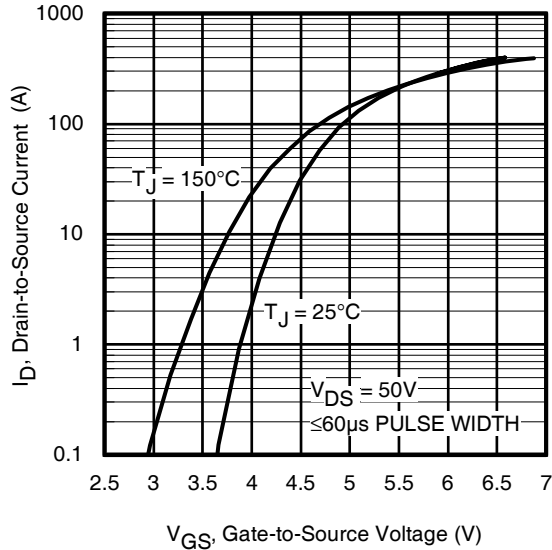
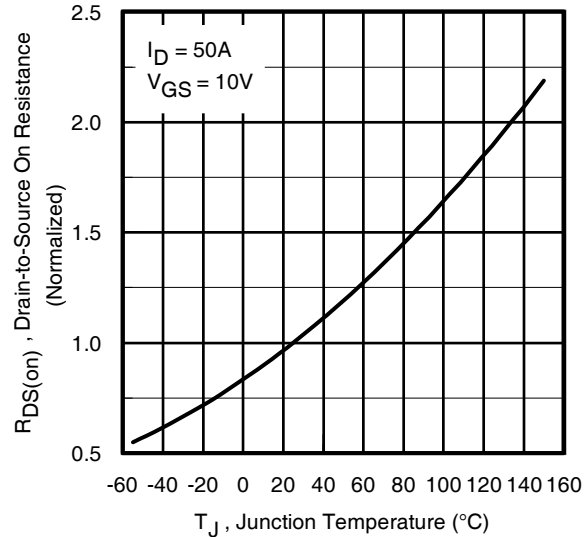
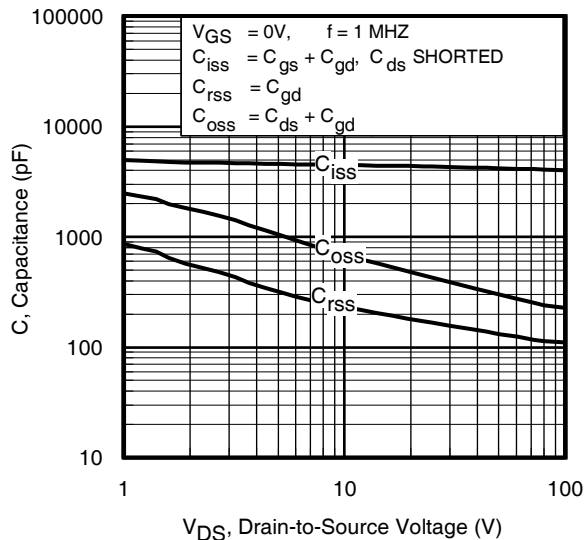
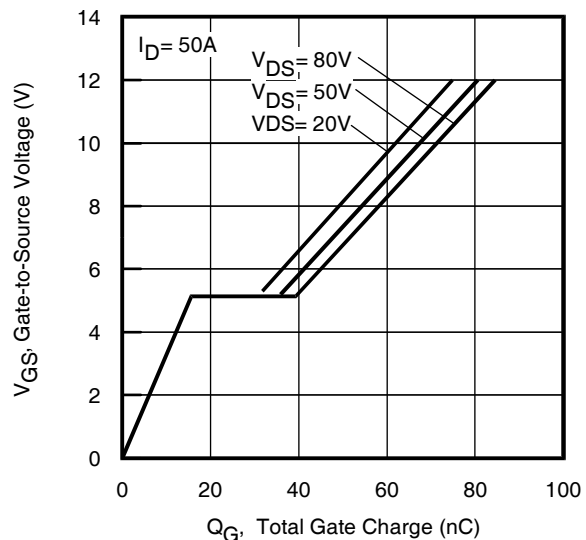
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	227	mJ
I_{AR}	Avalanche Current ①	—	50	A

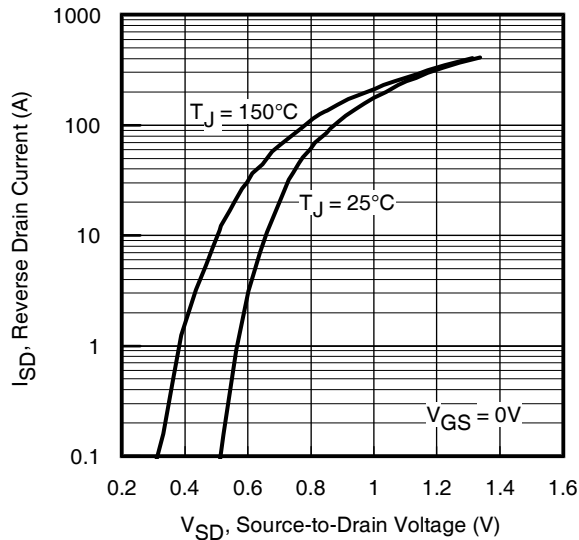
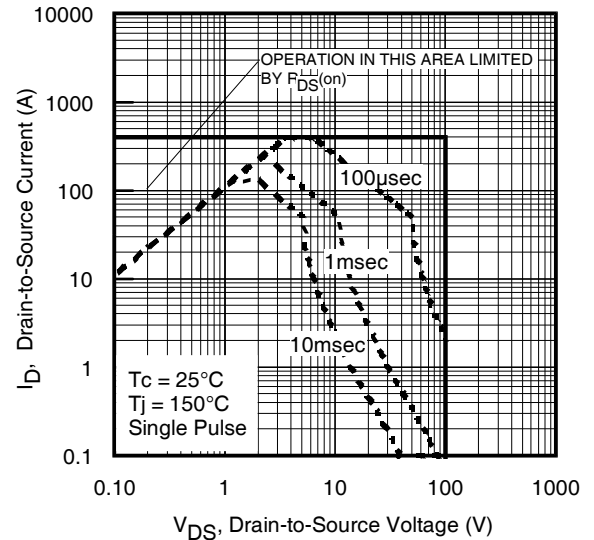
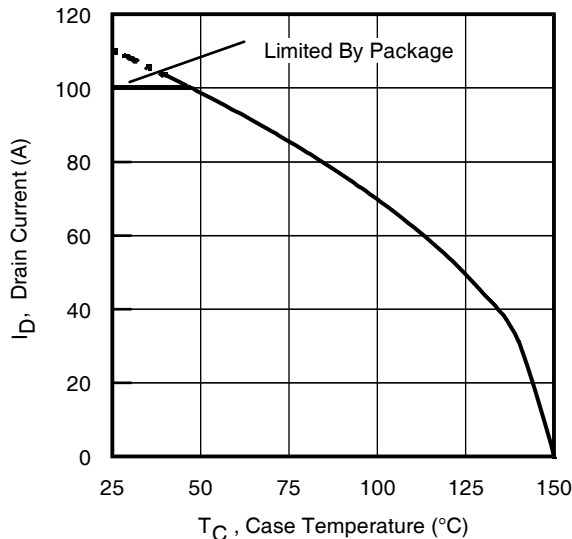
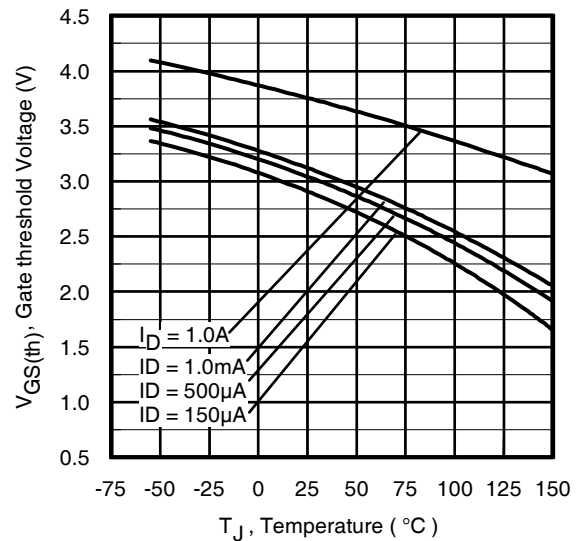
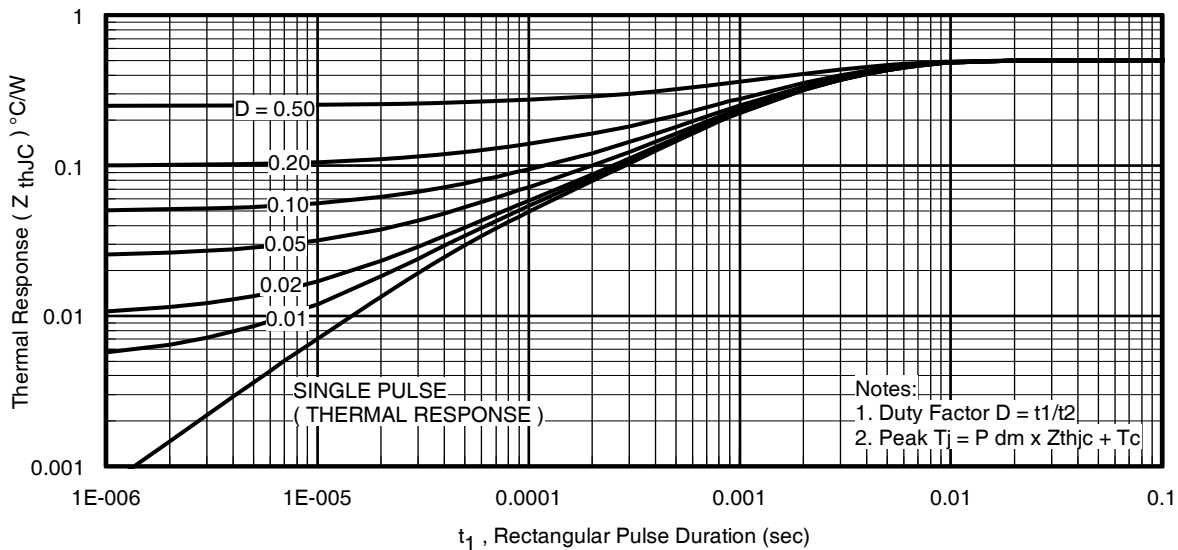
Diode Characteristics

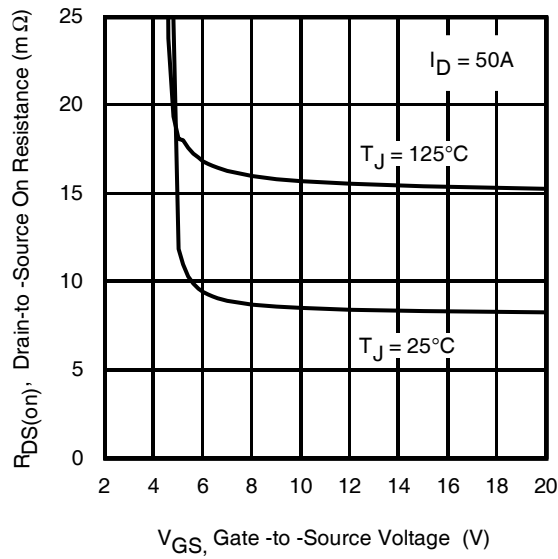
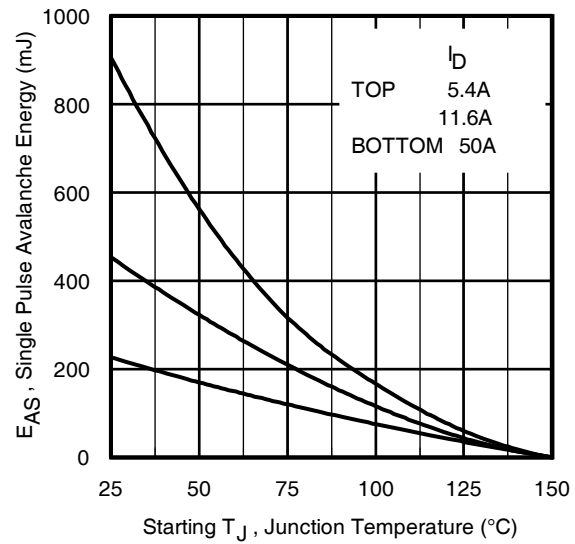
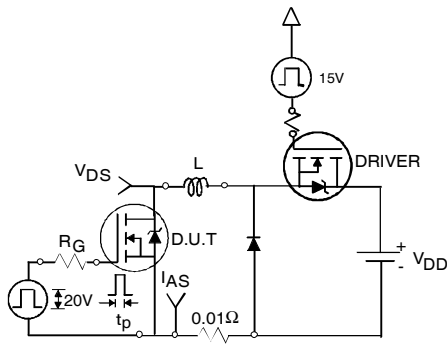
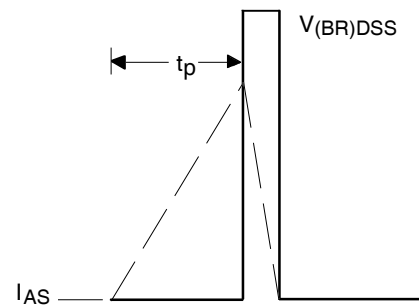
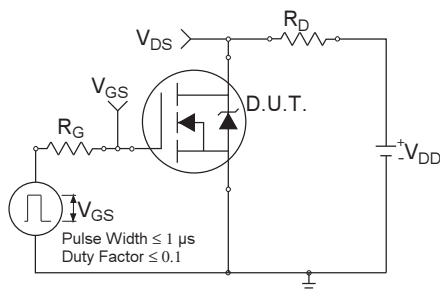
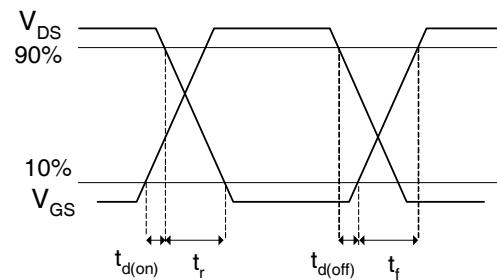
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	100 ^⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	34	51	ns	T _J = 25°C, I _F = 50A, V _{DD} = 50V
Q _{rr}	Reverse Recovery Charge	—	256	384	nC	di/dt = 500A/μs ③
t _{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				


Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	0.5	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	22	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current Vs. Case (Bottom) Temperature

Fig 10. Threshold Voltage Vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Unclamped Inductive Test Circuit

Fig 14b. Unclamped Inductive Waveforms

Fig 15a. Switching Time Test Circuit

Fig 15b. Switching Time Waveforms

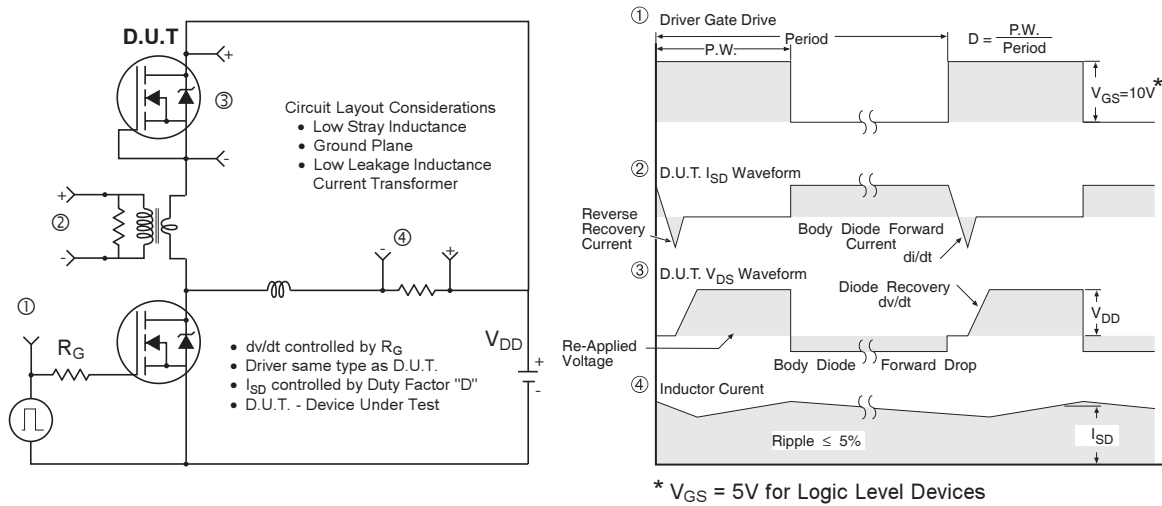


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

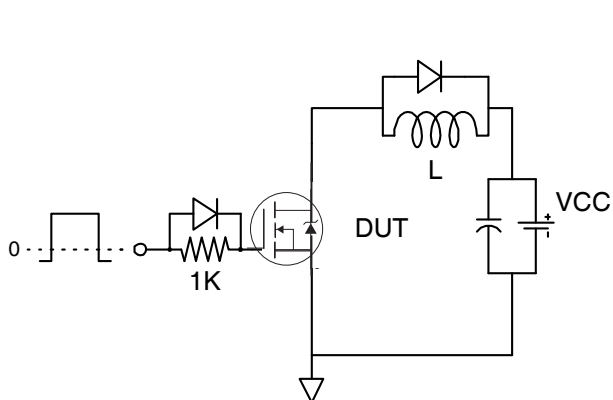


Fig 17. Gate Charge Test Circuit

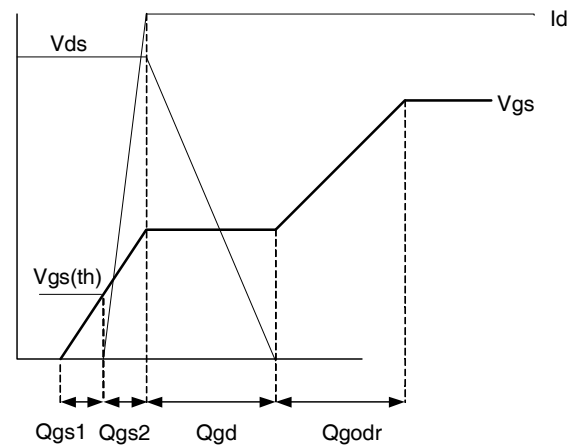
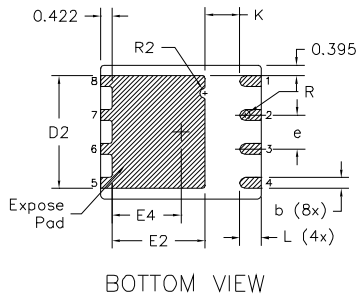
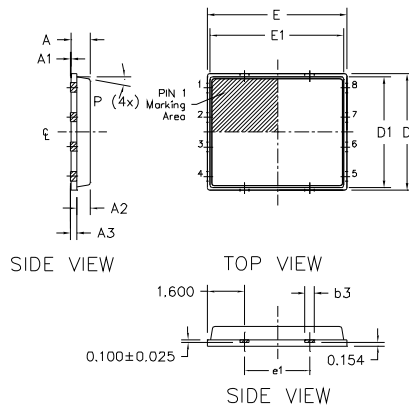


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details

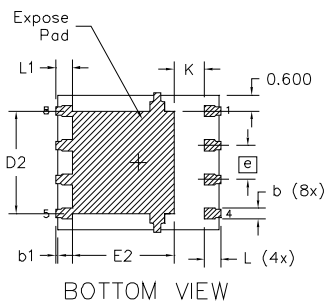
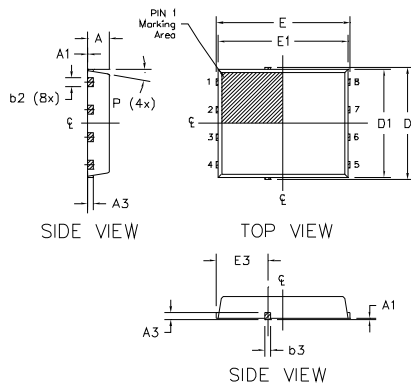


DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

Note:

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

PQFN 5x6 Outline "G" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254 REF		0.0100 REF	
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150 BSC		0.2028 BSC	
D1	5.000 BSC		0.1969 BSC	
D2	3.700	3.900	0.1457	0.1535
E	6.150 BSC		0.2421 BSC	
E1	6.000 BSC		0.2362 BSC	
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27 REF		0.050 REF	
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

Note:

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

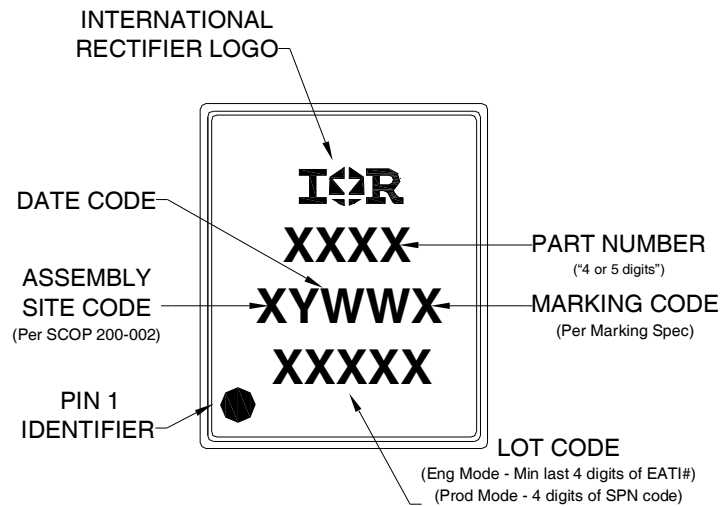
<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

<http://www.irf.com/technical-info/appnotes/an-1154.pdf>

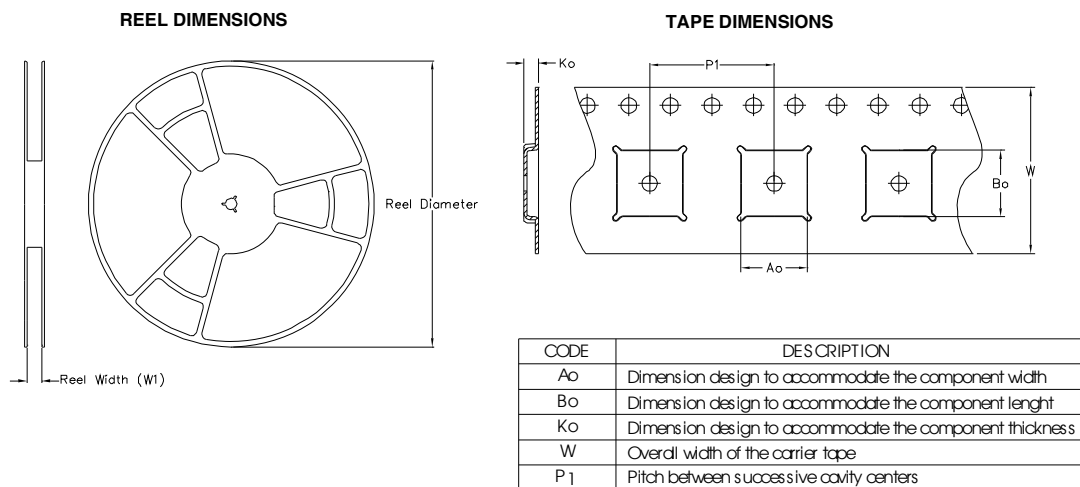
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Part Marking

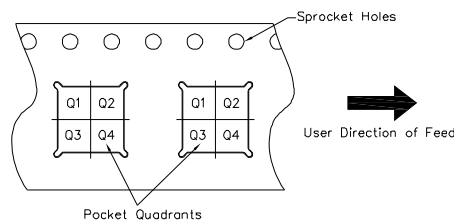


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Tape and Reel



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.
Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$, $L = 0.181\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability

Revision History

Date	Comments
5/11/2015	- Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) - Updated package outline for "option B" and added package outline for "option G" on page 7 - Updated tape and reel on page 8.
5/19/2015	- Updated package outline for "option G" on page 7. - Updated "IFX logo" on page 1 and page 9.