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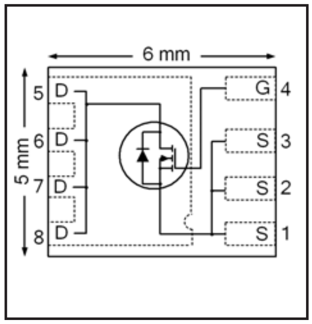
International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

IRFH7110PbF

HEXFET® Power MOSFET

V_{DS}	100	V
V_{gs} max	± 20	V
$R_{DS(on)}$ max (@V_{GS} = 10V)	13.5	mΩ
Q_{G} (typical)	58	nC
R_{G} (typical)	0.6	Ω
I_D (@$T_{c(Bottom)}$ = 25°C)	50⑦	A



PQFN 5X6 mm

Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features and Benefits

Features		Benefits
Low RDSon (< 13.5mW)		Lower Conduction Losses
Low Thermal Resistance to PCB (< 1.2°C/W)		Enables better thermal dissipation
Low Profile (<0.9 mm)	results in	Increased Power Density
Industry-Standard Pinout	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant Containing no Lead, no Bromide and no Halogen		Environmentally Friendlier
MSL1, Industrial Qualification		Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH7110TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
~~IRFH7110TR2PBF~~	~~PQFN 5mm x 6mm~~	~~Tape and Reel~~	~~400~~	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	11	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	8.6	A
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V	58⑥⑦	A
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	37⑥	A
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	50⑦	A
I_{DM}	Pulsed Drain Current ①	240	A
P_D @T_A = 25°C	Power Dissipation ⑤	3.6	W
P_D @$T_{C(Bottom)}$ = 25°C	Power Dissipation ⑤	104	W
	Linear Derating Factor ⑤	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑦ are on page 9

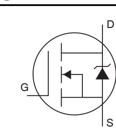
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	10.6	13.5	mΩ	V_{GS} = 10V, I_D = 35A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 100μA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-9.0	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	74	—	—	S	V_{DS} = 50V, I_D = 35A
Q_g	Total Gate Charge	—	58	87	nC	
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	11	—		V_{DS} = 50V
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	3.6	—		V_{GS} = 10V
Q_{gd}	Gate-to-Drain Charge	—	16	—		I_D = 35A
Q_{godr}	Gate Charge Overdrive	—	27.4	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	19.6	—		
Q_{oss}	Output Charge	—	17	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	0.6	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 50V, V_{GS} = 10V
t_r	Rise Time	—	23	—		I_D = 35A
$t_{d(off)}$	Turn-Off Delay Time	—	22	—		R_G=1.8Ω
t_f	Fall Time	—	18	—		
C_{iss}	Input Capacitance	—	3240	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	300	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	140	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	110	mJ
I_{AR}	Avalanche Current ①	—	35	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	50⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	240		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 35A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	27	41	ns	T_J = 25°C, I_F = 35A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	—	140	210	nC	di/dt = 500A/μs ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	1.2	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	32	
$R_{\theta JA}$	Junction-to-Ambient ④⑤	—	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	22	

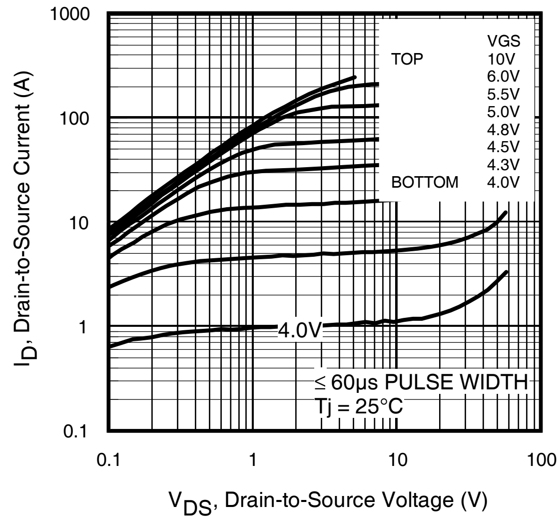


Fig 1. Typical Output Characteristics

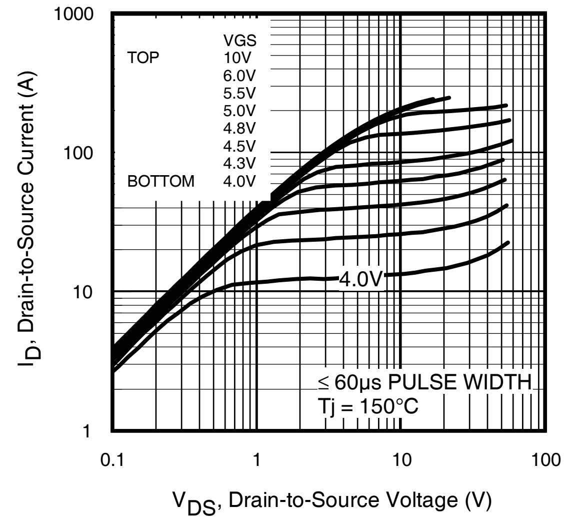


Fig 2. Typical Output Characteristics

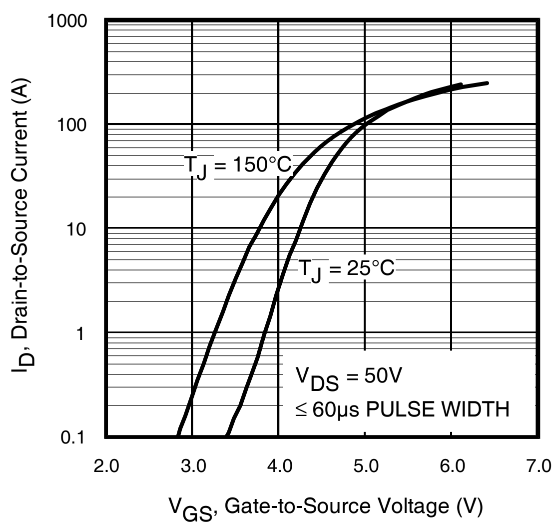


Fig 3. Typical Transfer Characteristics

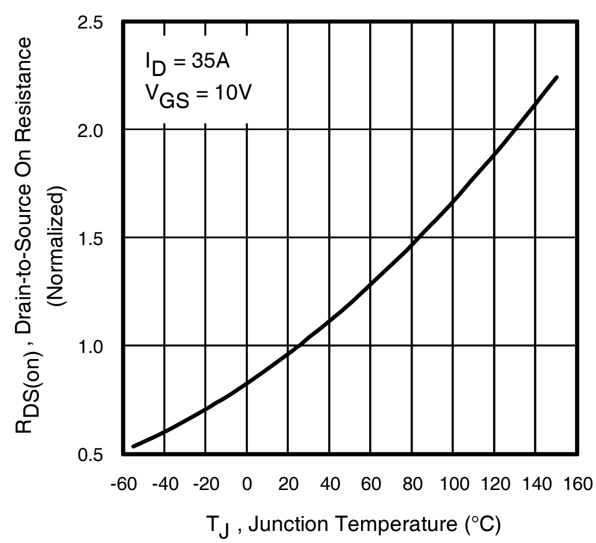


Fig 4. Normalized On-Resistance vs. Temperature

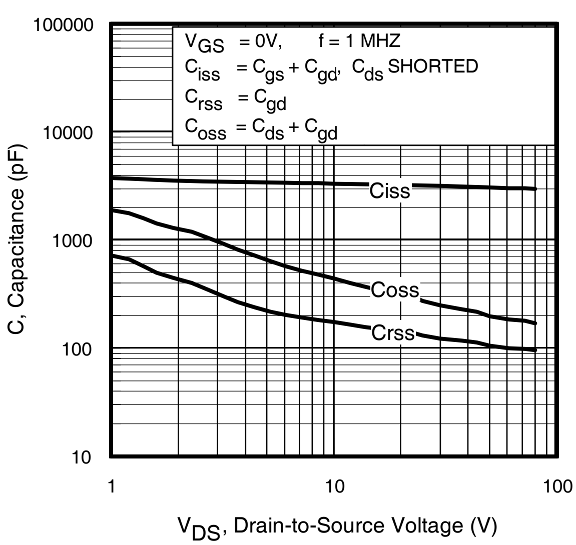


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

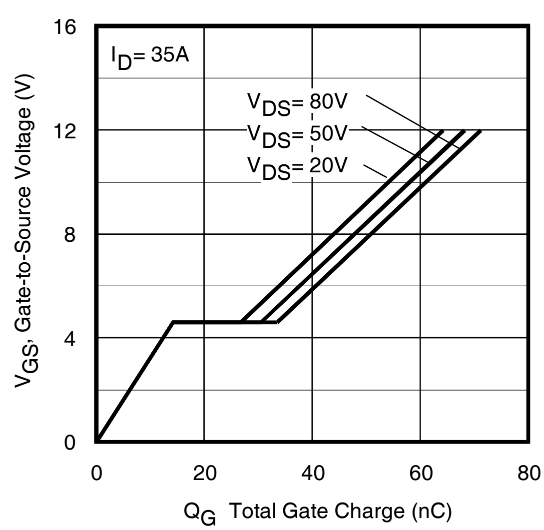


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

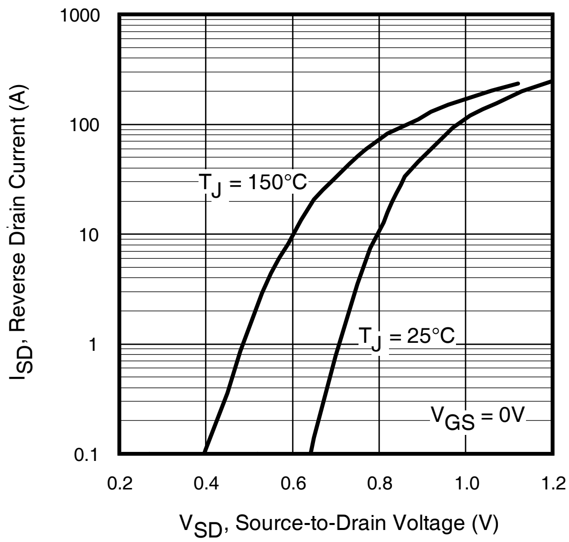


Fig 7. Typical Source-Drain Diode Forward Voltage

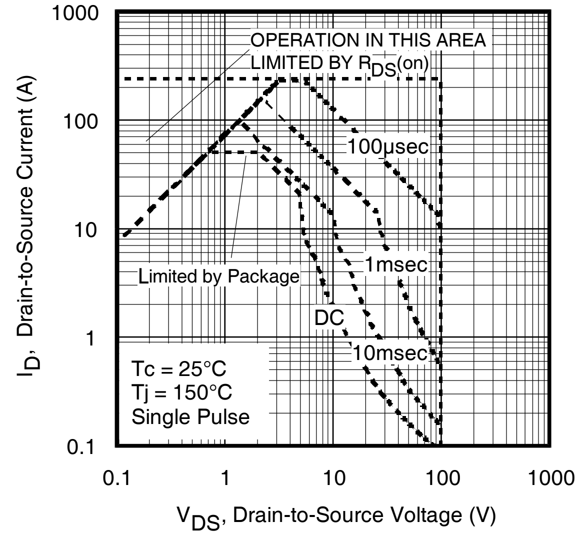


Fig 8. Maximum Safe Operating Area

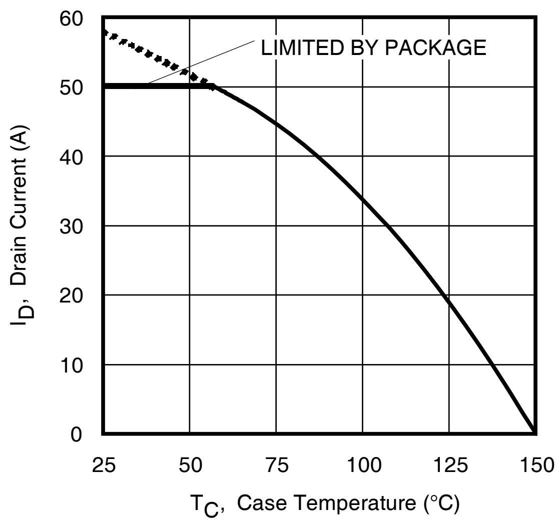


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

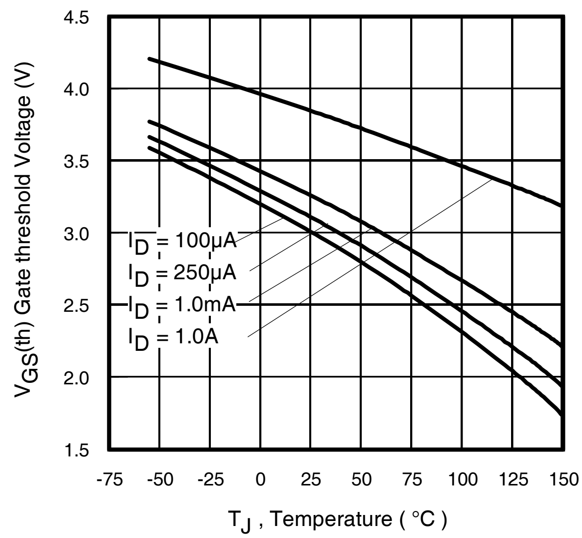


Fig 10. Threshold Voltage vs. Temperature

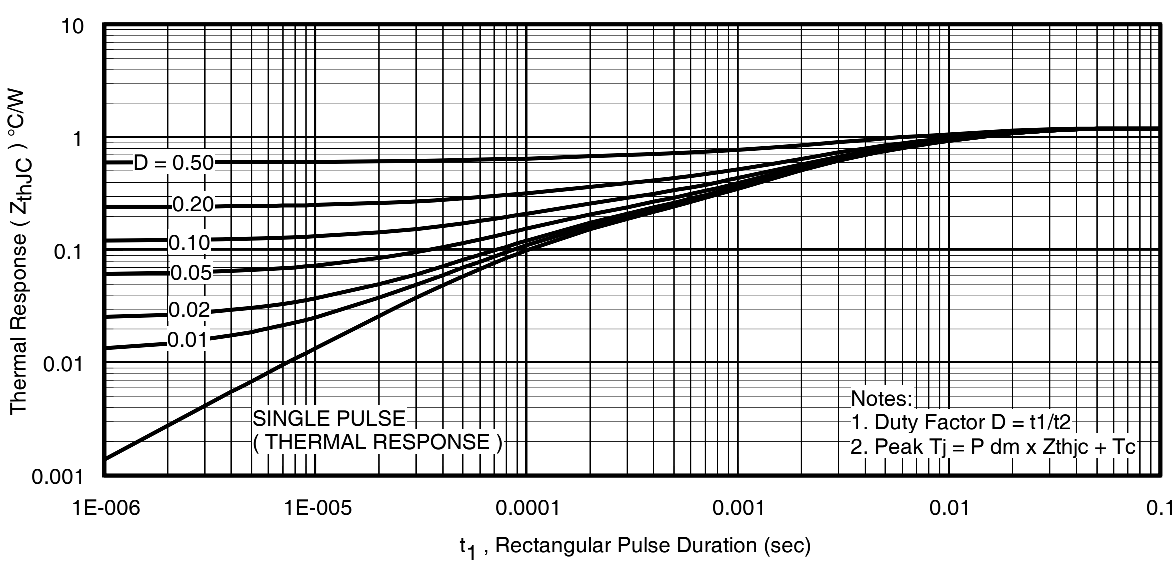


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

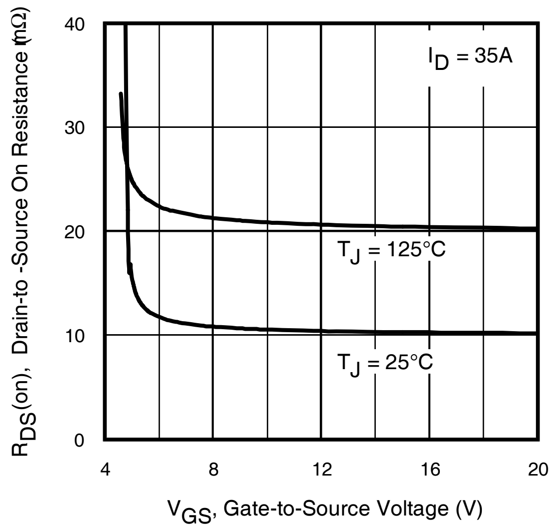


Fig 12. On-Resistance vs. Gate Voltage

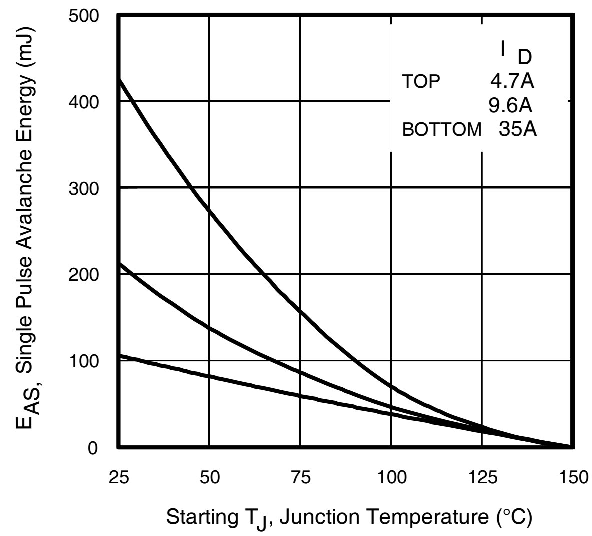


Fig 13. Maximum Avalanche Energy vs. Drain Current

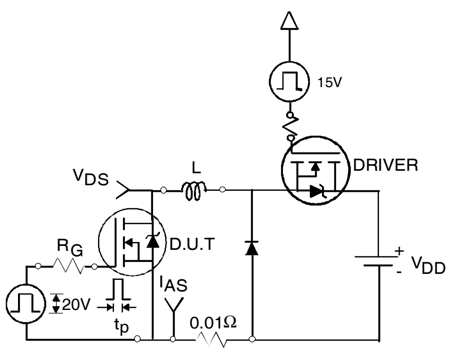


Fig 14a. Unclamped Inductive Test Circuit

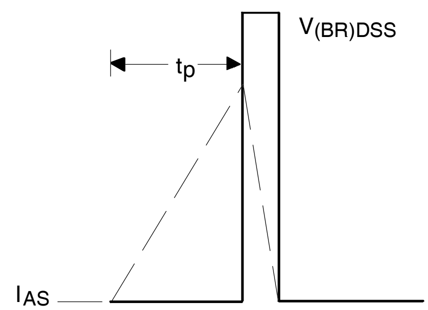


Fig 14b. Unclamped Inductive Waveforms

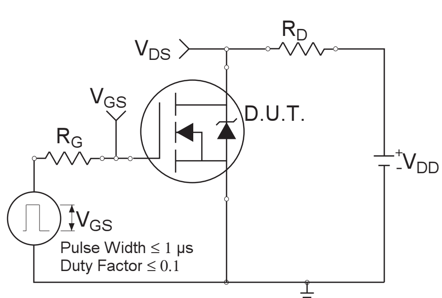


Fig 15a. Switching Time Test Circuit

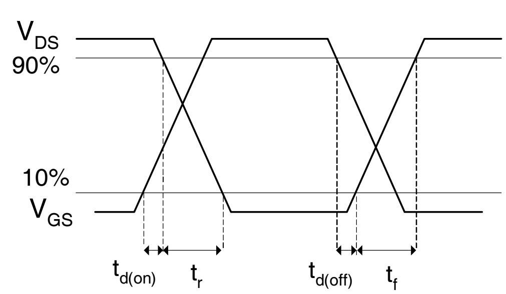


Fig 15b. Switching Time Waveforms

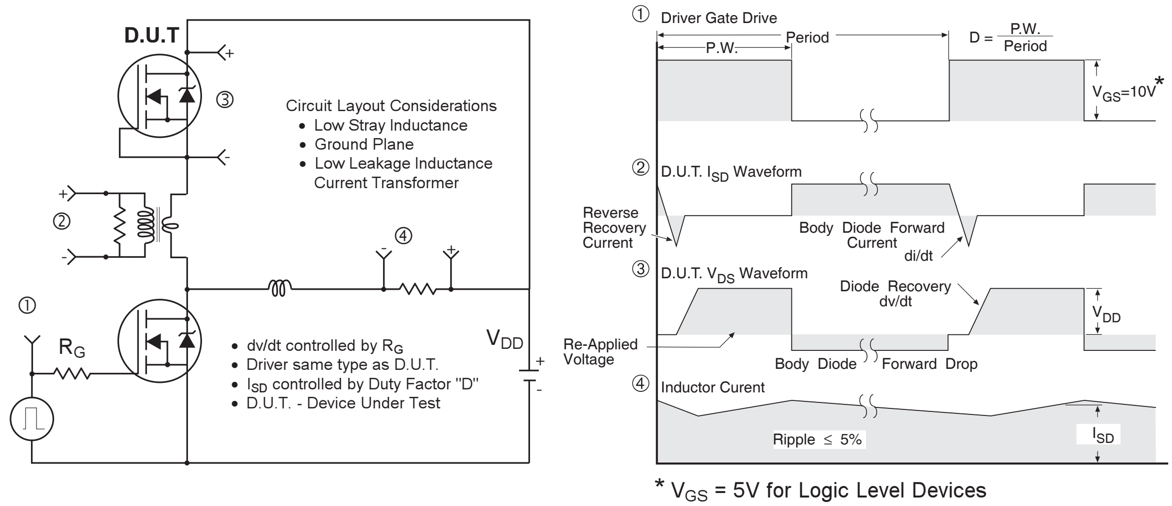


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

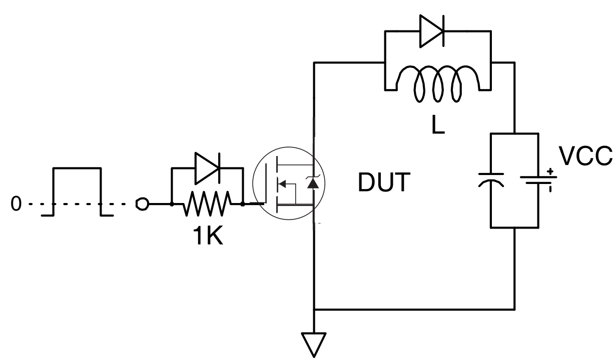


Fig 17. Gate Charge Test Circuit

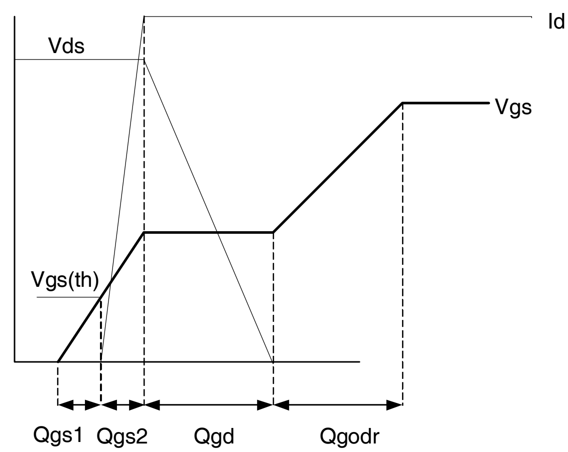
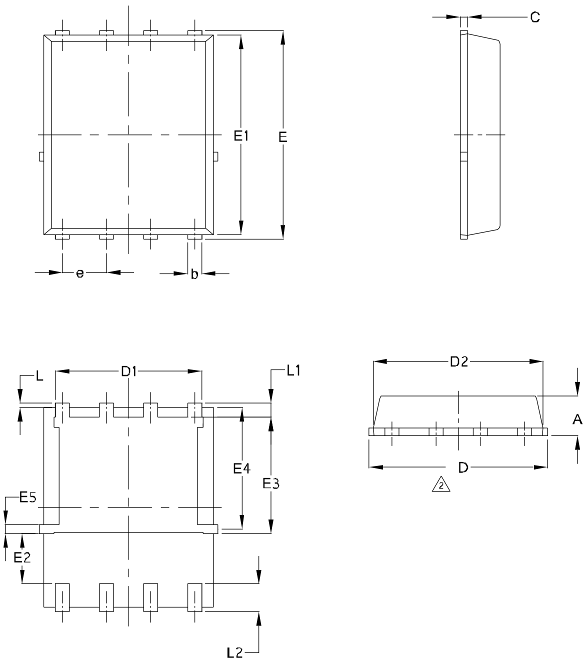


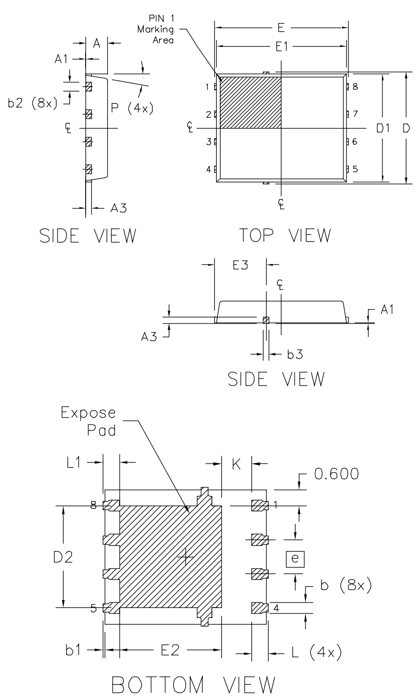
Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "E" Package Details



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.33	0.48	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.15	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.00	0.1890	0.1968
E	5.90	6.15	0.2323	0.2421
E1	5.65	6.00	0.2224	0.2362
E2	1.51	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.42	3.58	0.1346	0.1409
E5	0.18	0.32	0.0071	0.0126
e	1.27 BSC		0.050 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.66	0.0150	0.0260
L2	0.51	0.86	0.0201	0.0339
I	0	0.18	0	0.0071

PQFN 5x6 Outline "G" Package Details



SYMBOL \ DIM	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254 REF		0.0100 REF	
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150 BSC		0.2028 BSC	
D1	5.000 BSC		0.1969 BSC	
D2	3.700	3.900	0.1457	0.1535
E	6.150 BSC		0.2421 BSC	
E1	6.000 BSC		0.2362 BSC	
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27 REF		0.050 REF	
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

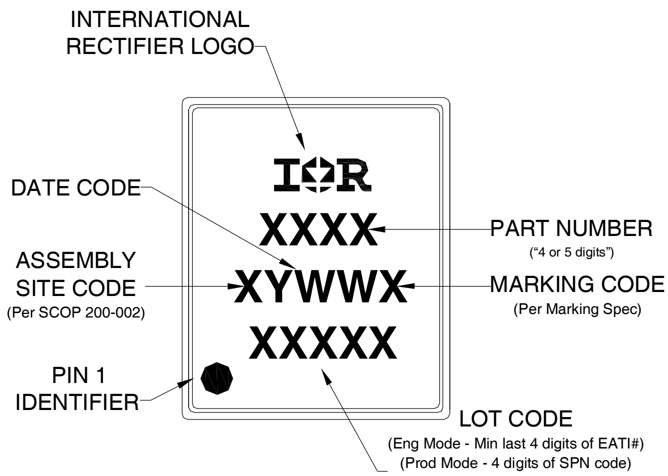
Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:
http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154:
http://www.irf.com/technical-info/appnotes/an-1154.pdf

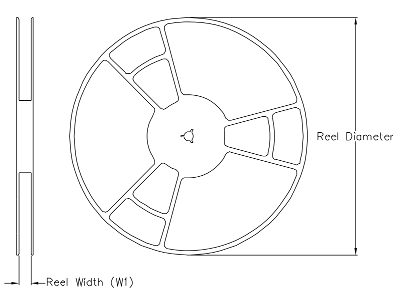
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

PQFN 5x6 Outline Part Marking

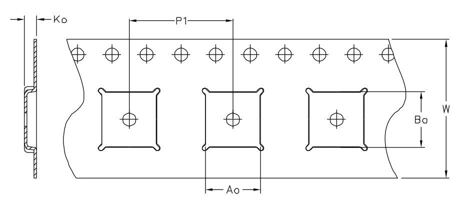


PQFN 5x6 Outline Tape and Reel

REEL DIMENSIONS

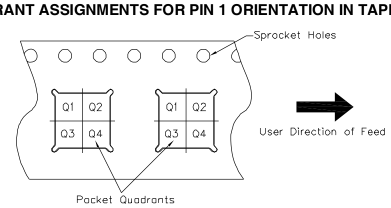


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Qualification information[†]

Qualification level	Industrial[††] (per JEDEC JESD47F [†††] guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D[†††])
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.174mH, R_G = 50Ω, I_{AS} = 35A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ R_θ is measured at T_J of approximately 90°C.
⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
⑥ Calculated continuous current based on maximum allowable junction temperature.
⑦ Package is limited to 50A by die-source to lead-frame bonding technology

Revision History

Date	Comment
5/13/2014	• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) • Updated Package outline on page 7. • Updated Tape and Reel on page 8. • Updated data sheet based on corporate template.
6/2/2015	• Corrected typo test condition for GFS from "25V" to "50V" on page 2. • Updated package outline for "option E" and added package outline for "option G" on page 7 • Updated "IFX" logo on page 1 & 9. • Updated tape and reel on page 8.

International Rectifier
AN INFINEON TECHNOLOGIES COMPANY

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