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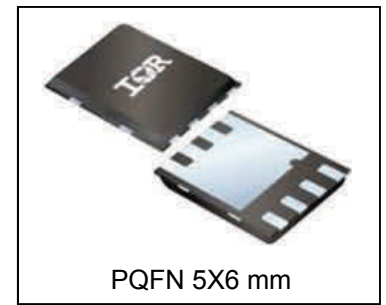
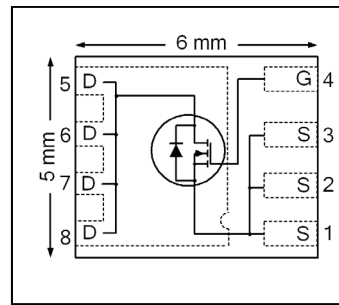
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



HEXFET® Power MOSFET

$V_{DSS}$	<b>100</b>	<b>V</b>
$R_{DS(on) \max}$ (@ $V_{GS} = 10V$ )	<b>8.0</b>	<b>mΩ</b>
$Q_g$ (typical)	<b>26</b>	<b>nC</b>
$R_g$ (typical)	<b>1.0</b>	<b>Ω</b>
$I_D$ (@ $T_C(Bottom) = 25^\circ C$ )	<b>80</b>	<b>A</b>



### Applications

- Primary Switch for High Frequency 48V/60V Telecom DC-DC Power Supplies
- Secondary Side Synchronous Rectifier
- Hot Swap and Active O-Ring

### Features

Low $R_{DS(ON)}$ (< 8.0mΩ)
Low Thermal Resistance to PCB (<1.2°C/W)
100% $R_g$ Tested
Low Profile (<1.05 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1

 results in  
 ⇒

### Benefits

Lower Conduction Losses
Increased Power Density
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7191PbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH7191TRPbF

### Absolute Maximum Ratings

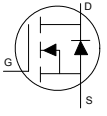
	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	15	A
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	80	
$I_D @ T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	51	
$I_{DM}$	Pulsed Drain Current ①	234	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.6	W
$P_D @ T_{C(Bottom)} = 25^\circ C$	Power Dissipation	104	
	Linear Derating Factor	0.03	W/°C
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

Notes ① through ⑤ are on page 9

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	103	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	6.2	8.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 48A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	3.6	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-4.9	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	112	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 48A
Q <sub>g</sub>	Total Gate Charge	—	26	39	nC	V <sub>DS</sub> = 50V V <sub>GS</sub> = 10V I <sub>D</sub> = 48A
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	4.7	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.9	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	8.3	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	12	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	10	—	nC	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V
Q <sub>oss</sub>	Output Charge	—	80	—		
R <sub>G</sub>	Gate Resistance	—	1.0	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	4.5	—	ns	V <sub>DD</sub> = 50V, V <sub>GS</sub> = 10V I <sub>D</sub> = 48A R <sub>G</sub> = 1.0Ω
t <sub>r</sub>	Rise Time	—	6.1	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	10.6	—		
t <sub>f</sub>	Fall Time	—	3.6	—		
C <sub>iss</sub>	Input Capacitance	—	1685	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	836	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	16	—		

**Diode Characteristics**

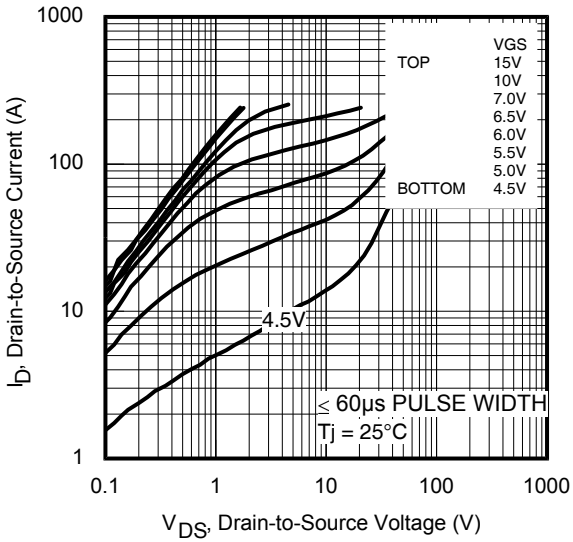
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	80	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	234	A	
V <sub>SD</sub>	Diode Forward Voltage	—	0.8	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 48A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	63	95	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 48A, V <sub>DD</sub> = 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	126	190	nC	di/dt = 100A/μs ③

**Avalanche Characteristics**

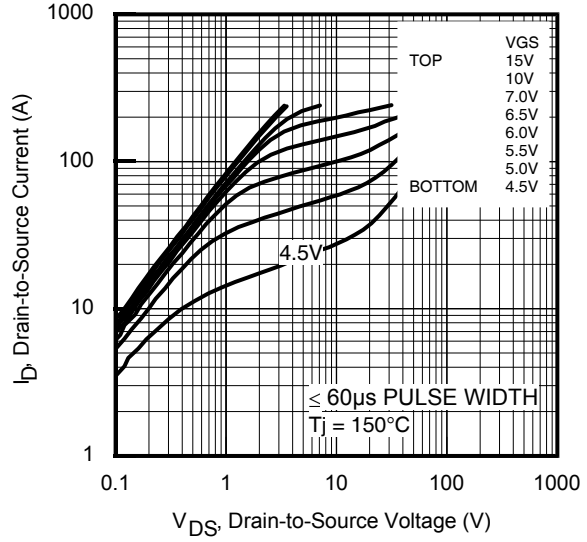
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	269	mJ
I <sub>AR</sub>	Avalanche Current ①	—	48	A

**Thermal Resistance**

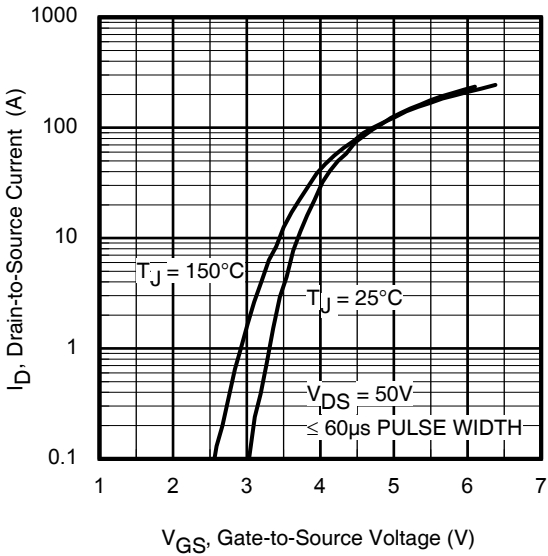
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	1.2	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	22	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	35	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	20	



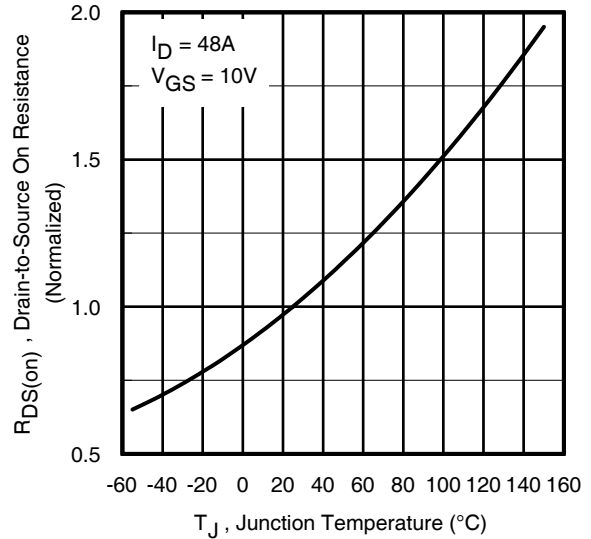
**Fig 1.** Typical Output Characteristics



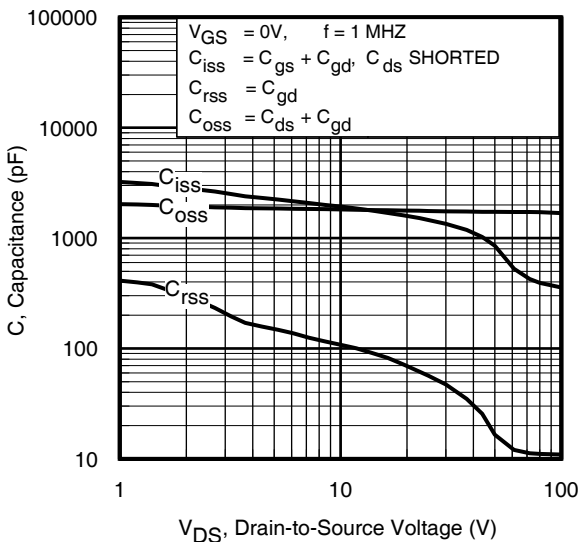
**Fig 2.** Typical Output Characteristics



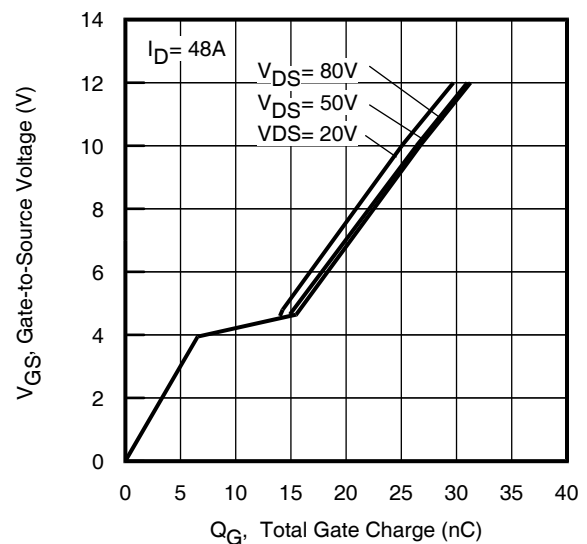
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance vs. Temperature



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

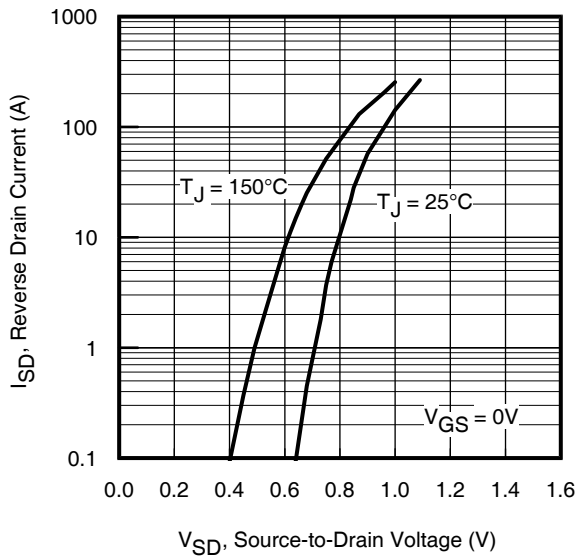


Fig 7. Typical Source-Drain Diode Forward Voltage

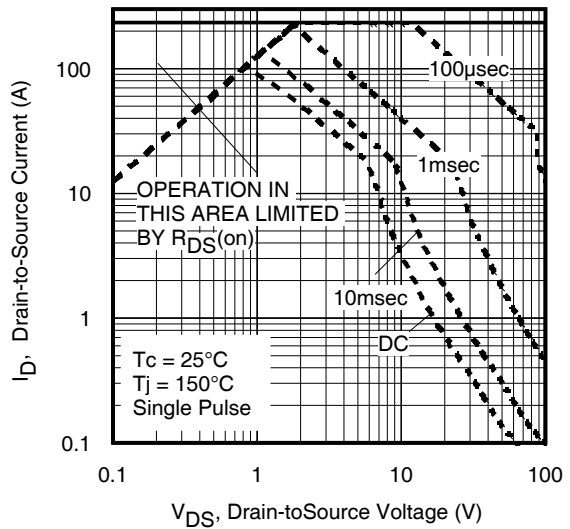


Fig 8. Maximum Safe Operating Area

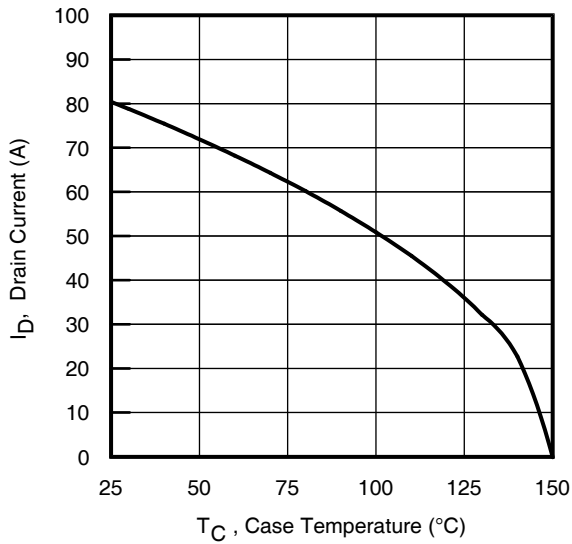


Fig 9. Maximum Drain Current vs. Case Temperature

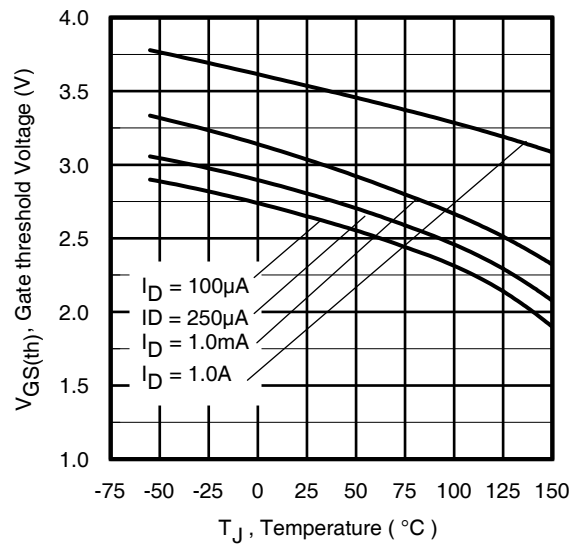


Fig 10. Threshold Voltage vs. Temperature

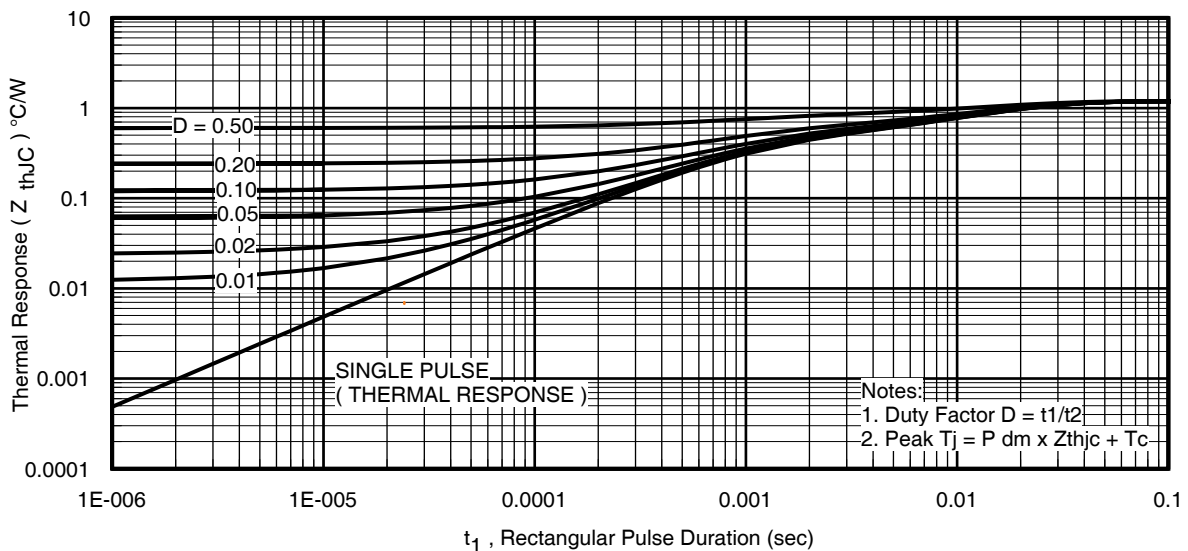


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

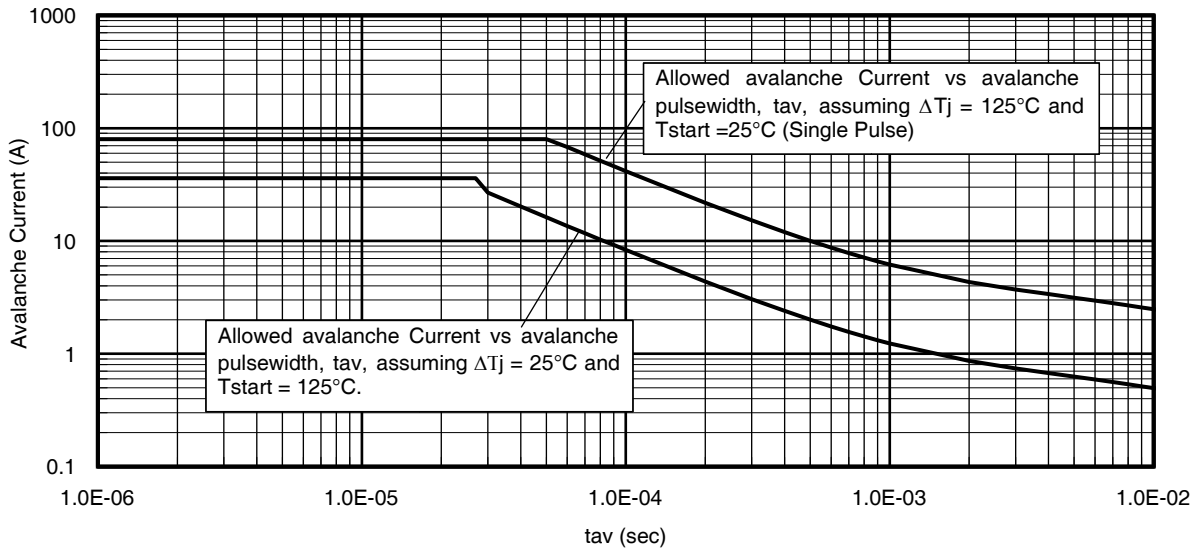


Fig 12. Typical Avalanche Current vs. Pulse Width

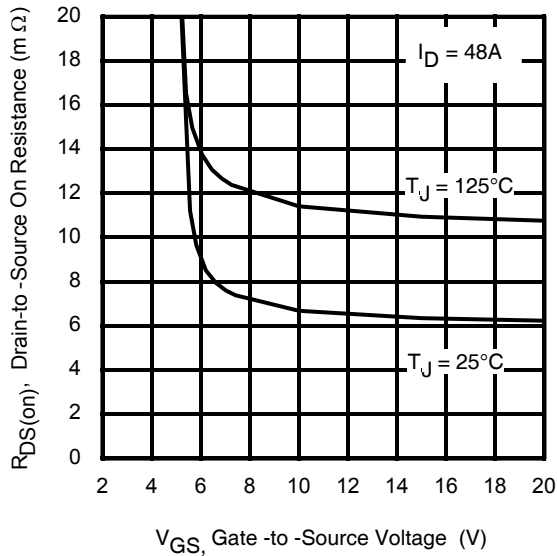


Fig 13. On-Resistance vs. Gate Voltage

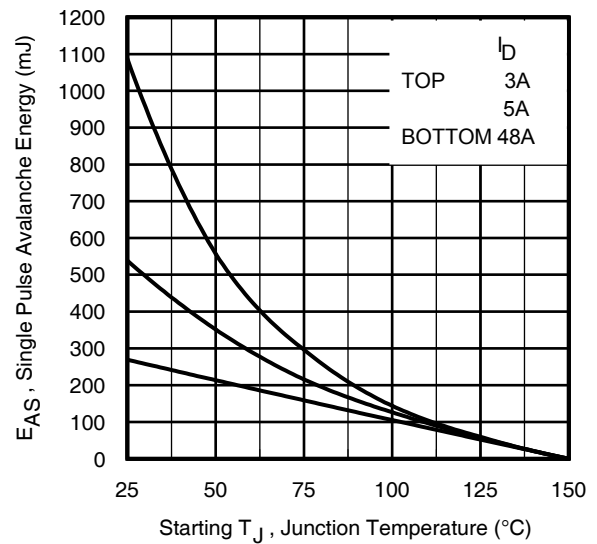
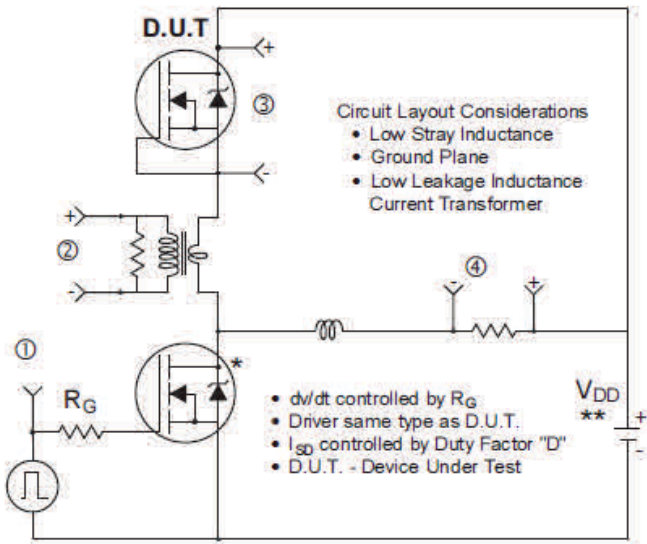
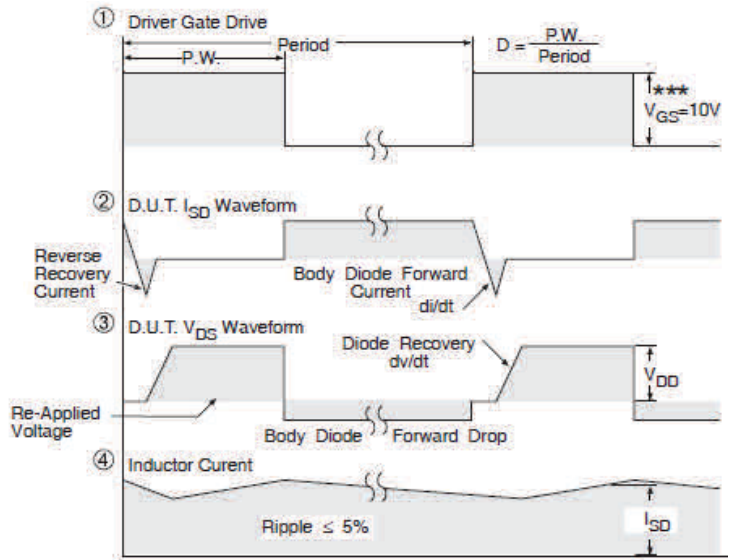


Fig 14. Maximum Avalanche Energy vs. Drain Current

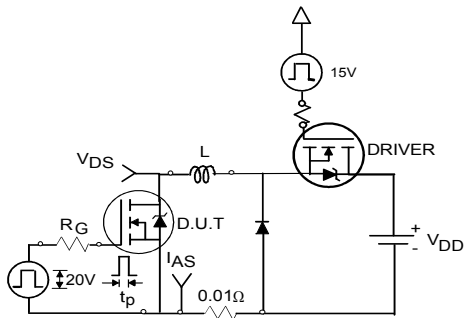


\* Use P-Channel Driver for P-Channel Measurements  
 \*\* Reverse Polarity for P-Channel

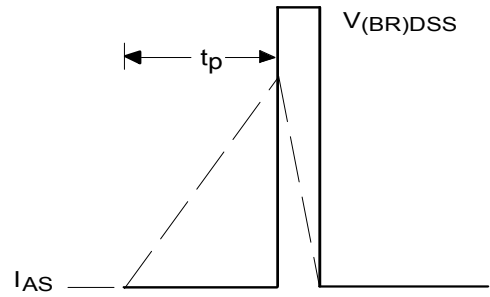


\*\*\*  $V_{GS} = 5V$  for Logic Level Devices

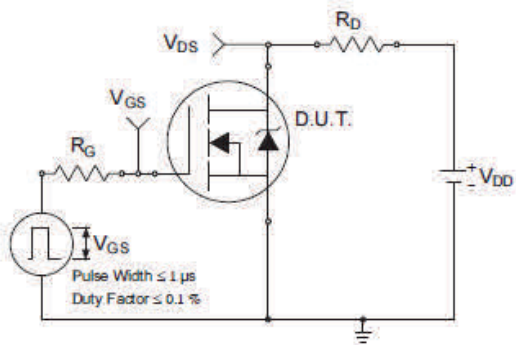
**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



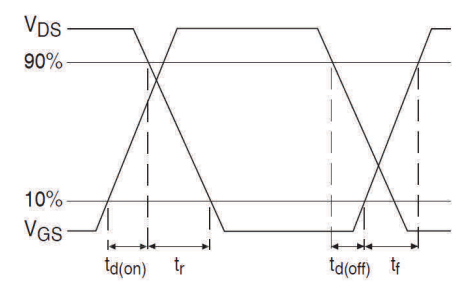
**Fig 16a. Unclamped Inductive Test Circuit**



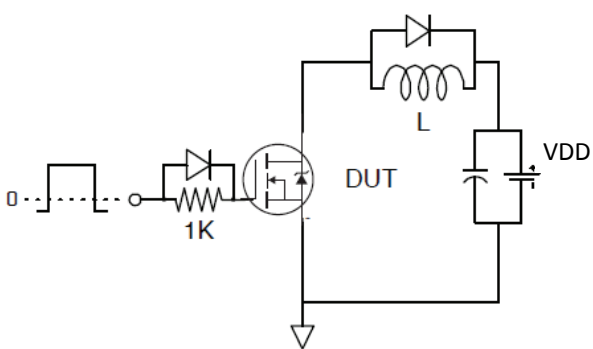
**Fig 16b. Unclamped Inductive Waveforms**



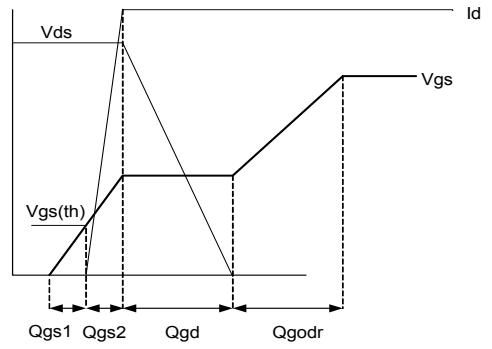
**Fig 17a. Switching Time Test Circuit**



**Fig 17b. Switching Time Waveforms**

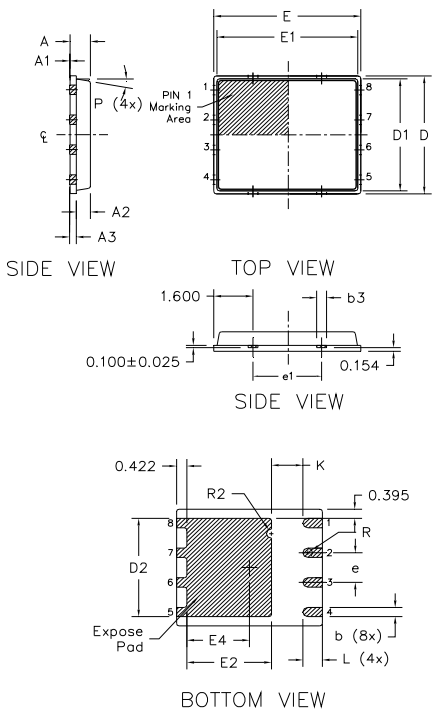


**Fig 18. Gate Charge Test Circuit**



**Fig 19. Gate Charge Waveform**

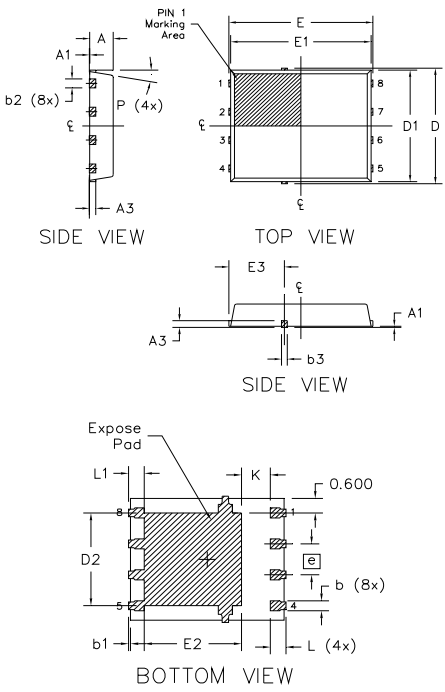
## PQFN 5x6 Outline "B" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

- Note:**
1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
  2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
  3. Coplanarity applies to the expose Heat Slug as well as the terminal
  4. Radius on terminal is Optional

## PQFN 5x6 Outline "G" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254 REF		0.0100 REF	
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150 BSC		0.2028 BSC	
D1	5.000 BSC		0.1969 BSC	
D2	3.700	3.900	0.1457	0.1535
E	6.150 BSC		0.2421 BSC	
E1	6.000 BSC		0.2362 BSC	
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27 REF		0.050 REF	
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

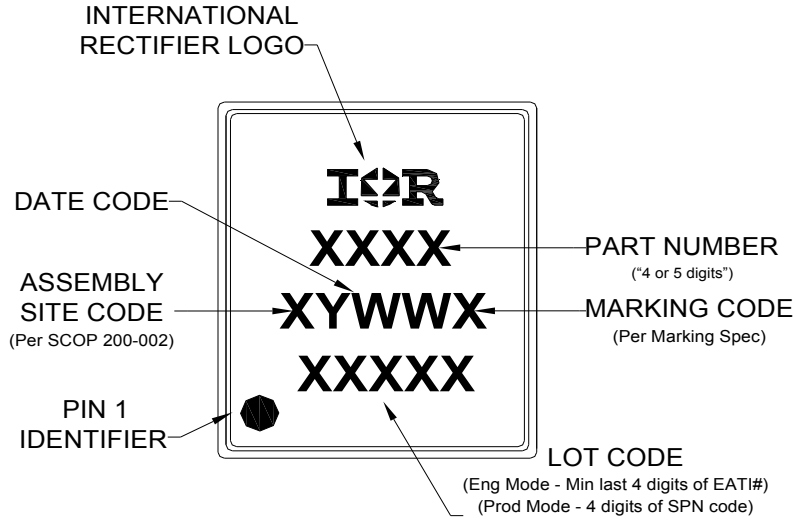
- Note:**
1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
  2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
  3. Coplanarity applies to the expose Heat Slug as well as the terminal
  4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.infineon.com/technical-info/appnotes/an-1136.pdf>  
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.infineon.com/technical-info/appnotes/an-1154.pdf>

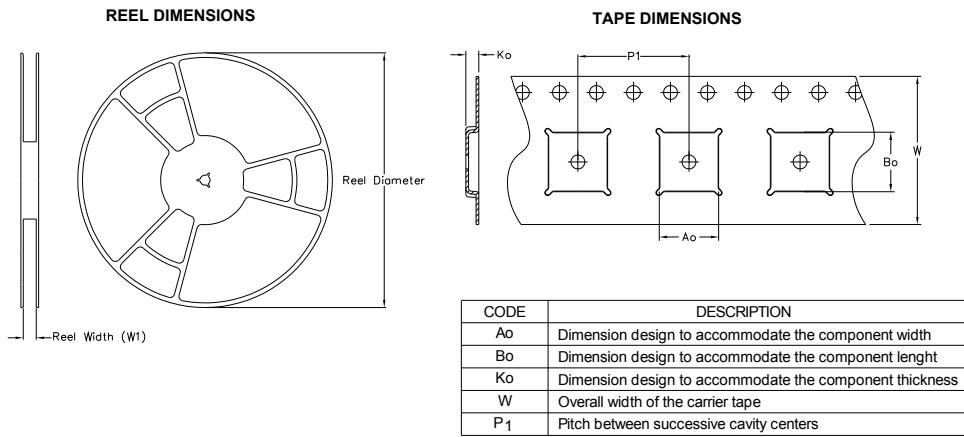
Note: For the most current drawing please refer to IR website at <http://www.infineon.com/package/>



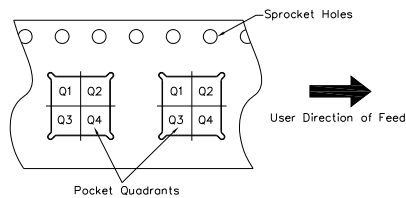
PQFN 5x6 Outline Part Marking



PQFN 5x6 Outline Tape and Reel



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at <http://www.infineon.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F <sup>††</sup> guidelines)	
<b>Moisture Sensitivity Level</b>	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.infineon.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.23\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 48\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.infineon.com/technical-info/appnotes/an-994.pdf>

**Revision History**

<b>Date</b>	<b>Comments</b>
01/24/2017	<ul style="list-style-type: none"> <li>• Changed datasheet with Infineon logo - all pages</li> <li>• Updated package outline for "option B" and added package outline for "option G" on page 7.</li> <li>• Added disclaimer on last page</li> </ul>

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