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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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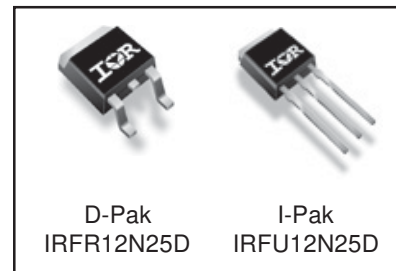
**Applications**

- High frequency DC-DC converters
- Lead-Free

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
250V	0.26Ω	14A

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	14	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	9.7	
$I_{DM}$	Pulsed Drain Current ①	56	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	9.3	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.04	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ⑤ are on page 10

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.26	$\Omega$	$V_{GS} = 10V, I_D = 8.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

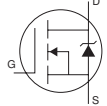
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	6.8	—	—	S	$V_{DS} = 25V, I_D = 8.4A$
$Q_g$	Total Gate Charge	—	23	35	nC	$I_D = 8.4A$
$Q_{gs}$	Gate-to-Source Charge	—	5.8	8.7		$V_{DS} = 200V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	12	19		$V_{GS} = 10V, \text{④}$
$t_{d(on)}$	Turn-On Delay Time	—	9.1	—	ns	$V_{DD} = 125V$
$t_r$	Rise Time	—	25	—		$I_D = 8.4A$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G = 6.8\Omega$
$t_f$	Fall Time	—	9.2	—		$V_{GS} = 10V, \text{④}$
$C_{iss}$	Input Capacitance	—	810	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	130	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	22	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1100	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	50	—		$V_{GS} = 0V, V_{DS} = 200V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	130	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 200V, \text{⑤}$

## Avalanche Characteristics

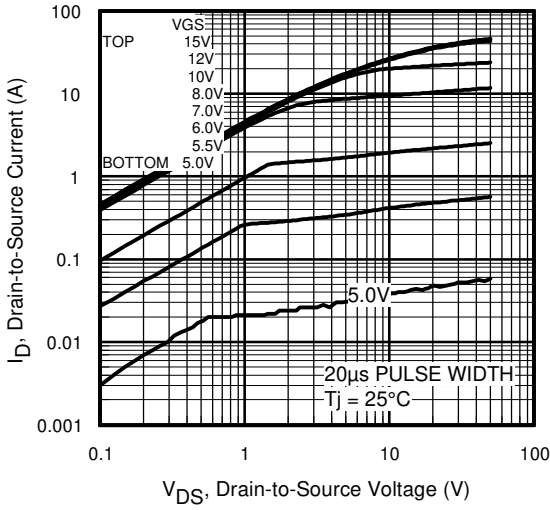
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	250	mJ
$I_{AR}$	Avalanche Current①	—	8.4	A
$E_{AR}$	Repetitive Avalanche Energy①	—	14	mJ

## Diode Characteristics

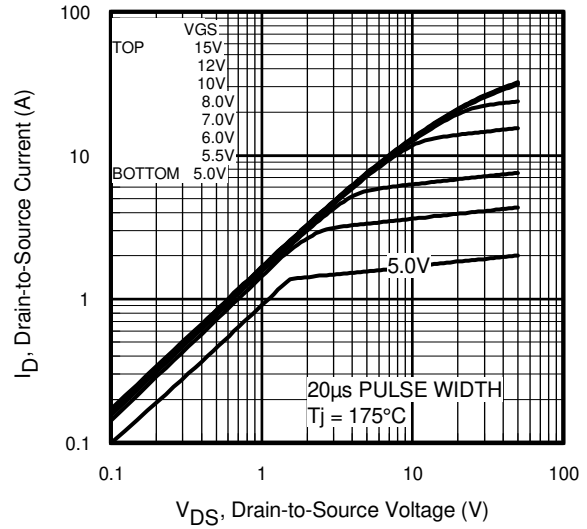
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	56		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 8.4A, V_{GS} = 0V, \text{④}$
$t_{rr}$	Reverse Recovery Time	—	140	—	ns	$T_J = 25^\circ\text{C}, I_F = 8.4A$
$Q_{rr}$	Reverse Recovery Charge	—	710	—	nC	$di/dt = 100A/\mu s, \text{④}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				



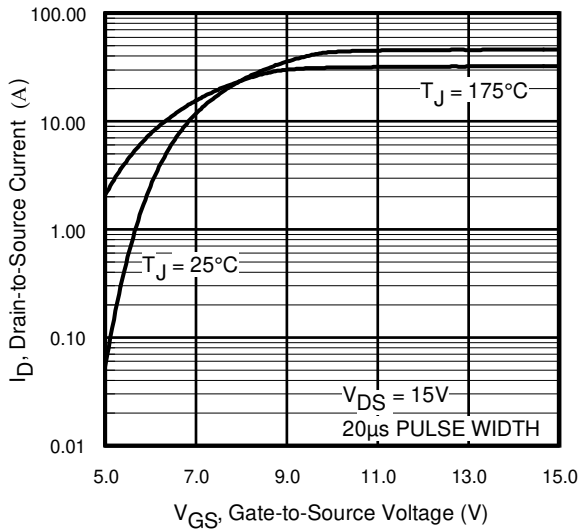
# IRFR/U12N25DPbF



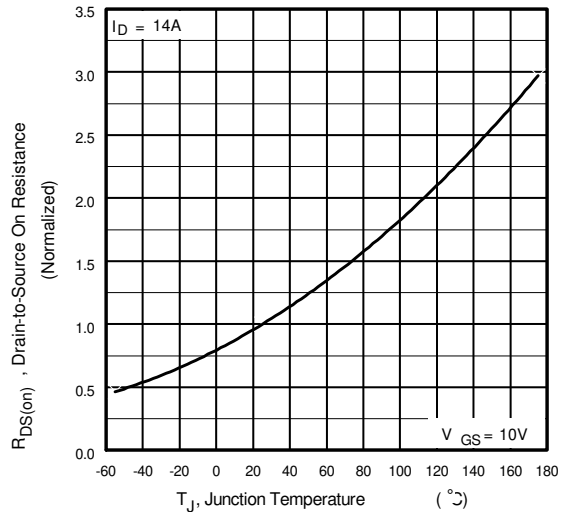
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

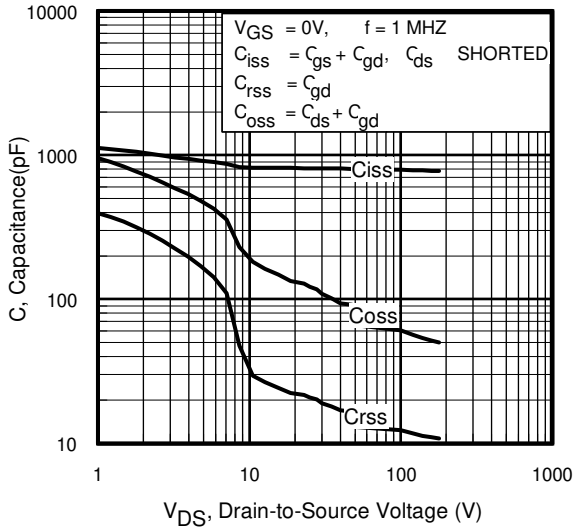


**Fig 3.** Typical Transfer Characteristics

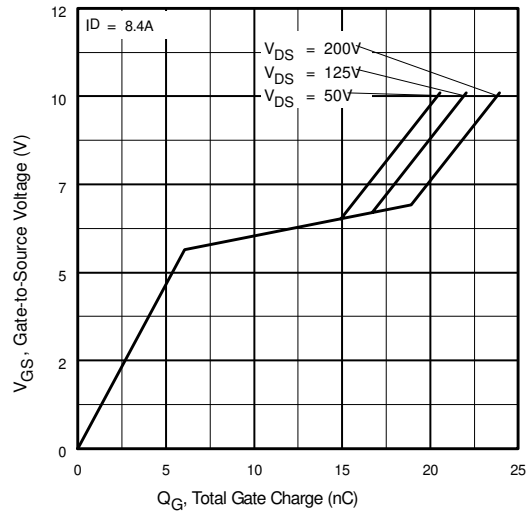


**Fig 4.** Normalized On-Resistance Vs. Temperature

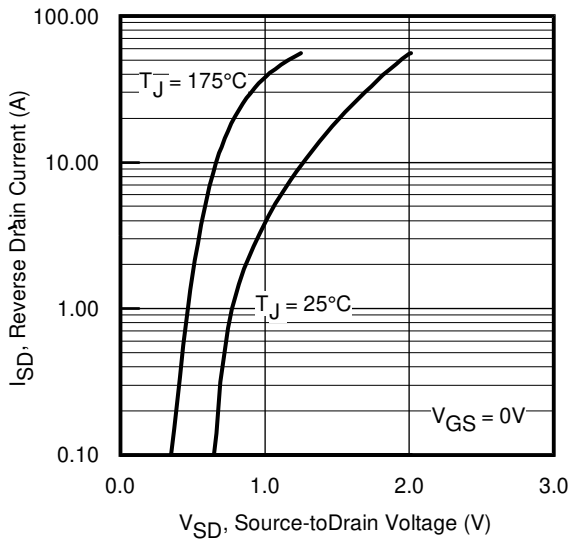
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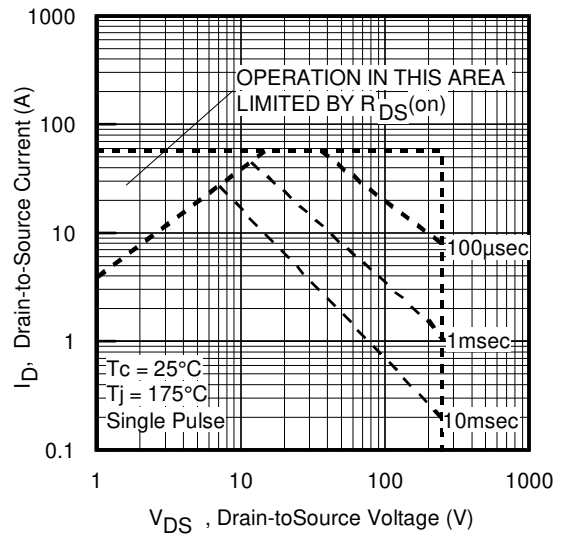
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



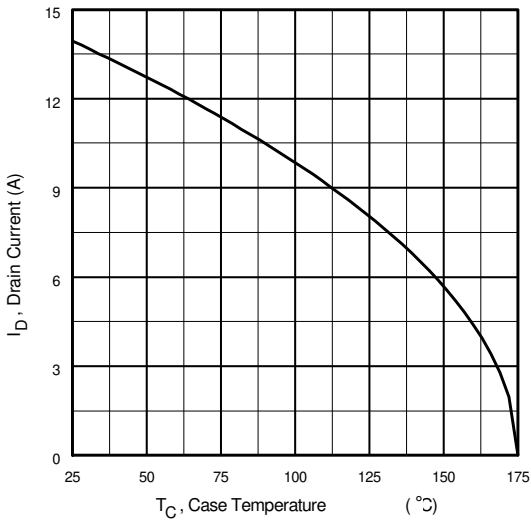
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



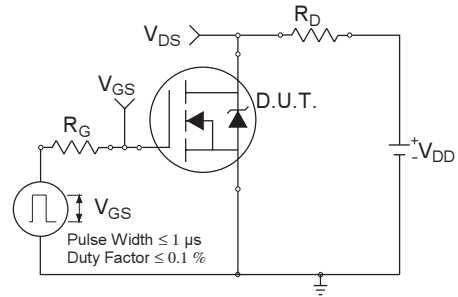
**Fig 7.** Typical Source-Drain Diode Forward Voltage



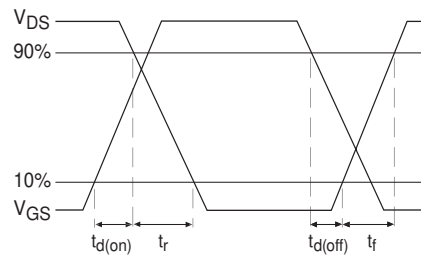
**Fig 8.** Maximum Safe Operating Area



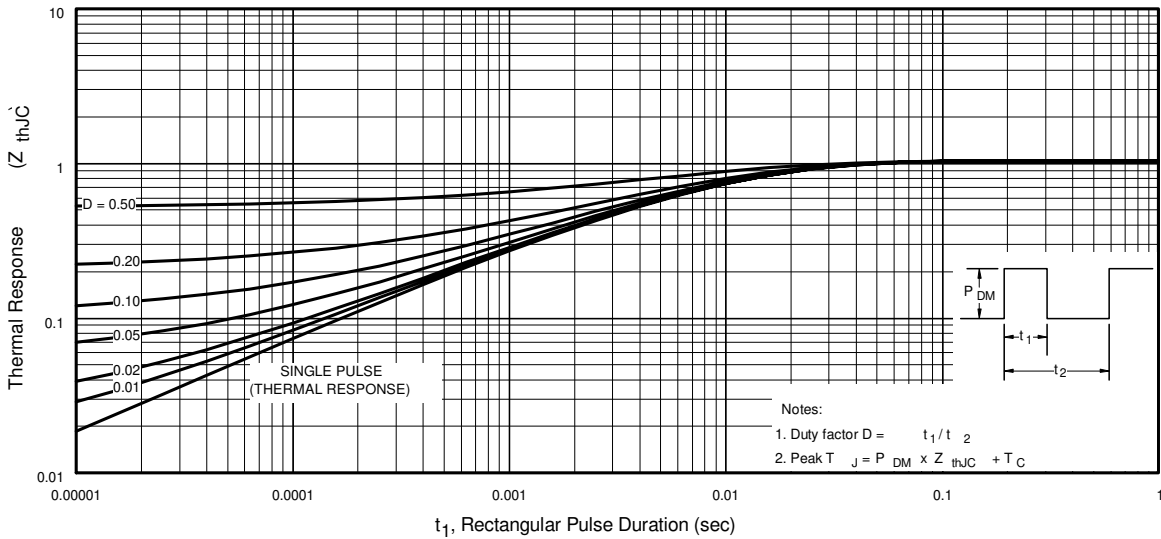
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

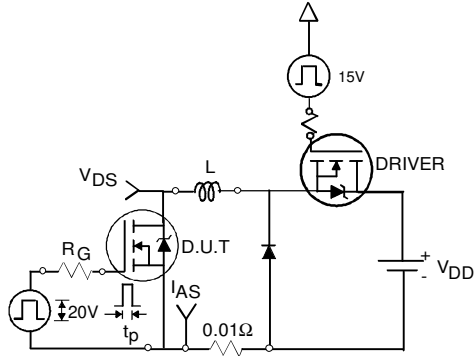


**Fig 10b.** Switching Time Waveforms

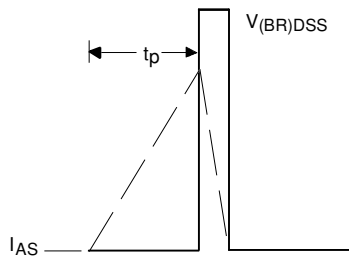


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

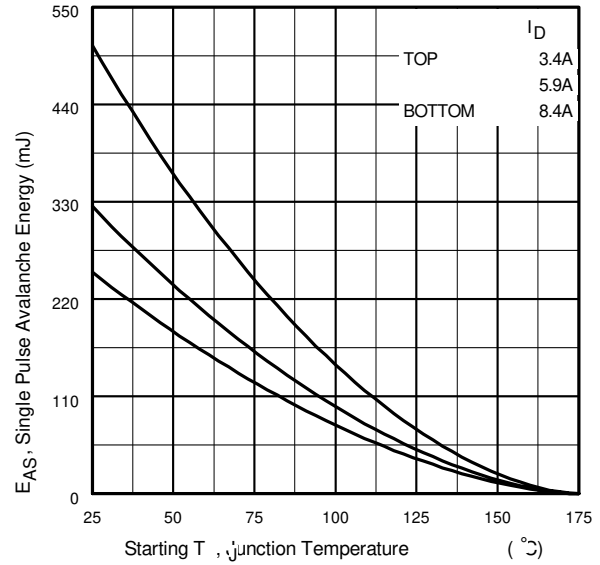
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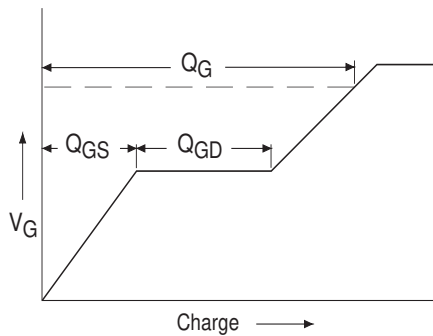
**Fig 12a.** Unclamped Inductive Test Circuit



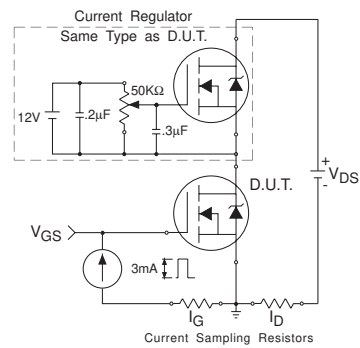
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

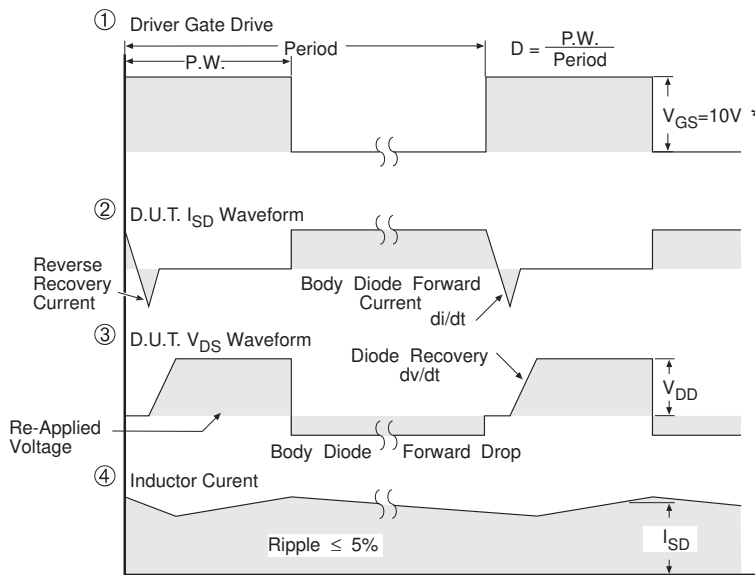
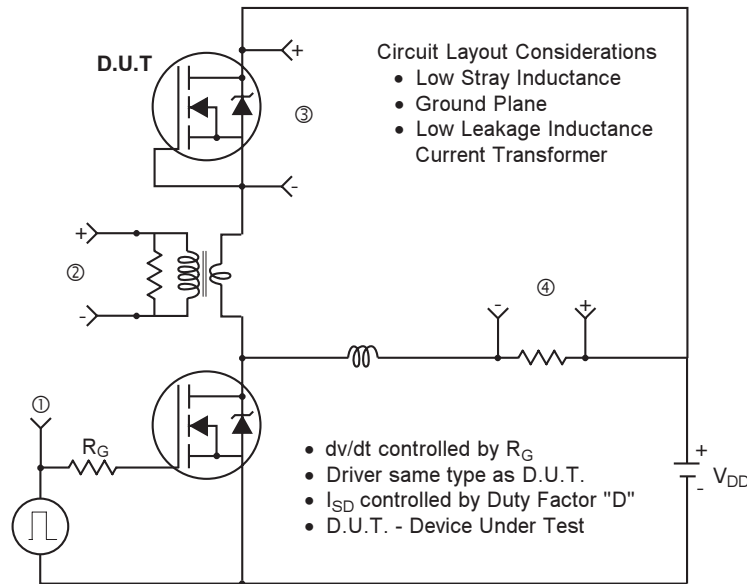


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

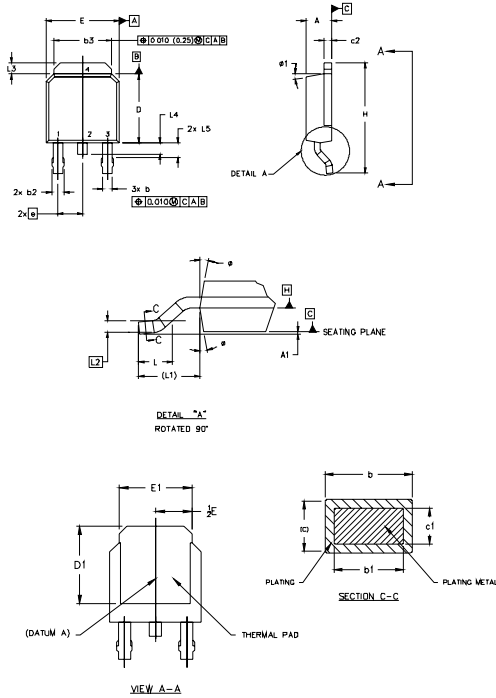
**Fig 14.** For N-Channel HEXFET® Power MOSFETs



# IRFR/U12N25DPbF



## D-Pak (TO-252AA) Package Outline



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.75	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ϕ	0"	10"	0"	10"	
ϕ1	0"	15"	0"	15"	

**LEAD ASSIGNMENTS**

- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

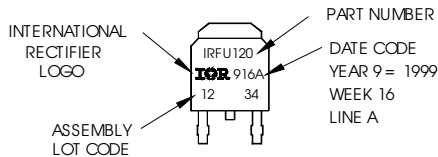
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

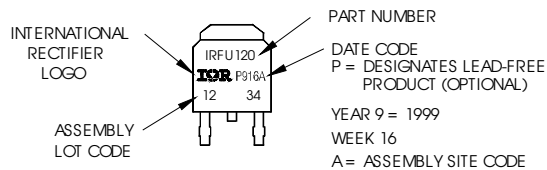
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE 'A'

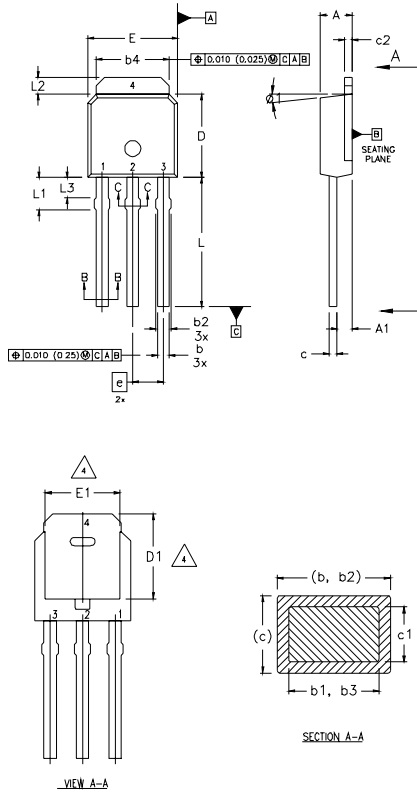
Note: "P" in assembly line position  
indicates "Lead-Free"



OR



## I-Pak (TO-251AA) Package Outline



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

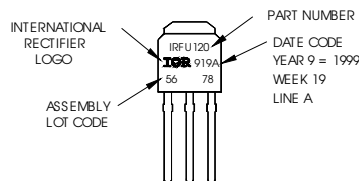
LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

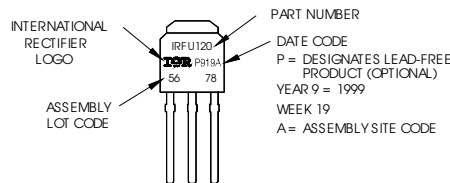
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"  
**Note:** 'P' in assembly line  
position indicates "Lead-Free"



OR

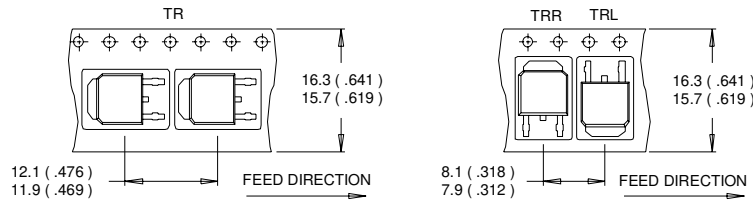


# IRFR/U12N25DPbF

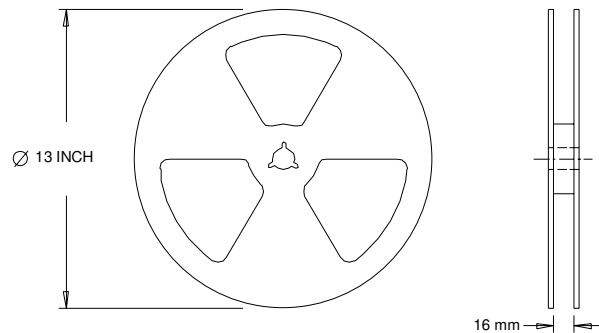
International  
**IR** Rectifier

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
  - ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 7.1\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 8.4\text{A}$ .
  - ③  $I_{SD} \leq 8.4\text{A}$ ,  $di/dt \leq 150\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
  - ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- \* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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[www.irf.com](http://www.irf.com)

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>