Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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International
IOR Rectifier

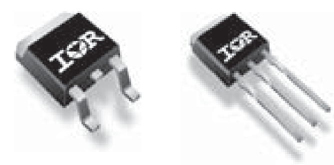
PD- 94061B

SMPS MOSFET

IRFR3711
IRFU3711

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	I_D
20V	**6.5mΩ**	**110A④**



D-Pak IRFR3711   I-Pak IRFU3711

Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Server Processor Power Synchronous FET
- Optimized for Synchronous Buck Converters Including Capacitive Induced Turn-on Immunity
- 100% R_G Tested

Benefits

- Ultra-Low Gate Impedance
- Very Low RDS(on) at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current

Absolute Maximum Ratings

Symbol	Parameter	Max	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	100 ④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	69 ④	
I_{DM}	Pulsed Drain Current ①	440	
P_D @T_A = 25°C	Maximum Power Dissipation ⑤	2.5	W
P_D @T_C = 25°C	Maximum Power Dissipation	120	
	Linear Derating Factor	0.96	W/°C
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	1.04	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤⑥	—	50	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	110	

Notes ① through ⑥ are on page 10

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.2	6.5	mΩ	V_{GS} = 10V, I_D = 15A ③
		—	6.7	8.5		V_{GS} = 4.5V, I_D = 12A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	140	µA	V_{DS} = 20V, V_{GS} = 0V
		—	—	20		V_{DS} = 16V, V_{GS} = 0V
		—	—	100		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V

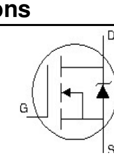
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
g_{fs}	Forward Transconductance	53	—	—	S	V_{DS} = 16V, I_D = 30A
Q_g	Total Gate Charge	—	29	44	nC	I_D = 15A
Q_{gs}	Gate-to-Source Charge	—	7.3	—		V_{DS} = 10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.9	—		V_{GS} = 4.5V ③
Q_{oss}	Output Gate Charge	—	33	—		V_{GS} = 0V, V_{DS} = 10V
R_G	Gate Resistance	0.3	—	2.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 10V
t_r	Rise Time	—	220	—		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		R_G = 1.8Ω
t_f	Fall Time	—	12	—		V_{GS} = 4.5V ③
C_{iss}	Input Capacitance	—	2980	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1770	—		V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	—	280	—		f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ	Max	Units
E_{AS}	Single Pulse Avalanche Energy②	—	460	mJ
I_{AR}	Avalanche Current ①	—	30	A

Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110 ④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	440		
V_{SD}	Diode Forward Voltage	—	0.88	1.3	V	T_J = 25°C, I_S = 30A, V_{GS} = 0V ③
		—	0.82	—		T_J = 125°C, I_S = 30A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	50	75	ns	T_J = 25°C, I_F = 16A, V_R = 10V
Q_{rr}	Reverse Recovery Charge	—	61	92	nC	di/dt = 100A/µs ③
t_{rr}	Reverse Recovery Time	—	48	72	ns	T_J = 125°C, I_F = 16A, V_R = 10V
Q_{rr}	Reverse Recovery Charge	—	65	98	nC	di/dt = 100A/µs ③

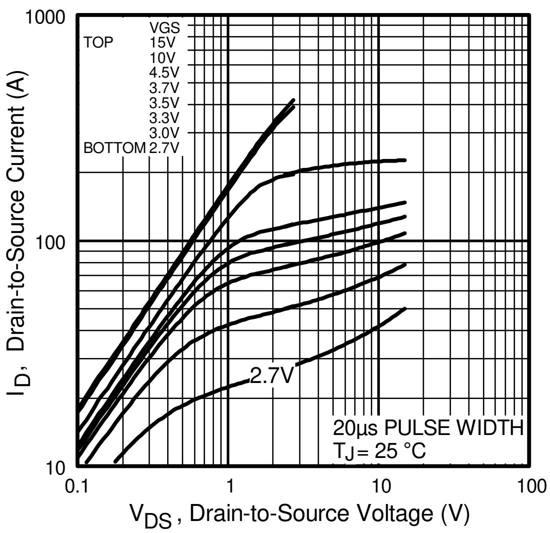


Fig 1. Typical Output Characteristics

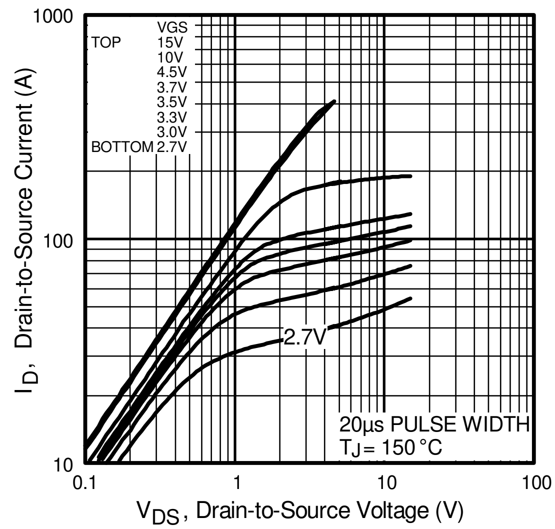


Fig 2. Typical Output Characteristics

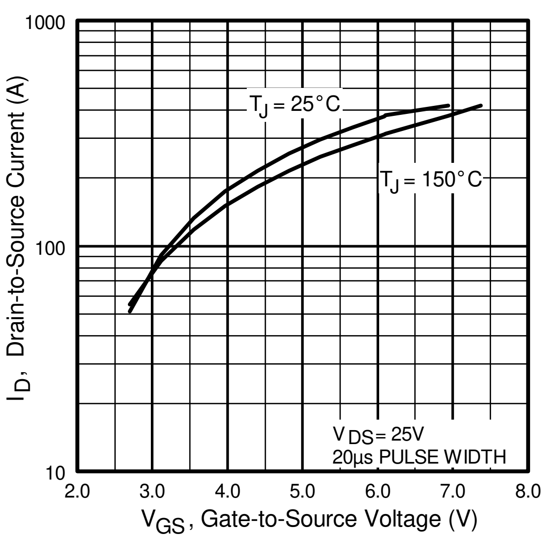


Fig 3. Typical Transfer Characteristics

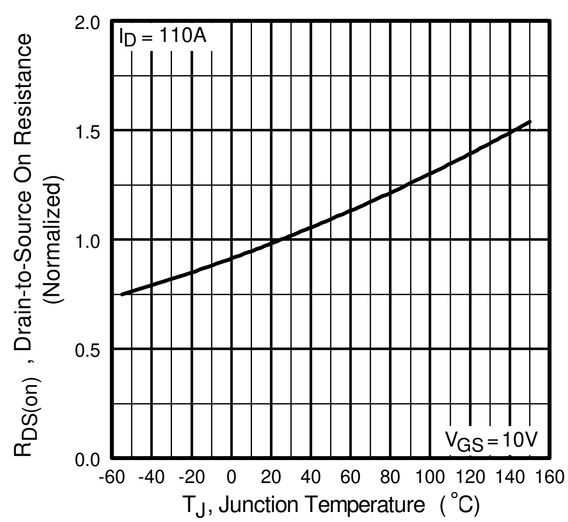


Fig 4. Normalized On-Resistance
Vs. Temperature

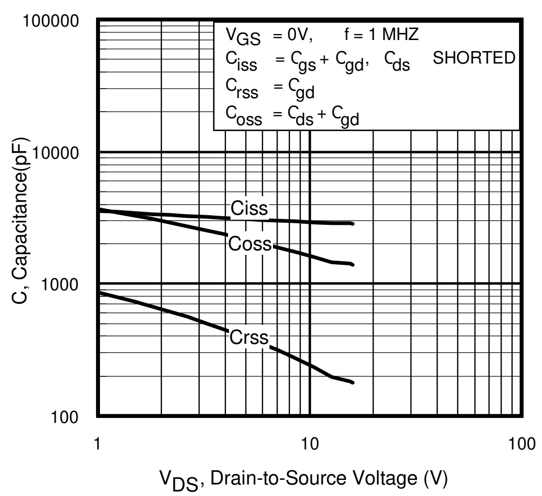


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

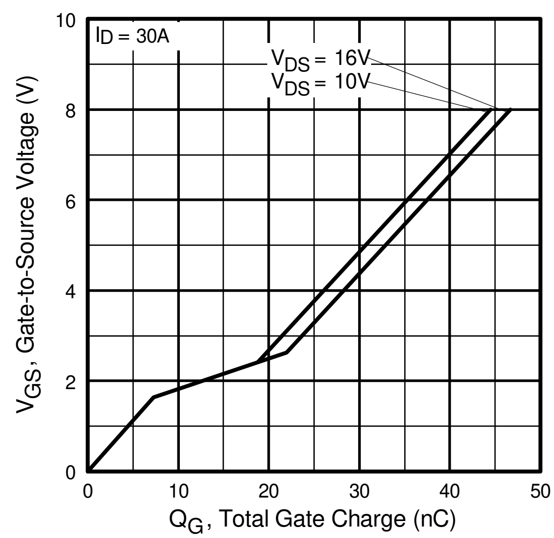


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

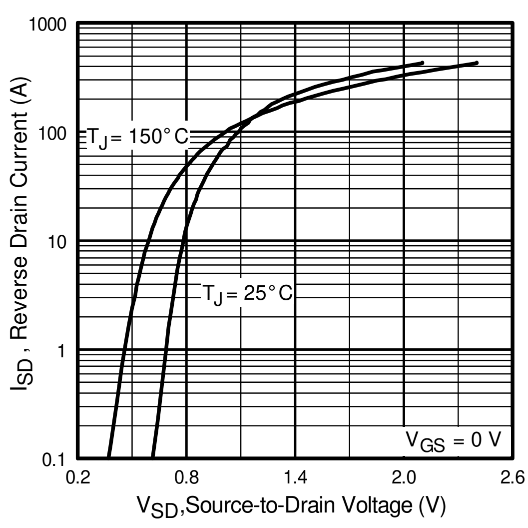


Fig 7. Typical Source-Drain Diode Forward Voltage

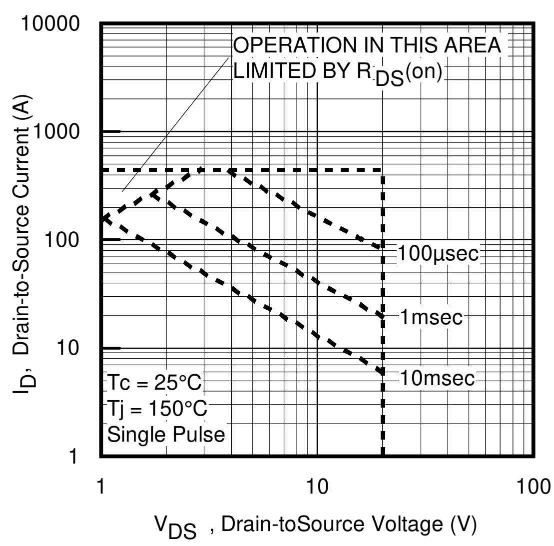


Fig 8. Maximum Safe Operating Area

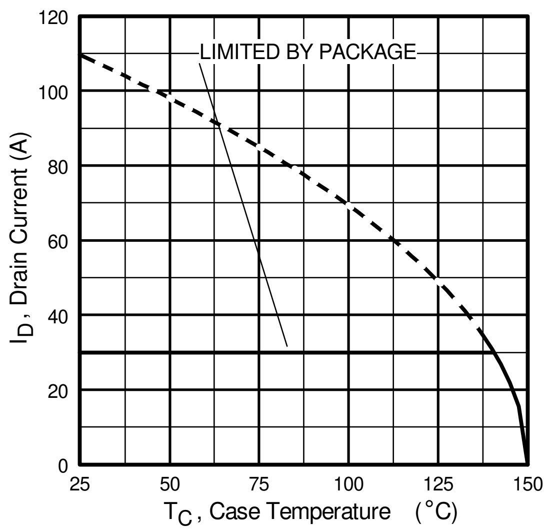


Fig 9. Maximum Drain Current Vs. Case Temperature

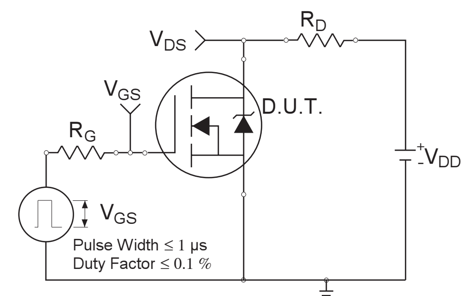


Fig 10a. Switching Time Test Circuit

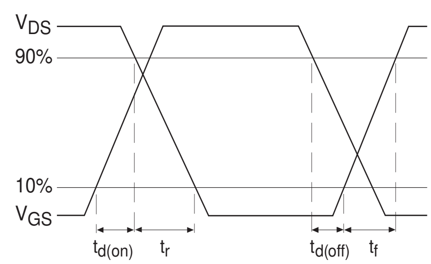


Fig 10b. Switching Time Waveforms

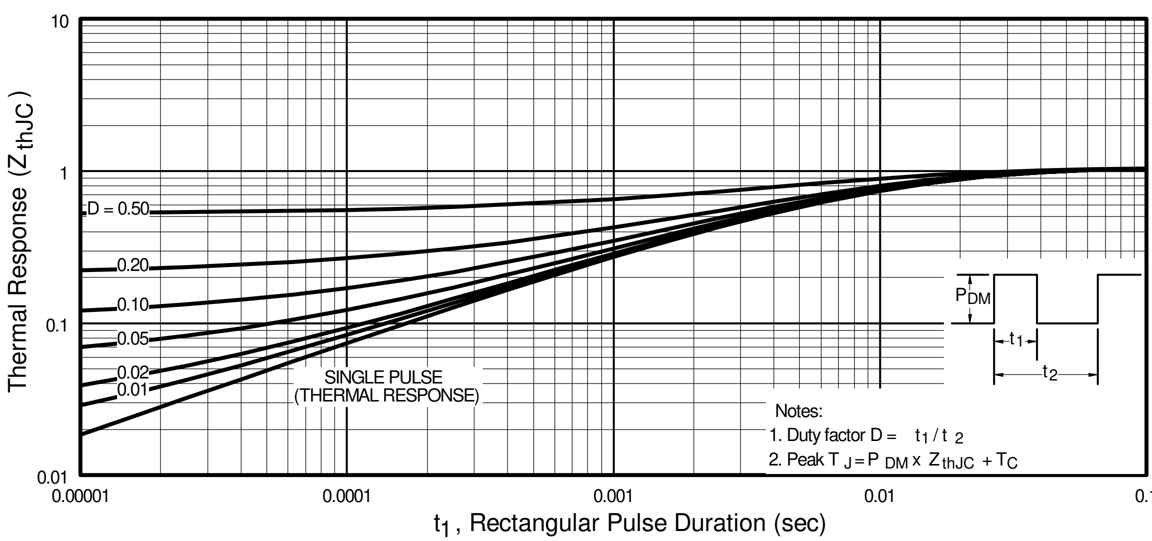


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

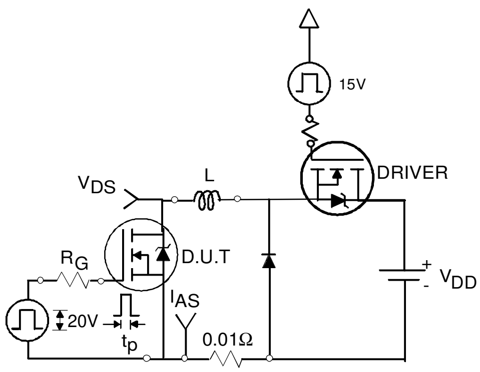


Fig 12a. Unclamped Inductive Test Circuit

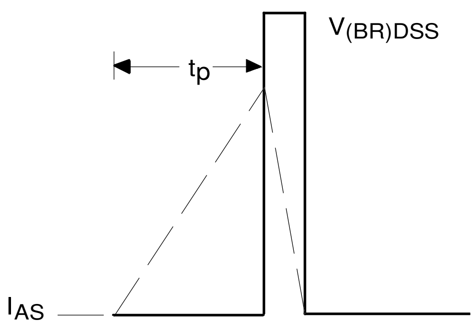


Fig 12b. Unclamped Inductive Waveforms

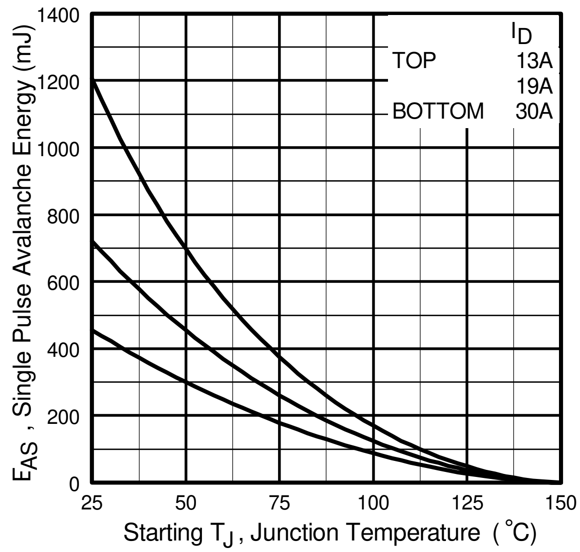


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

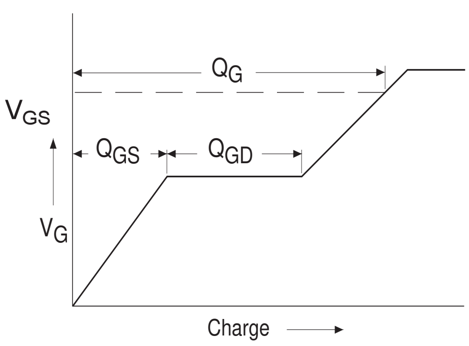


Fig 13a. Basic Gate Charge Waveform

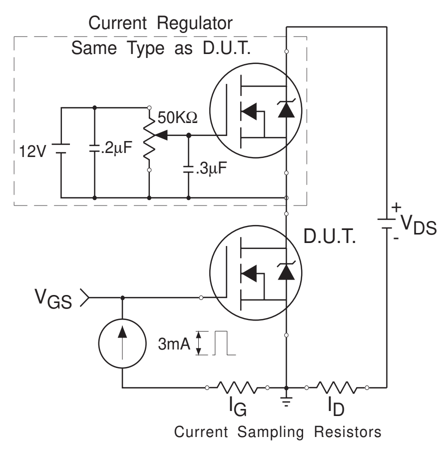
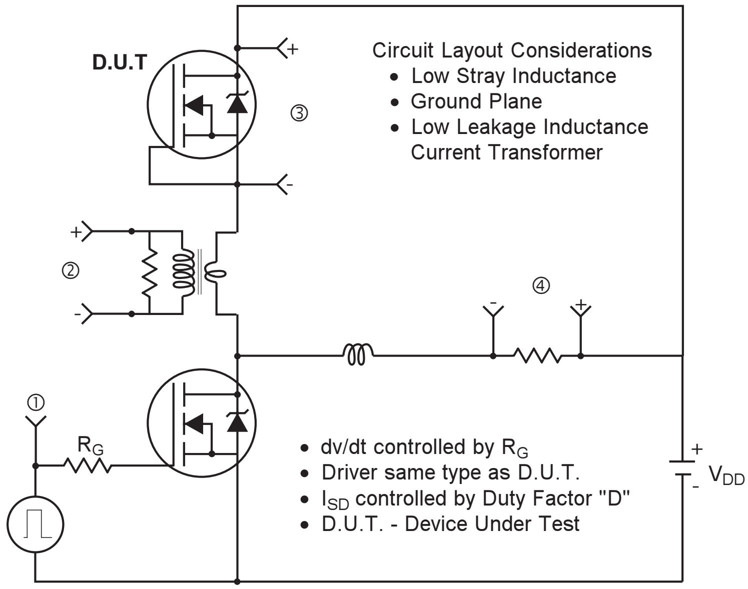
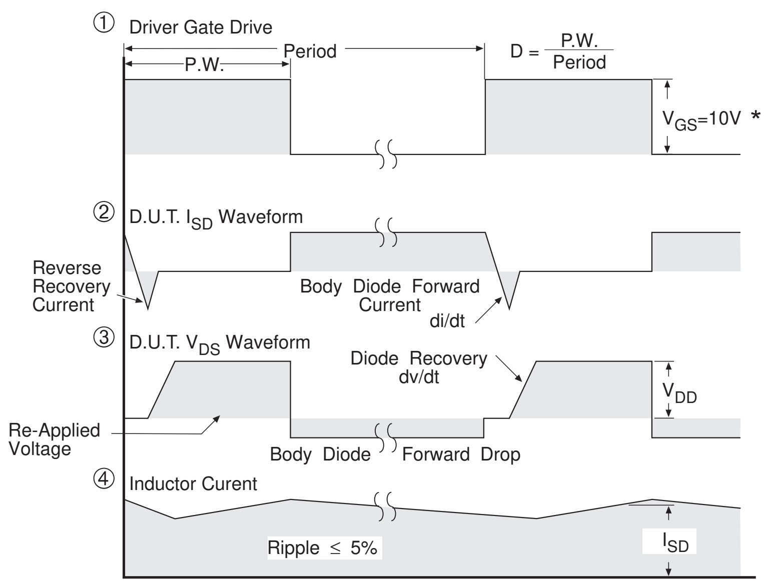


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



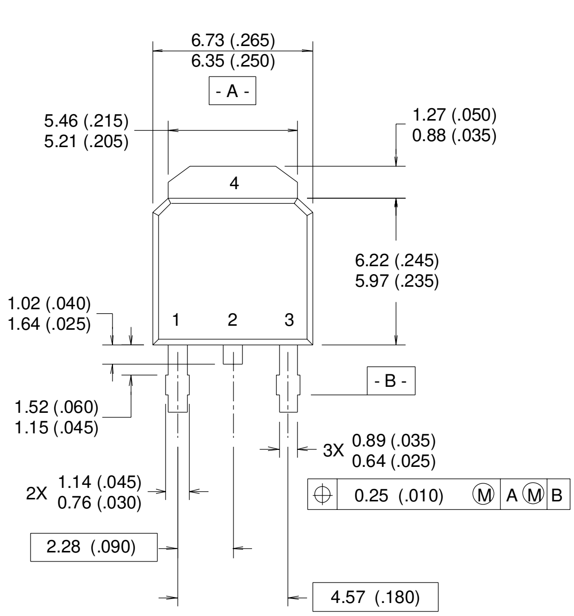


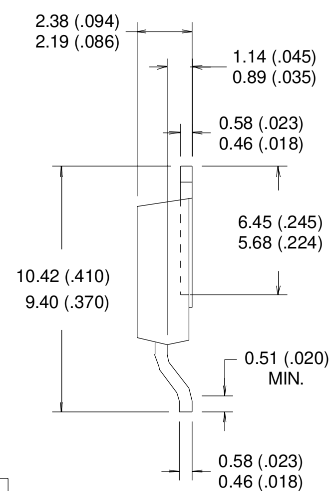
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)





LEAD ASSIGNMENTS

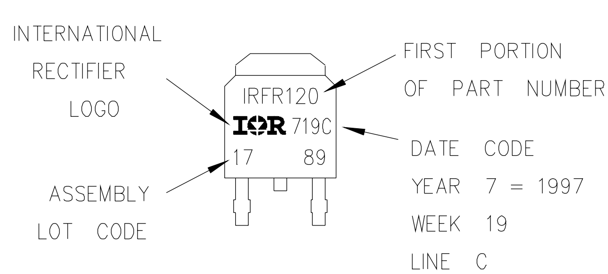
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

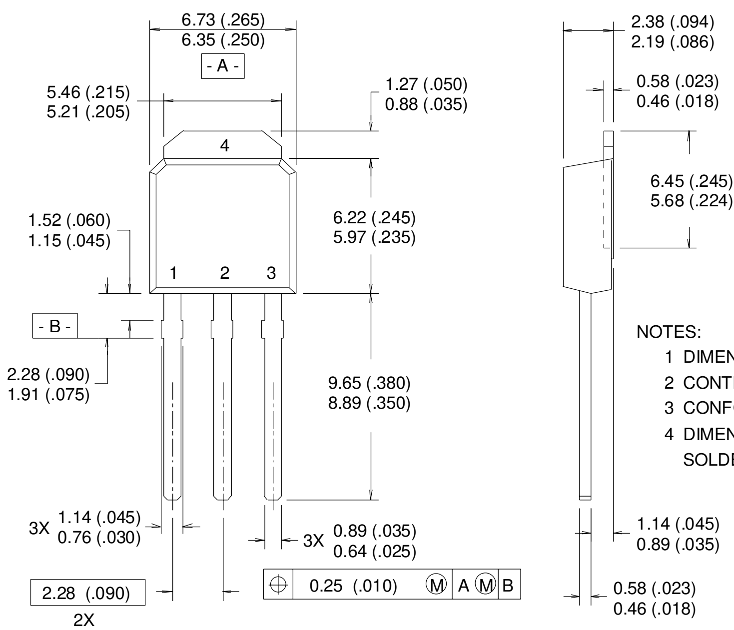
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

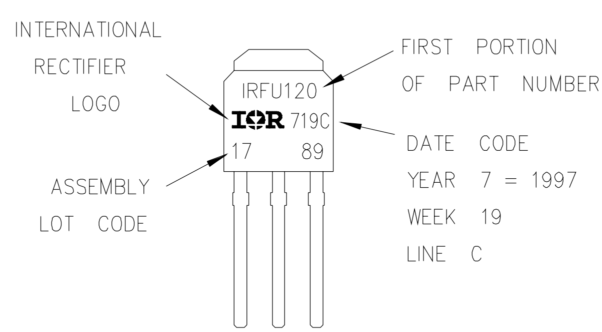


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

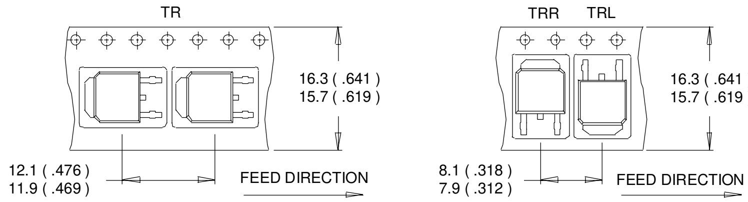
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

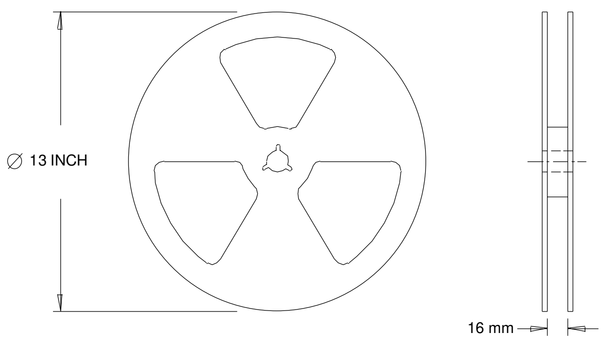


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.0mH R_G = 25Ω, I_{AS} = 30A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994

⑥ R_θ is measured at T_J approximately at 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
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TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 1/04

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/