Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

International IƏR Rectifier

IRFR3711ZPbF
# IRFU3711ZPbF

Applications

- High Frequency Synchronous Buck
  Converters for Computer Processor Power
- High Frequency Isolated DC-DC
  Converters with Synchronous Rectification
  for Telecom and Industrial Use
- Lead-Free

Benefits

- Very Low RDS(on) at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage
  and Current

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Qg
20V	5.7mΩ	18nC

D-Pak
IRFR3711Z

I-Pak
IRFU3711Z
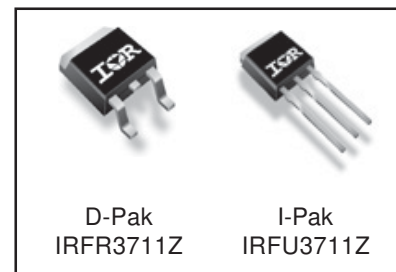
Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	93④	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	66④	A
I_{DM}	Pulsed Drain Current ①	370	
P_D @T_C = 25°C	Maximum Power Dissipation ⑤	79	W
P_D @T_C = 100°C	Maximum Power Dissipation ⑤	39	
	Linear Derating Factor	0.53	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.9	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	——	50	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Notes ① through ⑤ are on page 11

12/13/04

IRFR/U3711ZPbF

Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	13	——	mV/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.5	5.7	mΩ	V$_{GS}$ = 10V, I$_D$ = 15A ③
		——	6.2	7.8		V$_{GS}$ = 4.5V, I$_D$ = 12A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.55	2.0	2.45	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Coefficient	——	-5.4	——	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	1.0	µA	V$_{DS}$ = 16V, V$_{GS}$ = 0V
		——	——	150		V$_{DS}$ = 16V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V$_{GS}$ = -20V
gfs	Forward Transconductance	48	——	——	S	V$_{DS}$ = 10V, I$_D$ = 12A
Q$_g$	Total Gate Charge	——	18	27		
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	——	5.1	——		V$_{DS}$ = 10V
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	——	1.8	——	nC	V$_{GS}$ = 4.5V
Q$_{gd}$	Gate-to-Drain Charge	——	6.5	——		I$_D$ = 12A
Q$_{godr}$	Gate Charge Overdrive	——	4.6	——		See Fig. 16
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	——	8.3	——		
Q$_{oss}$	Output Charge	——	9.8	——	nC	V$_{DS}$ = 10V, V$_{GS}$ = 0V
t$_{d(on)}$	Turn-On Delay Time	——	12	——		V$_{DD}$ = 15V, V$_{GS}$ = 4.5V③
t$_r$	Rise Time	——	13	——		I$_D$ = 12A
t$_{d(off)}$	Turn-Off Delay Time	——	15	——	ns	Clamped Inductive Load
t$_f$	Fall Time	——	5.2	——		
C$_{iss}$	Input Capacitance	——	2160	——		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	700	——	pF	V$_{DS}$ = 10V
C$_{rss}$	Reverse Transfer Capacitance	——	360	——		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy②	——	140	mJ
I$_{AR}$	Avalanche Current ①	——	12	A
E$_{AR}$	Repetitive Avalanche Energy ①	——	7.9	mJ

Diode Characteristics

|	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	93④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	370		
V$_{SD}$	Diode Forward Voltage	——	——	1.0	V	T$_J$ = 25°C, I$_S$ = 12A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	19	28	ns	T$_J$ = 25°C, I$_F$ = 12A, V$_{DD}$ = 10V
Q$_{rr}$	Reverse Recovery Charge	——	9.4	14	nC	di/dt = 100A/µs ③
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

IRFR/U3711ZPbF
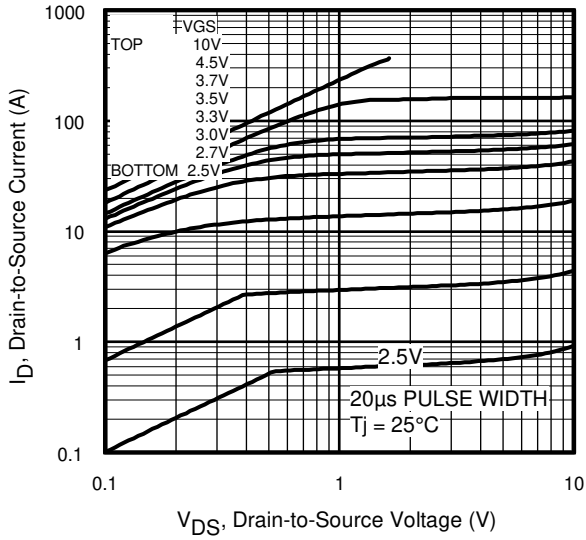
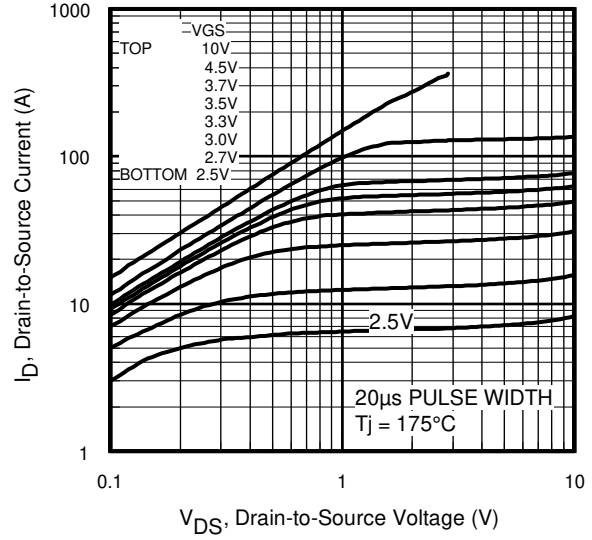**Fig 1.** Typical Output Characteristics

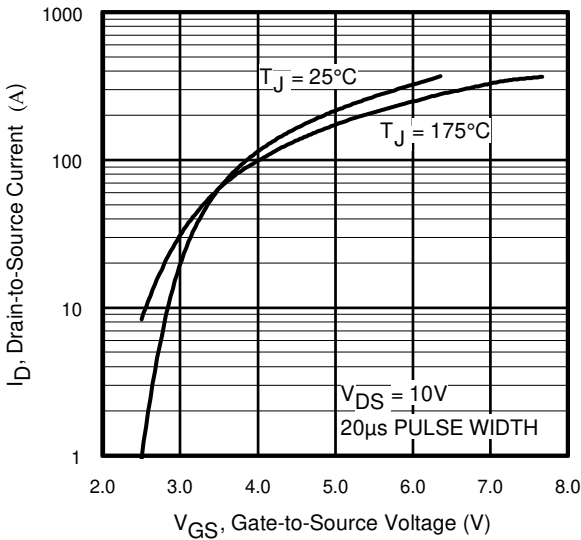**Fig 2.** Typical Output Characteristics

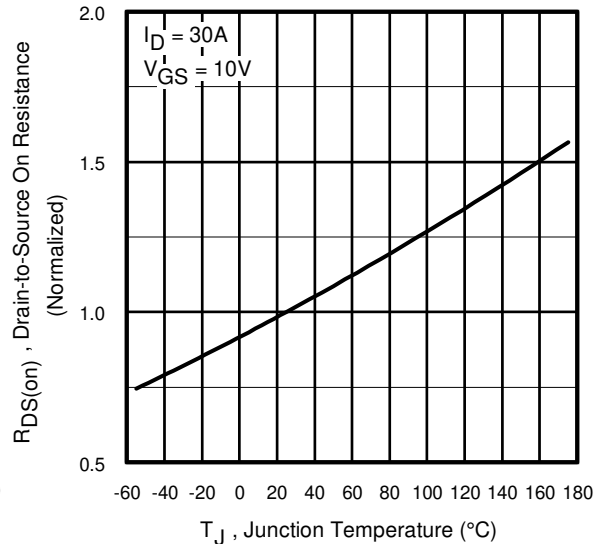**Fig 3.** Typical Transfer Characteristics

Fig 4. Normalized On-Resistance
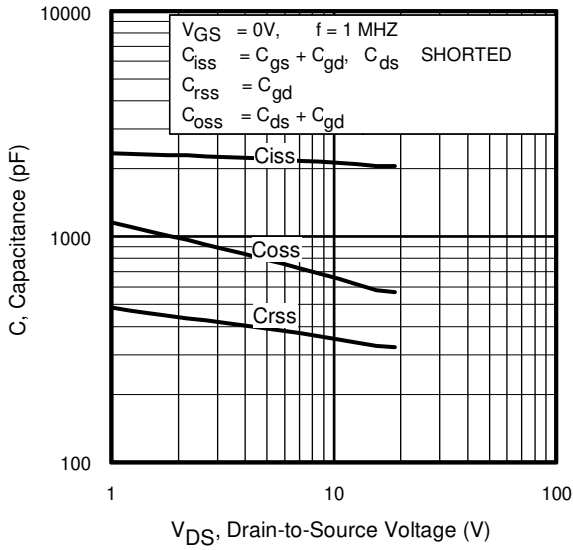vs. Temperature

IRFR/U3711ZPbF

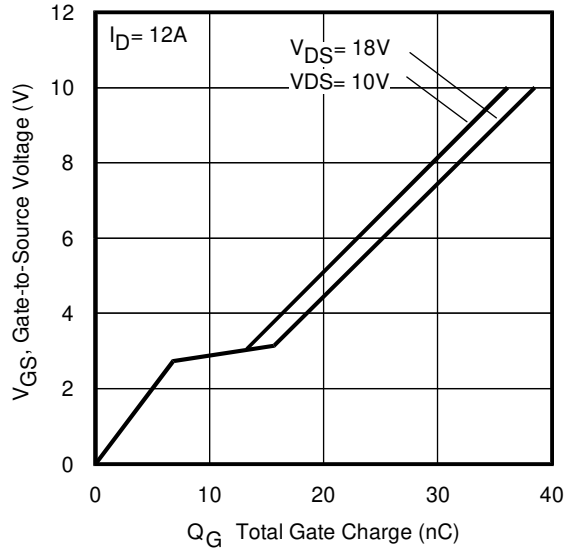Fig 5. Typical Capacitance vs.
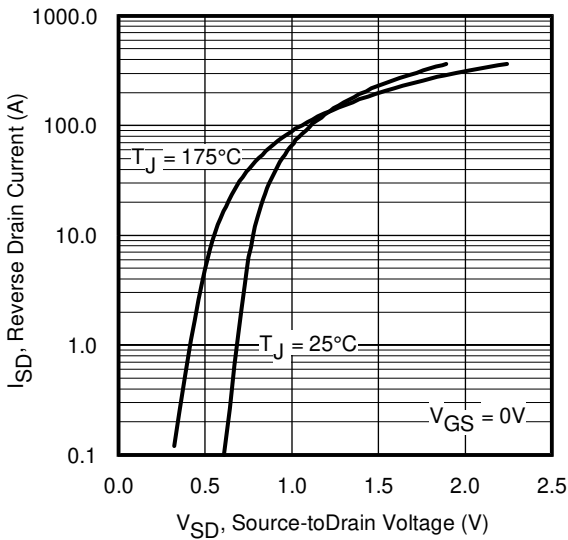Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

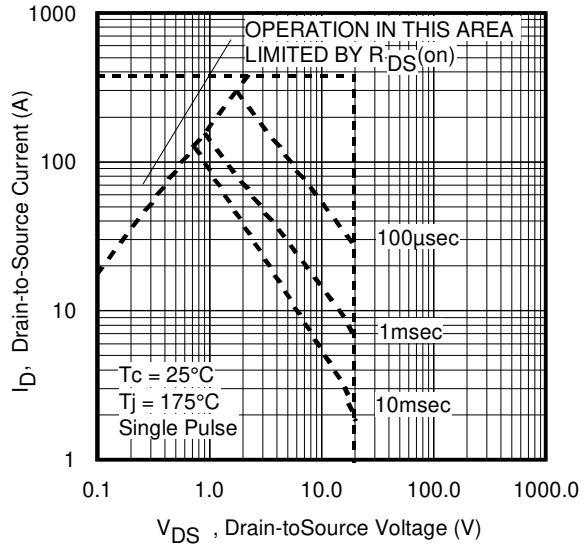Fig 7. Typical Source-Drain Diode
Forward Voltage

Fig 8. Maximum Safe Operating Area

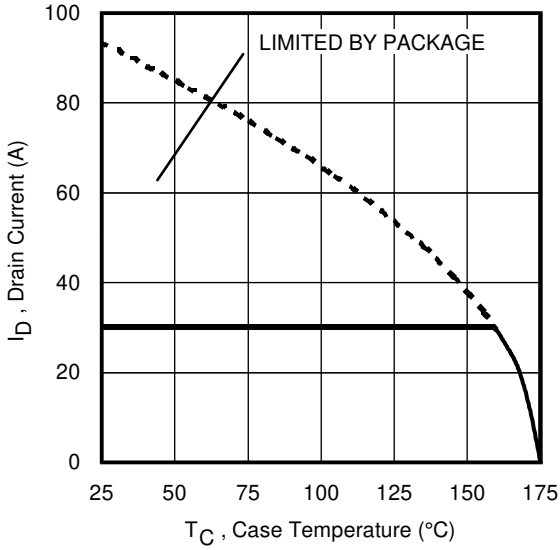4   www.irf.com
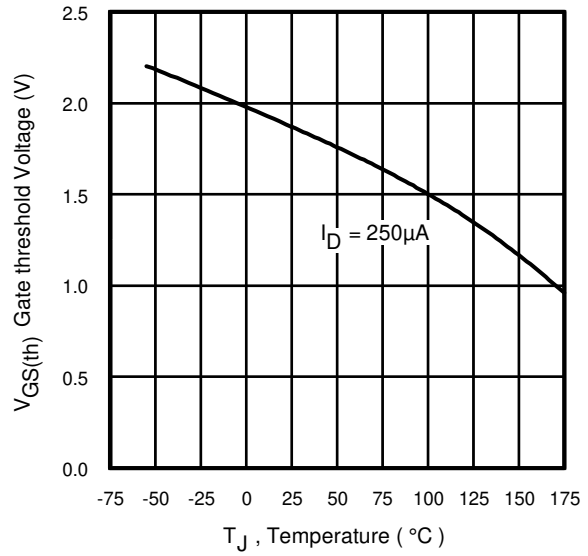
Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τi (sec)
0.805	0.000237
0.606	0.001005
0.492	0.101628

Ci= τi/Ri

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc
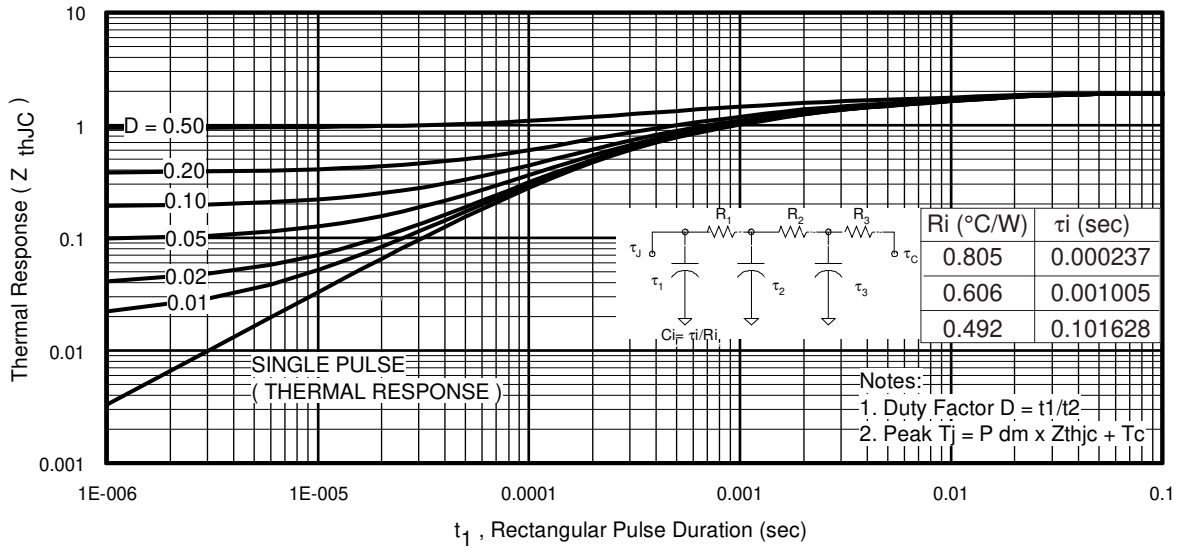
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFR/U3711ZPbF

International
IOR Rectifier
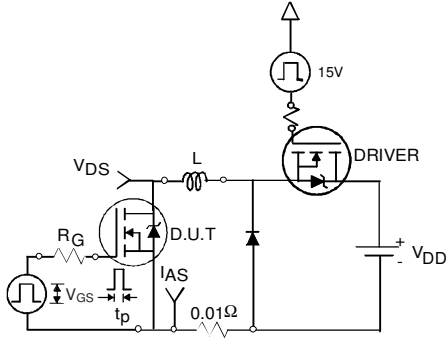
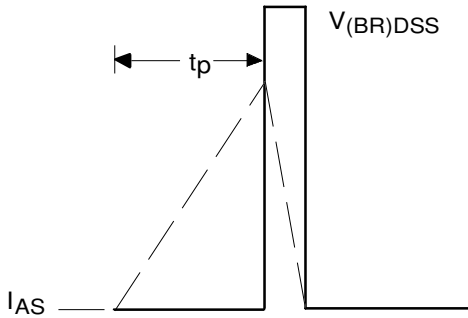**Fig 12a.** Unclamped Inductive Test Circuit
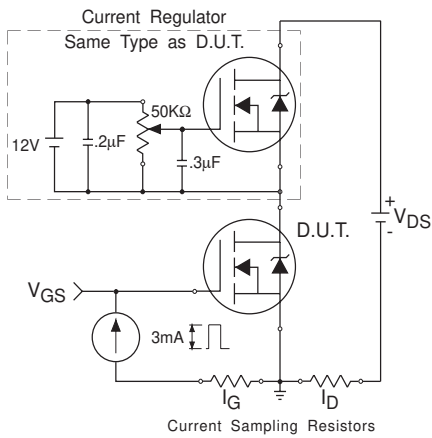

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

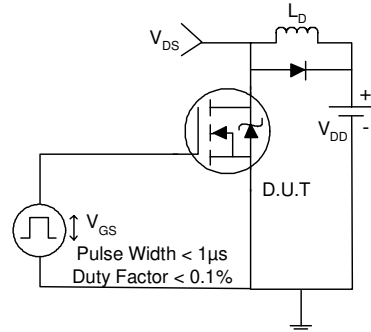**Fig 13.** Gate Charge Test Circuit

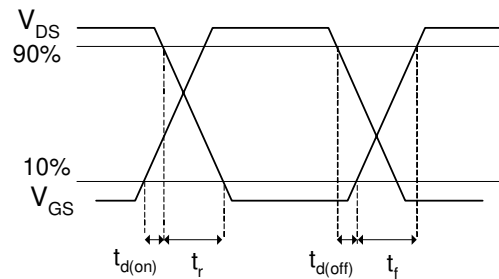**Fig 14a.** Switching Time Test Circuit

Fig 14b. Switching Time Waveforms

6

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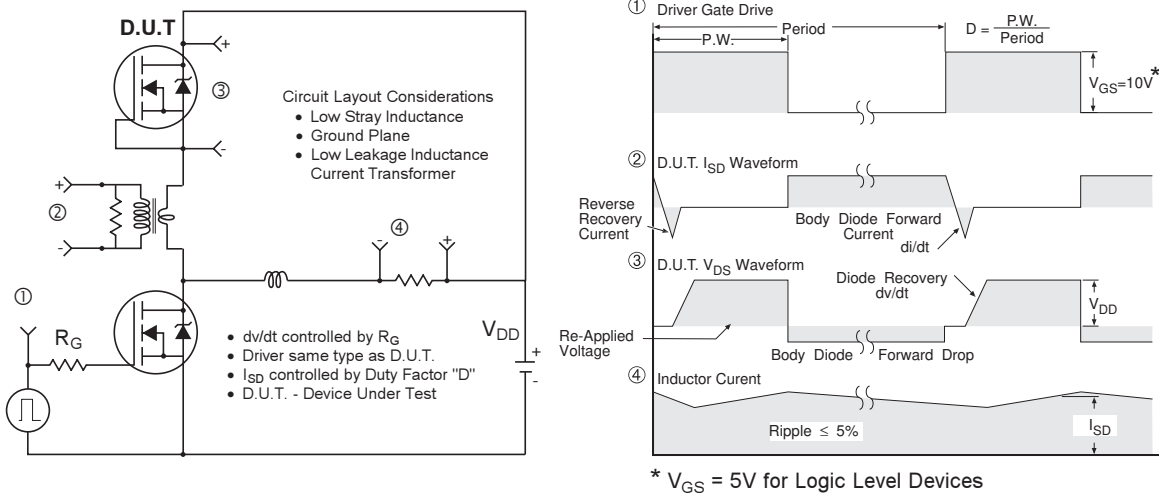
Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs

Fig 16. Gate Charge Waveform

IRFR/U3711ZPbF
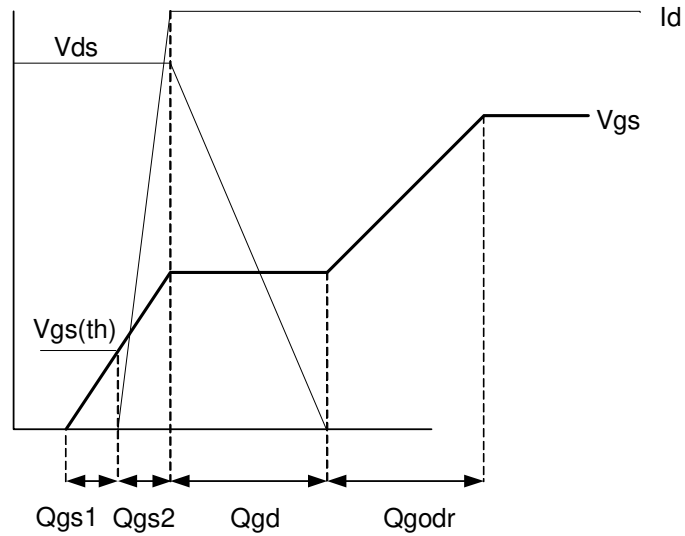
Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$
$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.
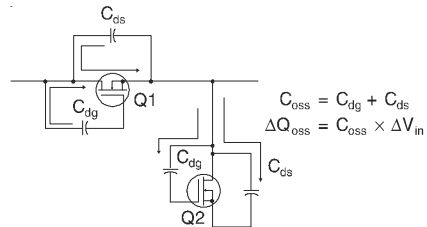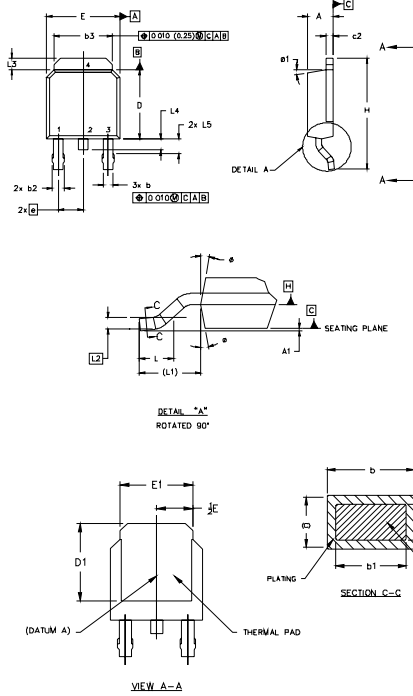

$$C_{oss} = C_{dg} + C_{ds}$$
$$\Delta Q_{oss} = C_{oss} \times \Delta V_{in}$$

Figure A: Q_{oss} Characteristic

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

NOTES:
1.0   DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0   DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0   LEAD DIMENSION UNCONTROLLED IN L5
4.0   DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0   SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND
       .010 [0.2540 FROM THE LEAD TIP.
6.0   DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED
       .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST
       EXTREMES OF THE PLASTIC BODY.
7.0   OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.196	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	6
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170		4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

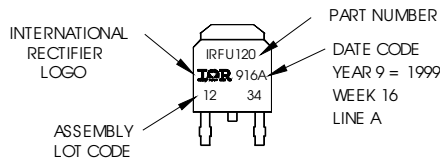HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR
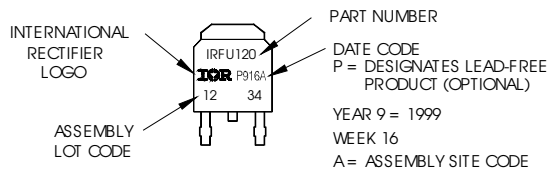
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
           WITH ASSEMBLY
           LOT CODE 1234
           ASSEMBLED ON WW 16, 1999
           IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
      indicates "Lead-Free"

PART NUMBER
DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

OR

PART NUMBER
DATE CODE
P = DESIGNATES LEAD-FREE
    PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 16
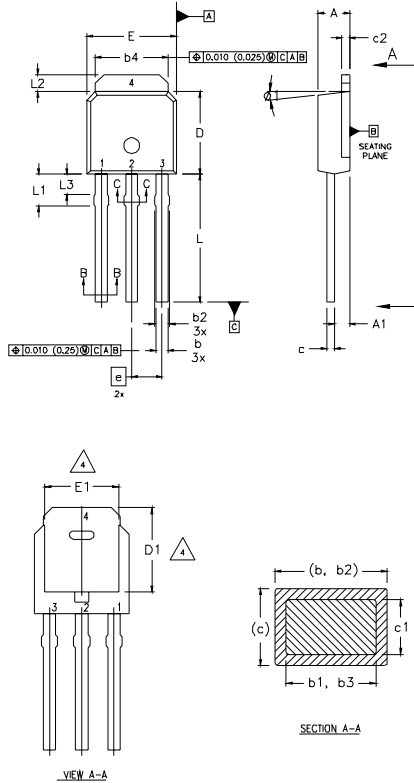A = ASSEMBLY SITE CODE

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

I-Pak (TO-251AA) Package Outline
Dimensions are shown in millimeters (inches)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5. LEAD DIMENSION UNCONTROLLED IN L3.
6. DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7. OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
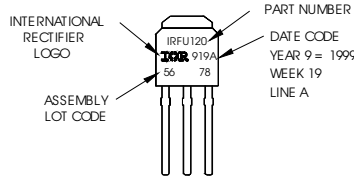8. CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

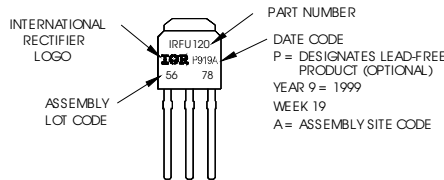| SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	–	0.205	–	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	–	0.170	–	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0°	15°	0°	15°	

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"

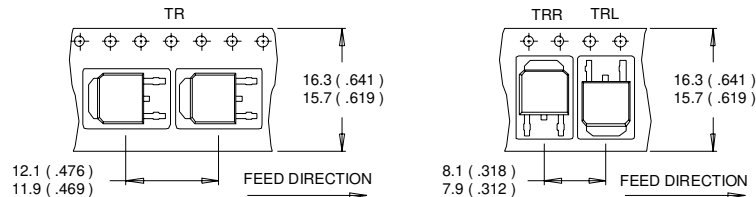**Note:** "P" in assembly line position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE YEAR 9 = 1999 WEEK 19 LINE A

ASSEMBLY LOT CODE

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 19
A = ASSEMBLY SITE CODE

ASSEMBLY LOT CODE

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TR

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

TRR   TRL

16.3 (.641)
15.7 (.619)

8.1 (.318)
7.9 (.312)

FEED DIRECTION

NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

⌀ 13 INCH

16 mm
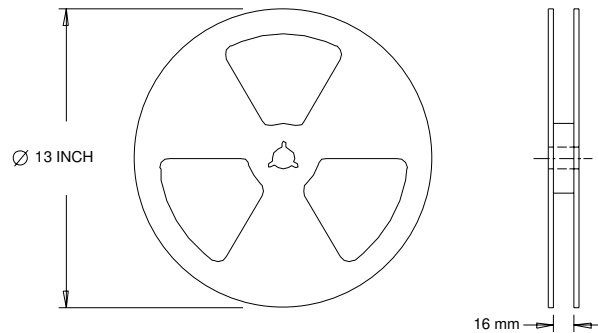
NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.9mH, R_G = 25Ω, I_{AS} = 12A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

International **IƏR** Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/