



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

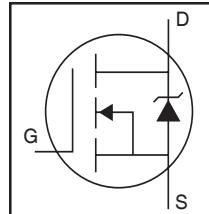
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

IRFR4620PbF

IRFU4620PbF

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

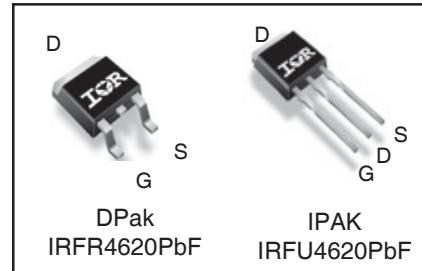


HEXFET® Power MOSFET

V_{DSS}	200V
R_{DS(on)}	typ. 64mΩ
	max. 78mΩ
I_D	24A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	24	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	17	
I _{DM}	Pulsed Drain Current ①	100	
P _D @ T _C = 25°C	Maximum Power Dissipation	144	W
	Linear Derating Factor	0.96	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	54	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	113	mJ
I _{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E _{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑧	—	1.045	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) ⑦	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes ① through ⑧ are on page 11

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ①
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	64	78	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 15\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250	μA	$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$R_{\text{G}(\text{int})}$	Internal Gate Resistance	—	2.6	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	37	—	—	S	$V_{DS} = 50V, I_D = 15\text{A}$
Q_g	Total Gate Charge	—	25	38	nC	$I_D = 15\text{A}$
Q_{gs}	Gate-to-Source Charge	—	8.2	—	nC	$V_{DS} = 100V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.9	—	nC	$V_{GS} = 10V$ ④
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	17	—	nC	$I_D = 15\text{A}, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	13.4	—	ns	$V_{DD} = 130V$
t_r	Rise Time	—	22.4	—	ns	$I_D = 15\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	25.4	—	ns	$R_G = 7.3\Omega$
t_f	Fall Time	—	14.8	—	ns	$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	1710	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	125	—	pF	$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	30	—	pF	$f = 1.0\text{MHz}$ (See Fig.5)
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) ⑥	—	113	—		$V_{GS} = 0V, V_{DS} = 0V$ to $160V$ ⑥ (See Fig.11)
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) ⑤	—	317	—		$V_{GS} = 0V, V_{DS} = 0V$ to $160V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	24	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{sM}	Pulsed Source Current (Body Diode) ①	—	—	100	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 15\text{A}, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	78	—	ns	$T_J = 25^\circ\text{C} \quad V_R = 100V,$
		—	99	—	ns	$T_J = 125^\circ\text{C} \quad I_F = 15\text{A}$
Q_{rr}	Reverse Recovery Charge	—	294	—	nC	$T_J = 25^\circ\text{C} \quad \text{di/dt} = 100\text{A}/\mu\text{s}$ ④
		—	432	—	nC	$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	7.6	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

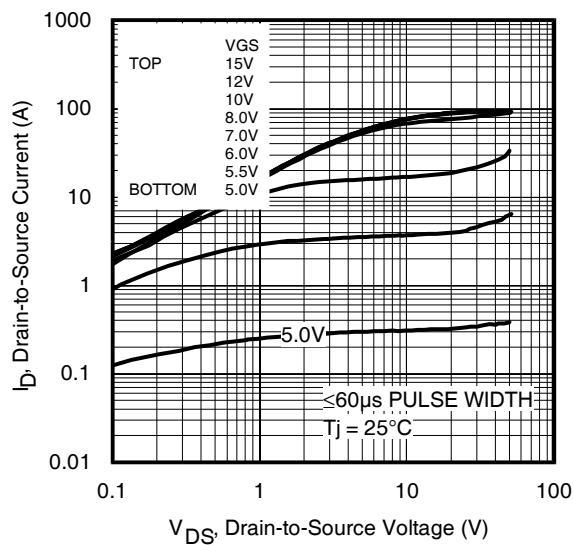


Fig 1. Typical Output Characteristics

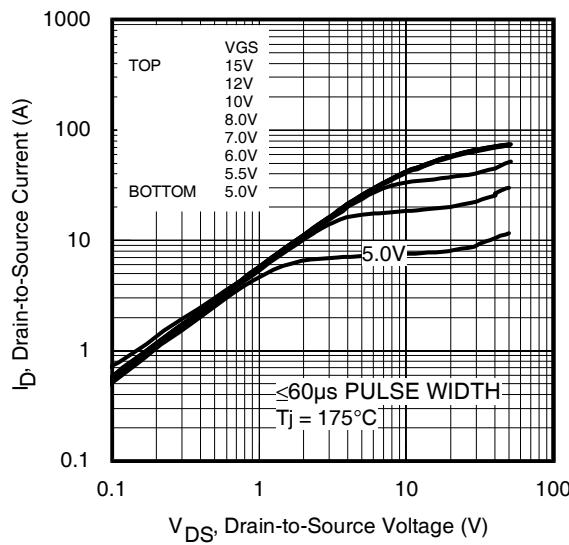


Fig 2. Typical Output Characteristics

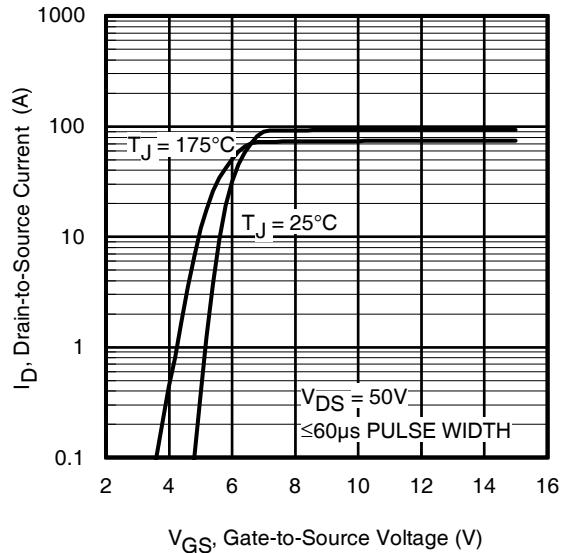


Fig 3. Typical Transfer Characteristics

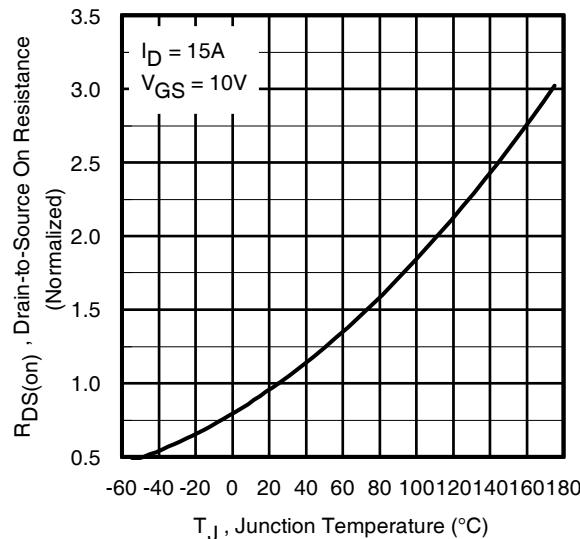


Fig 4. Normalized On-Resistance vs. Temperature

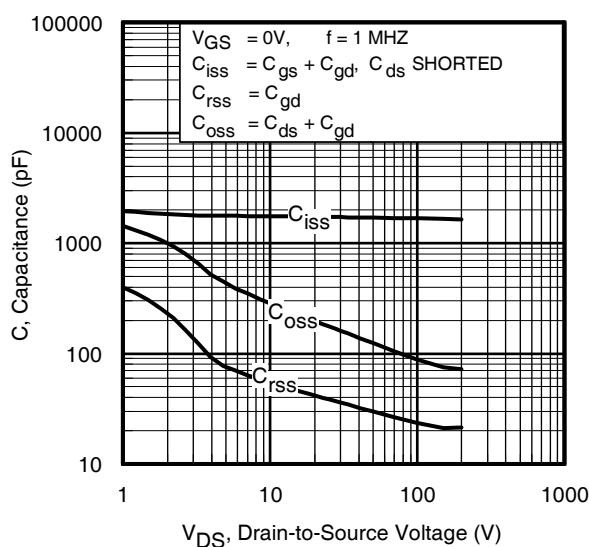


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

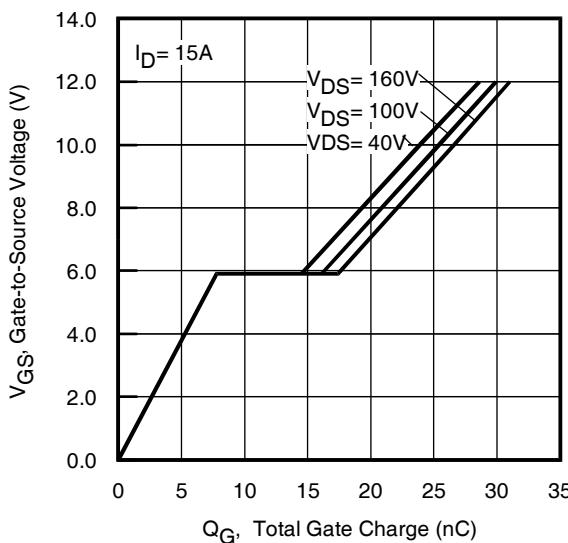


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

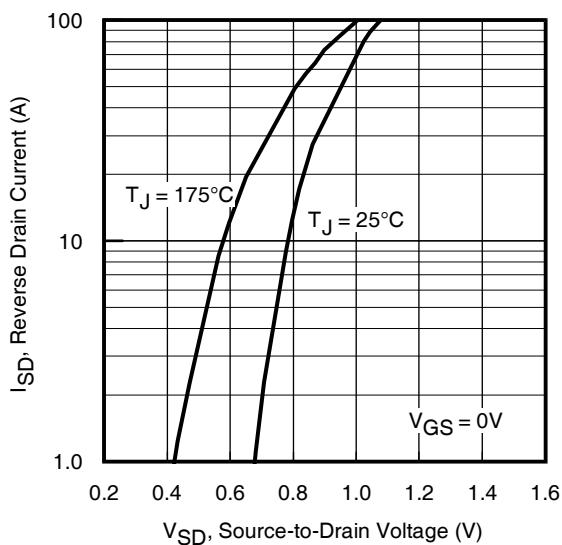


Fig 7. Typical Source-Drain Diode Forward Voltage

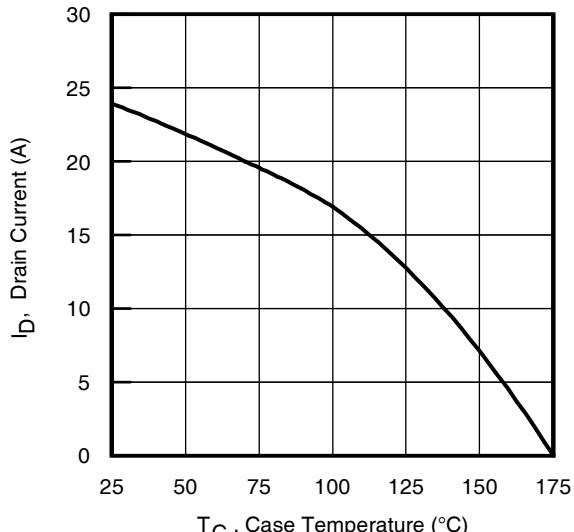


Fig 9. Maximum Drain Current vs. Case Temperature

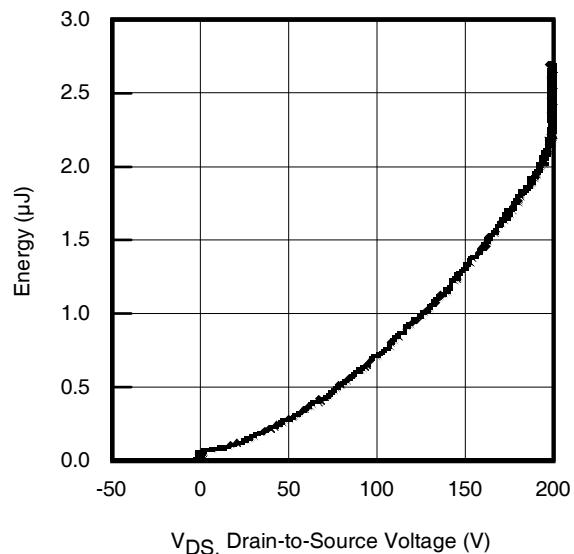


Fig 11. Typical C_{oss} Stored Energy

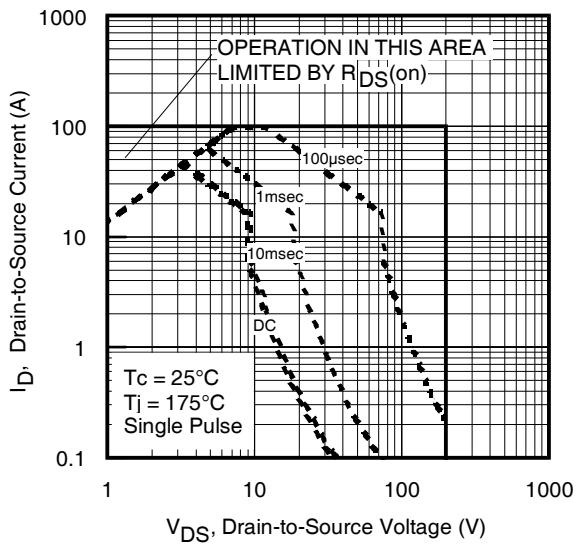


Fig 8. Maximum Safe Operating Area

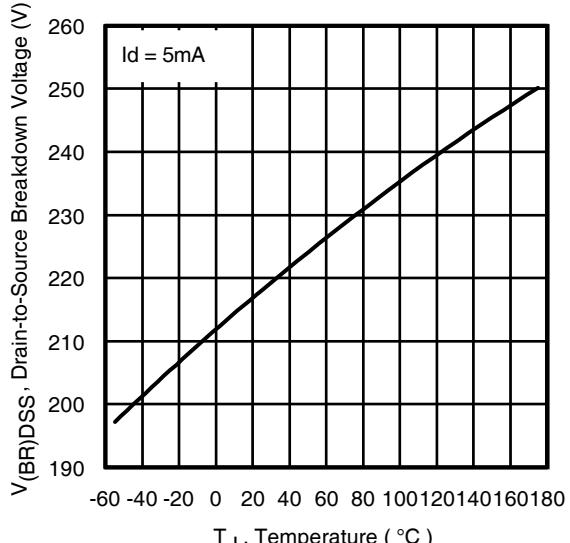


Fig 10. Drain-to-Source Breakdown Voltage

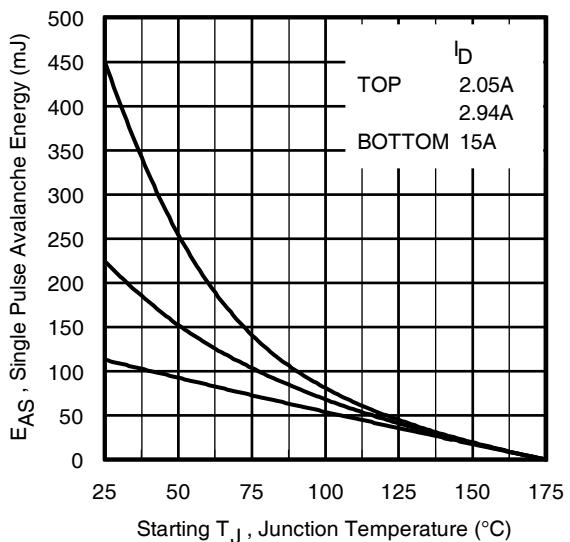


Fig 12. Maximum Avalanche Energy vs. Drain Current

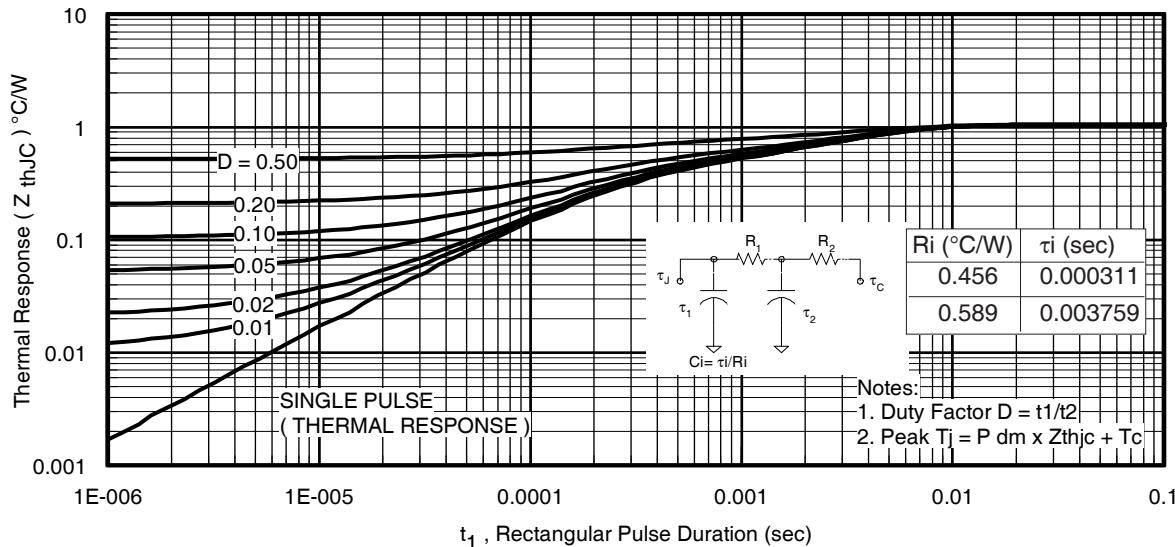


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

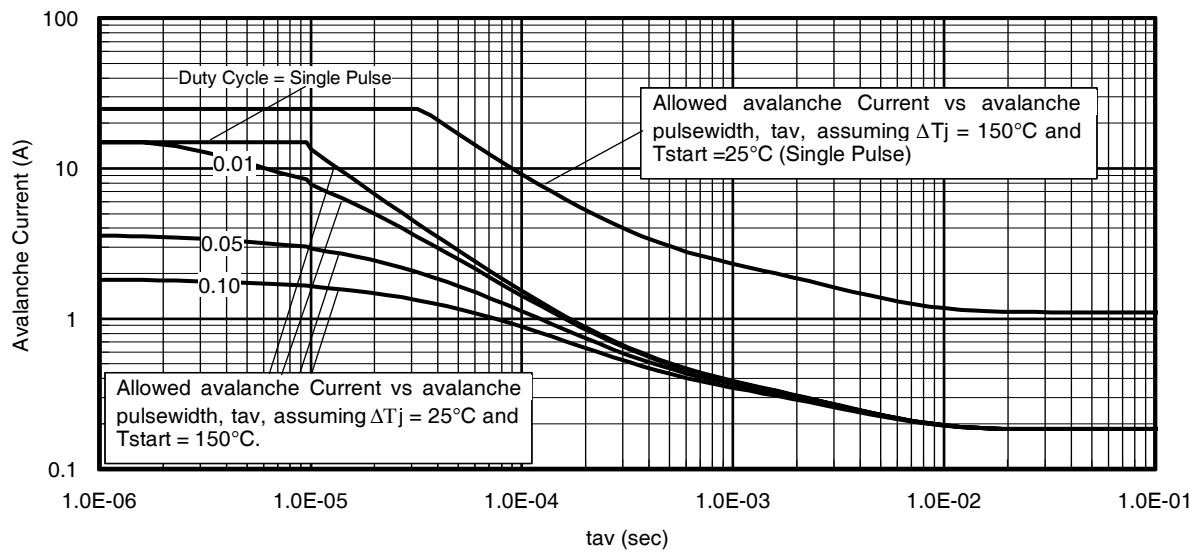


Fig 14. Typical Avalanche Current vs.Pulsewidth

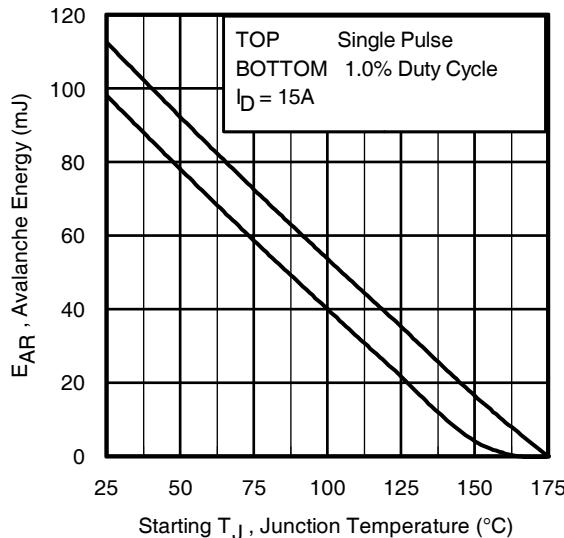
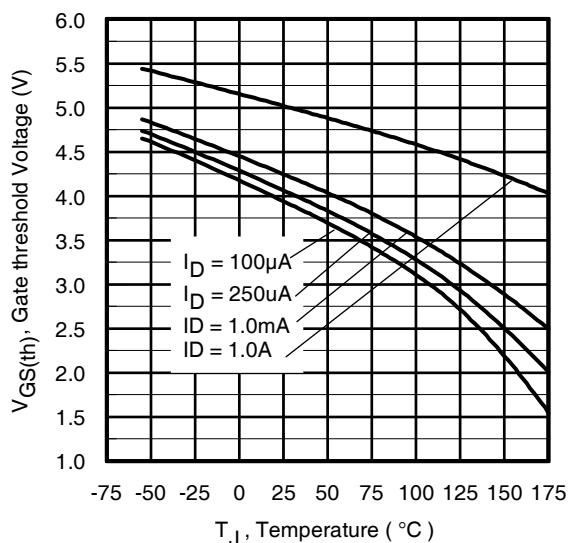
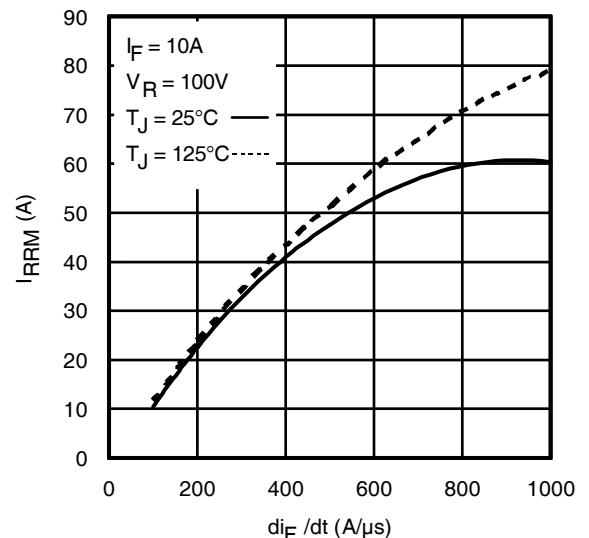
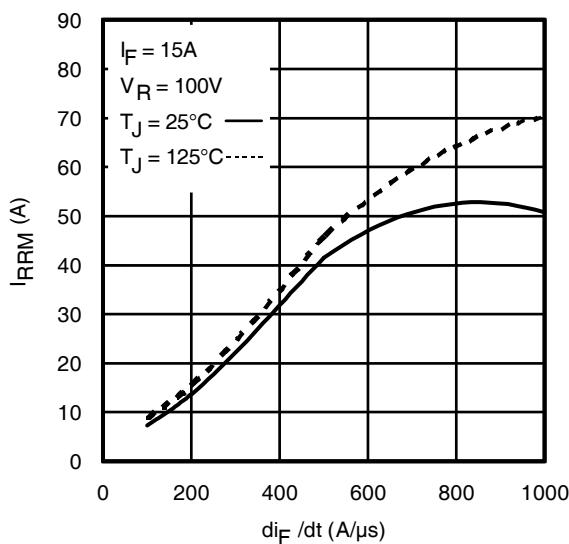
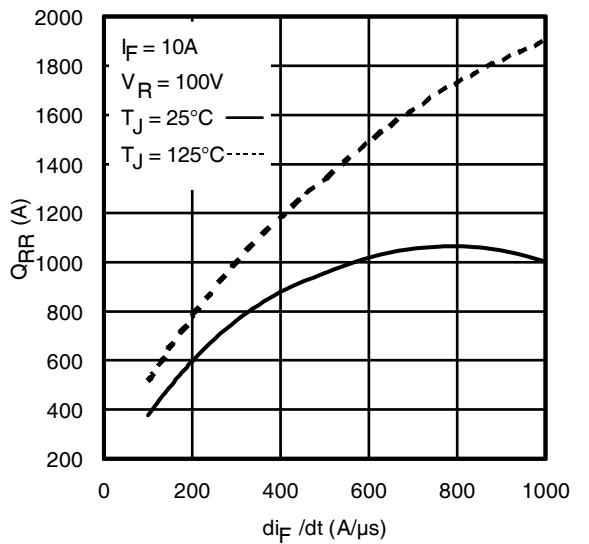
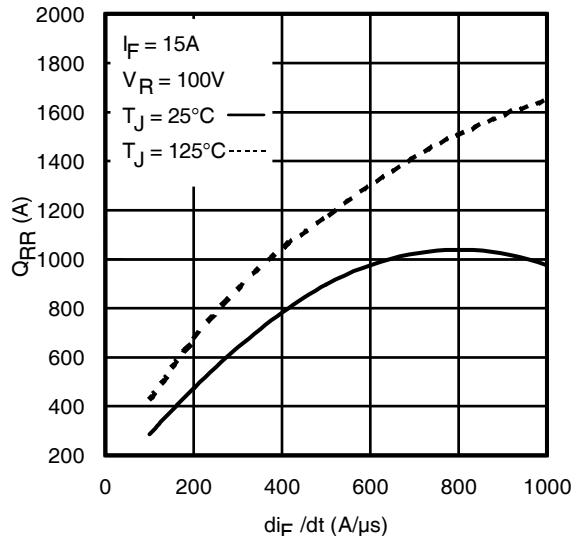


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
- t_{av} = Average time in avalanche.
- D = Duty cycle in avalanche = $t_{av} \cdot f$
- $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13

$$\begin{aligned} P_{D(ave)} &= 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC} \\ I_{av} &= 2\Delta T / [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS(AR)} &= P_{D(ave)} \cdot t_{av} \end{aligned}$$

**Fig. 16.** Threshold Voltage vs. Temperature**Fig. 17 -** Typical Recovery Current vs. di_f/dt **Fig. 18 -** Typical Recovery Current vs. di_f/dt **Fig. 19 -** Typical Stored Charge vs. di_f/dt **Fig. 20 -** Typical Stored Charge vs. di_f/dt

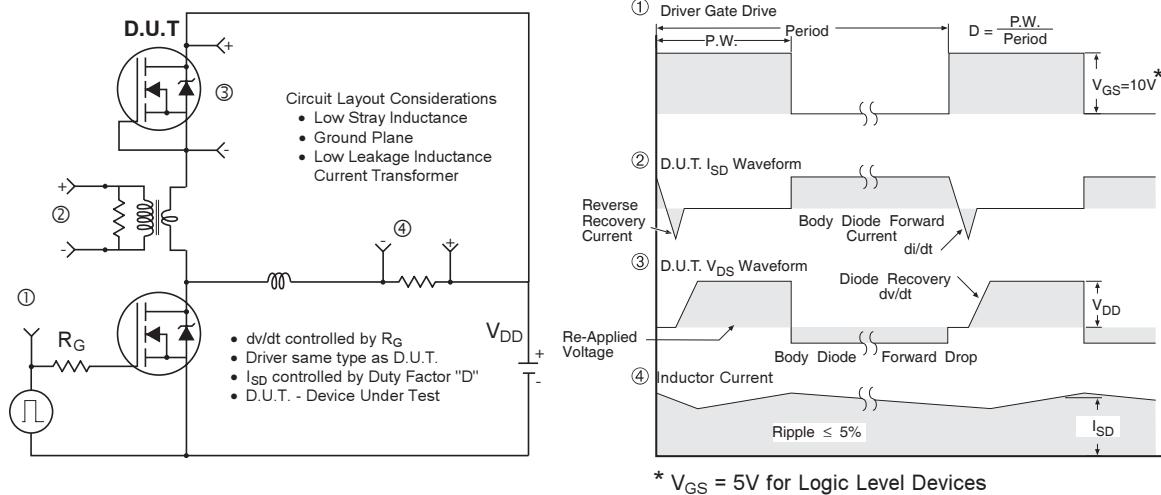


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

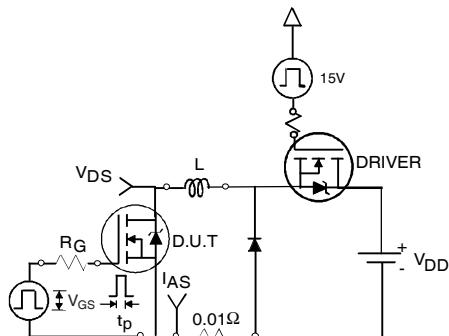


Fig 22a. Unclamped Inductive Test Circuit

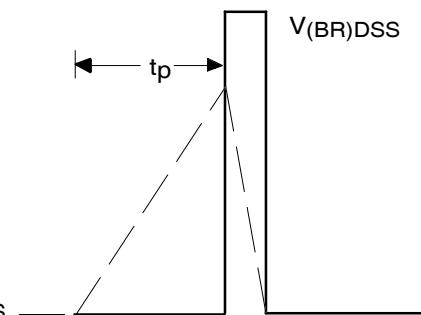


Fig 22b. Unclamped Inductive Waveforms

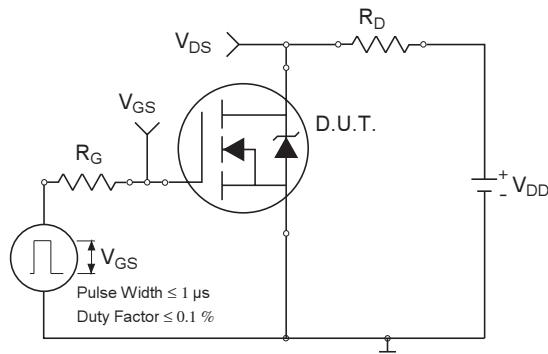


Fig 23a. Switching Time Test Circuit

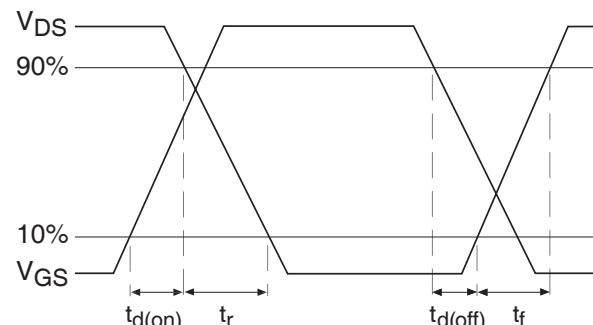


Fig 23b. Switching Time Waveforms

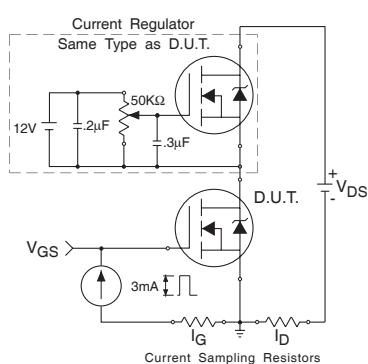


Fig 24a. Gate Charge Test Circuit

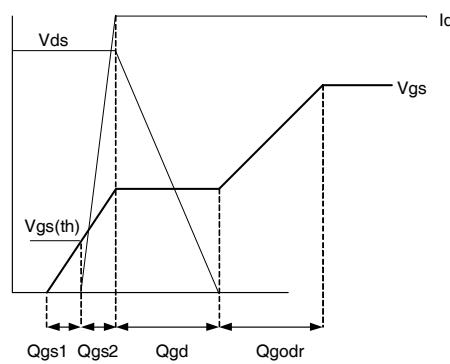
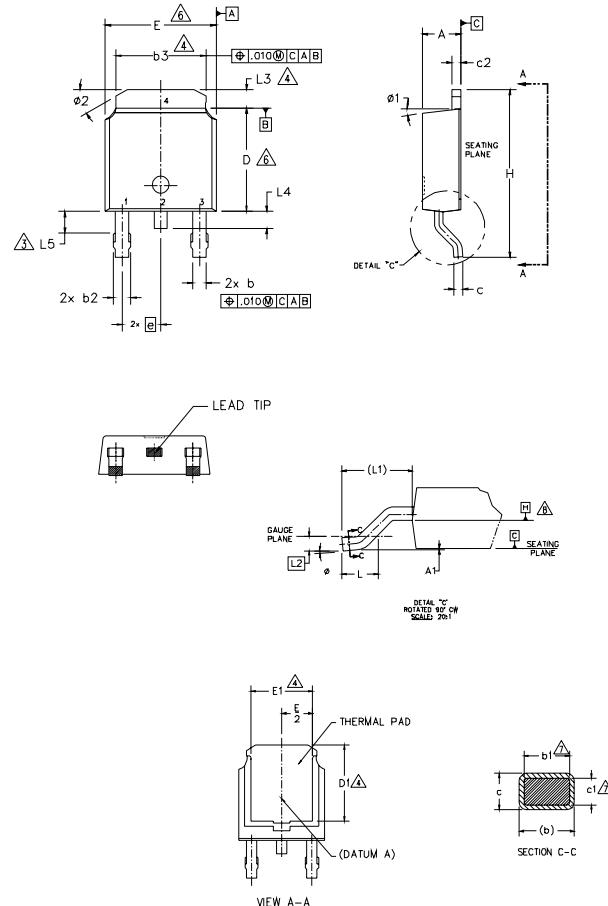


Fig 24b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- △ - LEAD DIMENSION UNCONTROLLED IN L5.
- △ - DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △ - DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △ - DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △ - DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS		NOTES	
	MILLIMETERS			
	MIN.	MAX.		
A	2.18	2.39	.086 .094	
A1	—	0.13	— .005	
b	0.64	0.89	.025 .035	
b1	0.65	0.79	.025 .031	
b2	0.76	1.14	.030 .045	
b3	4.95	5.46	.195 .215	
c	0.46	0.61	.018 .024	
c1	0.41	0.56	.016 .022	
c2	0.46	0.89	.018 .035	
D	5.97	6.22	.235 .245	
D1	5.21	—	.205 —	
E	6.35	6.73	.250 .265	
E1	4.32	—	.170 —	
e	2.29 BSC	—	.090 BSC	
H	9.40	10.41	.370 .410	
L	1.40	1.78	.055 .070	
L1	2.74 BSC	—	.108 REF.	
L2	0.51 BSC	—	.020 BSC	
L3	0.89	1.27	.035 .050	
L4	—	1.02	— .040	
L5	1.14	1.52	.045 .060	
Ø	0°	10°	0° 10°	
Ø1	0°	15°	0° 15°	
Ø2	25°	35°	25° 35°	

LEAD ASSIGNMENTSHEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

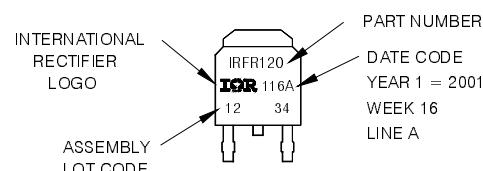
- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

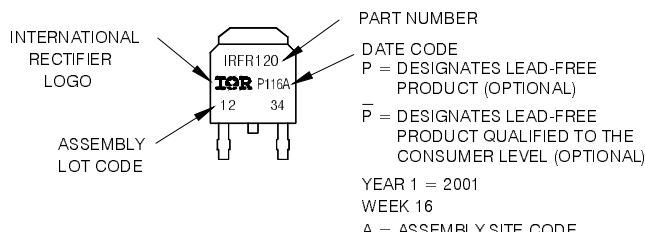
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position
indicates 'Lead-Free'

‘P’ in assembly line position indicates
‘Lead-Free’ qualification to the consumer-level



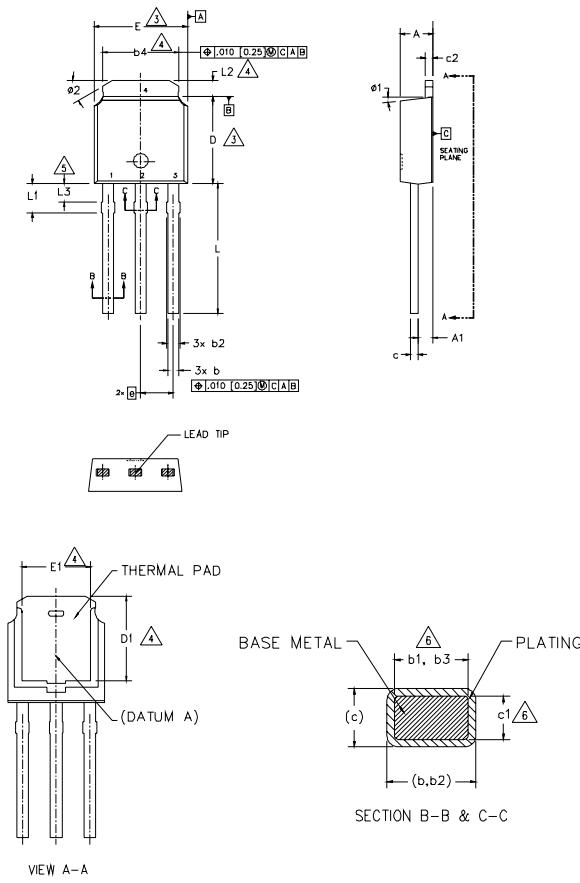
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5.- LEAD DIMENSION UNCONTROLLED IN L3.
- 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

S Y M B O L	DIMENSIONS		N O T E S	
	MILLIMETERS			
	MIN.	MAX.		
A	2.18	2.39	.086 .094	
A1	0.89	1.14	.035 .045	
b	0.64	0.89	.025 .035	
b1	0.65	0.79	.025 .031	
b2	0.76	1.14	.030 .045	
b3	0.76	1.04	.030 .041	
b4	4.95	5.46	.195 .215	
c	0.46	0.61	.018 .024	
c1	0.41	0.56	.016 .022	
c2	0.46	0.89	.018 .035	
D	5.97	6.22	.235 .245	
D1	5.21	—	.205 —	
E	6.35	6.73	.250 .265	
E1	4.32	—	.170 —	
e	2.29	BSC	.090 BSC	
L	8.89	9.65	.350 .380	
L1	1.91	2.29	.045 .090	
L2	0.89	1.27	.035 .050	
L3	1.14	1.52	.045 .060	
Ø1	0°	15°	0° 15°	
Ø2	25°	35°	25° 35°	

LEAD ASSIGNMENTS

HEXFET

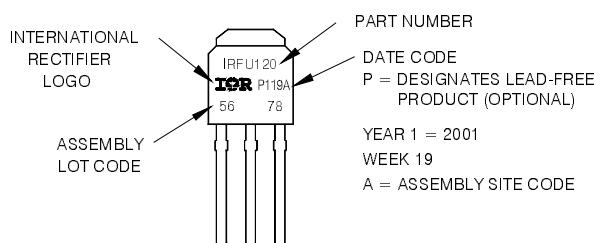
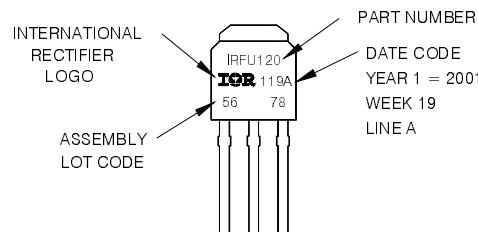
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 2001
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position
indicates Lead-Free'

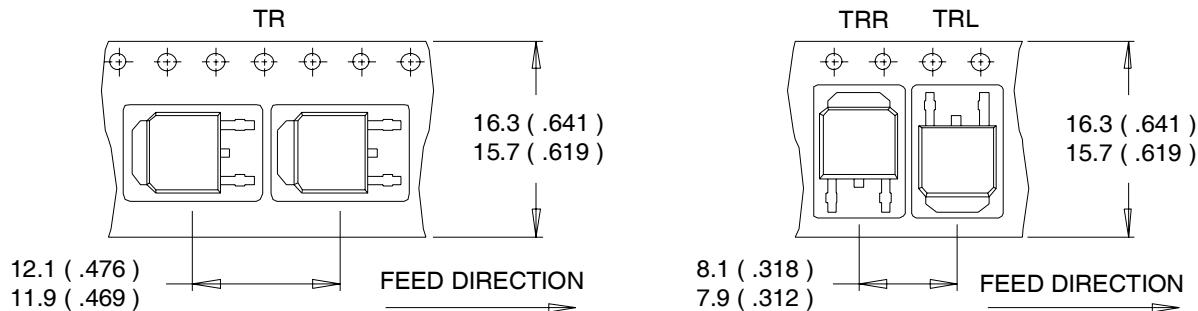
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
www.irf.com

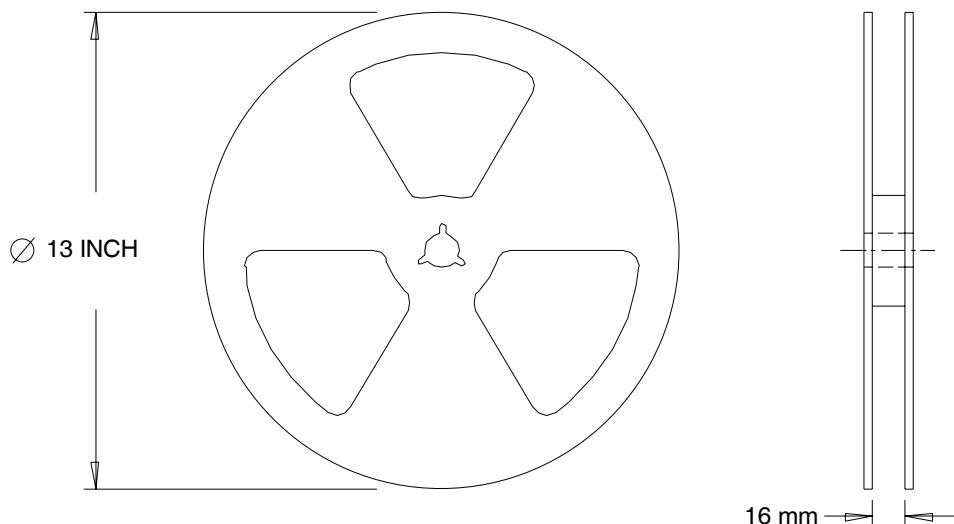
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFR4620PbF	D-PAK	Tube/Bulk	75	
IRFR4620TRPbF	D-PAK	Tape and Reel	2000	
IRFU4620PbF	I-PAK	Tube/Bulk	75	

Qualification Information[†]

Qualification level	Industrial ^{††}	
	(per JEDEC JESD47F ^{†††} guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	D-PAK	MSL1
		(per JEDEC J-STD-020D ^{†††})
	I-PAK	Not applicable
RoHS Compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ C$, $L = 1.0mH$
 $R_G = 25\Omega$, $I_{AS} = 15A$, $V_{GS} = 10V$. Part not recommended for use above this value .
- ③ $I_{SD} \leq 15A$, $dI/dt \leq 634A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ C$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately $90^\circ C$

Data and specifications subject to change without notice

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 06/2009