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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# IRFR825TRPbF

HEXFET® Power MOSFET

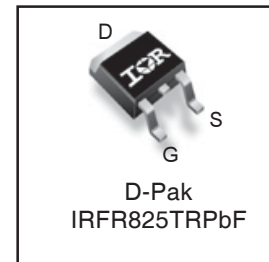
## Applications

- Zero Voltage Switching SMPS
- Uninterruptible Power Supplies
- Motor Control applications

$V_{DSS}$	$R_{DS(on)}$ typ.	$T_{rr}$ typ.	$I_D$
500V	1.05Ω	92ns	6.0A

## Features and Benefits

- Fast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Higher Gate voltage threshold offers improved noise immunity.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	6.0	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	3.9	
$I_{DM}$	Pulsed Drain Current ①	24	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	119	W
	Linear Derating Factor	1.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	9.9	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	6.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	24		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 6.0\text{A}$ , $V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	92	138	ns	$T_J = 25^\circ\text{C}$ , $I_F = 6.0\text{A}$
		—	152	228		$T_J = 125^\circ\text{C}$ , $di/dt = 100\text{A}/\mu\text{s}$ ④
$Q_{rr}$	Reverse Recovery Charge	—	167	251	nC	$T_J = 25^\circ\text{C}$ , $I_S = 6.0\text{A}$ , $V_{GS} = 0\text{V}$ ④
		—	292	438		$T_J = 125^\circ\text{C}$ , $di/dt = 100\text{A}/\mu\text{s}$ ④
$I_{RRM}$	Reverse Recovery Current	—	3.6	5.4	A	$T_J = 25^\circ\text{C}$ , $I_S = 6.0\text{A}$ , $V_{GS} = 0\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes ① through ⑦ are on page 2

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.33	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.05	1.3	$\Omega$	$V_{GS} = 10V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	7.5	—	—	S	$V_{DS} = 50V, I_D = 3.7A$
$Q_g$	Total Gate Charge	—	—	34	nC	$I_D = 6.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	11		$V_{DS} = 400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	14		$V_{GS} = 10V, \text{See Fig. 14a \& 14b}$ ④
$t_{d(on)}$	Turn-On Delay Time	—	8.5	—		$V_{DD} = 250V$
$t_r$	Rise Time	—	25	—	ns	$I_D = 6.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 7.5\Omega$
$t_f$	Fall Time	—	20	—		$V_{GS} = 10V, \text{See Fig. 15a \& 15b}$ ④
$C_{iss}$	Input Capacitance	—	1346	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	76	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	15	—		$f = 1.0\text{KHz}, \text{See Fig. 5}$
$C_{oss}$	Output Capacitance	—	1231	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	25	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	51	—		
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	43	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	178	mJ
$I_{AR}$	Avalanche Current ①	—	3	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	11.9	mJ

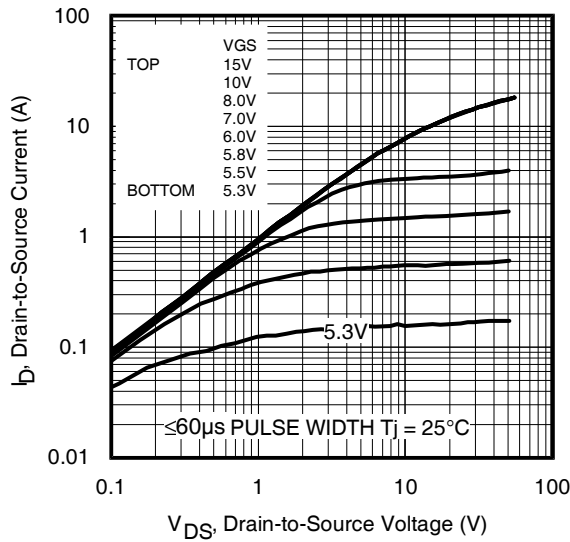
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	1.05	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

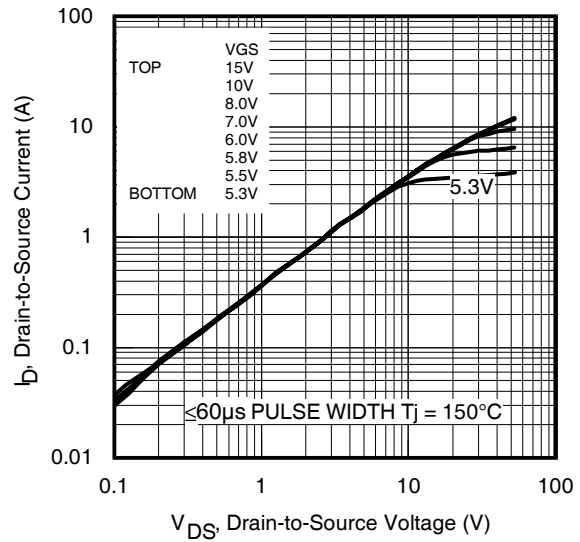
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 40\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 3.0A$ . (See Figure 13).
- ③  $I_{SD} = 6.0A$ ,  $di/dt \leq 416A/\mu s$ ,  $V_{DD} V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

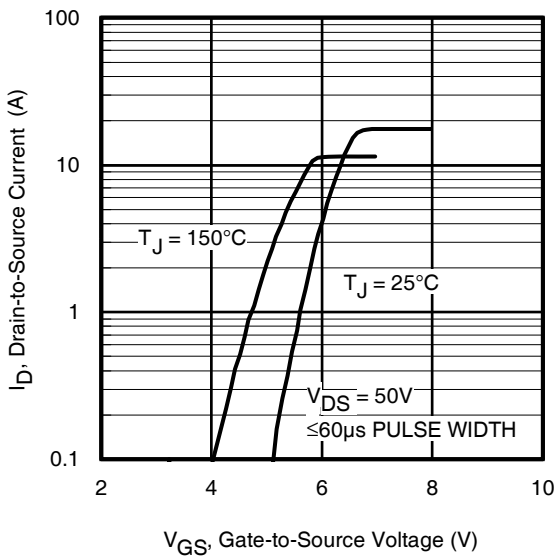
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that stores the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note # AN-994 techniques refer to application note #AN-994.



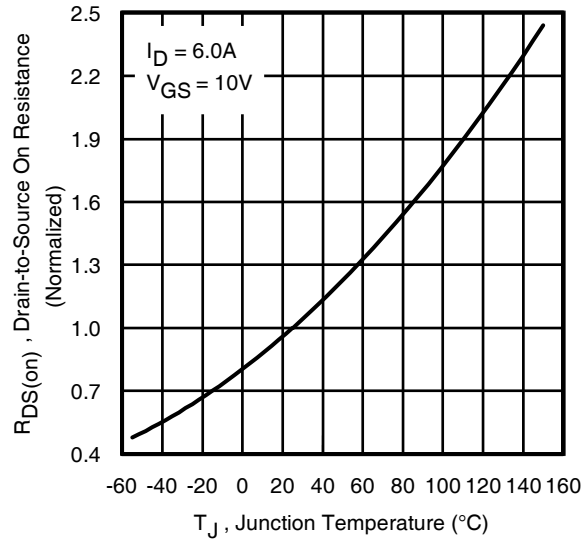
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



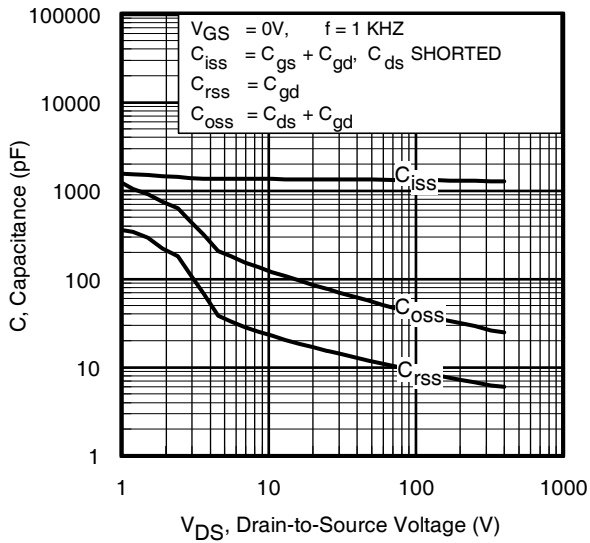
**Fig 3.** Typical Transfer Characteristics



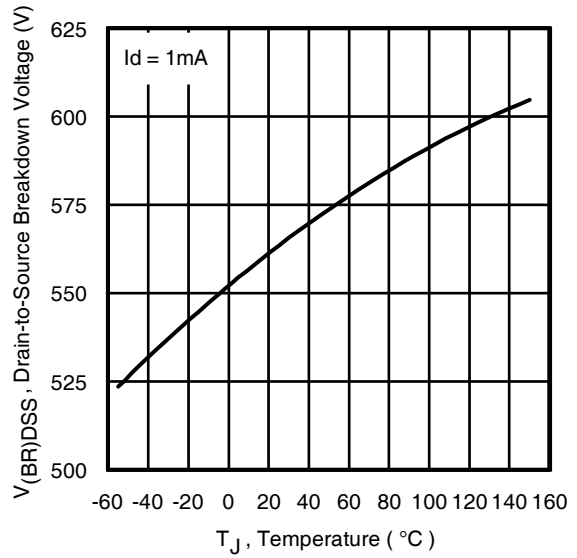
**Fig 4.** Normalized On-Resistance Vs. Temperature

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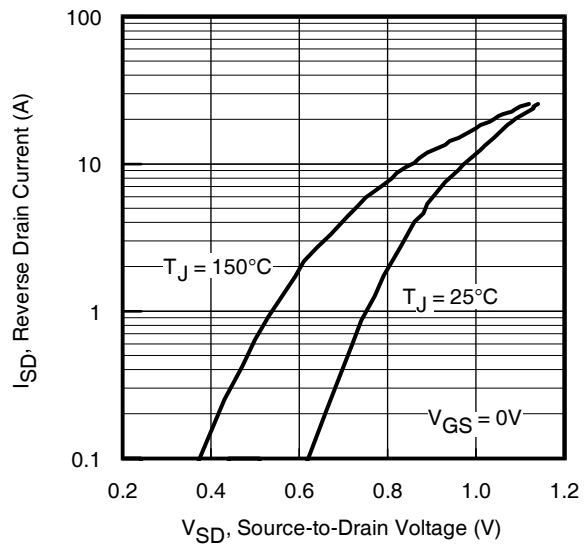
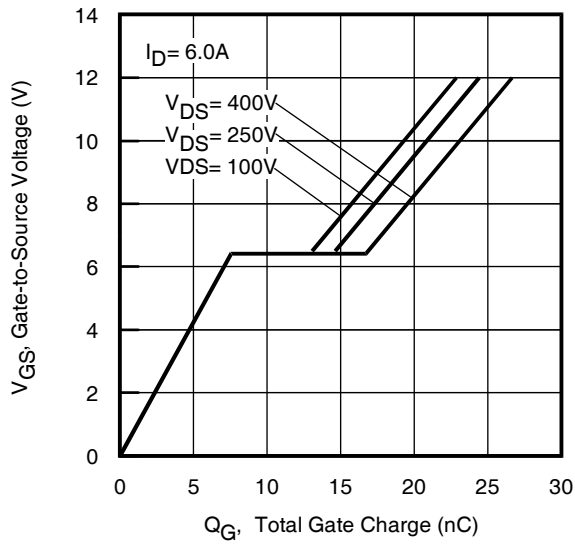
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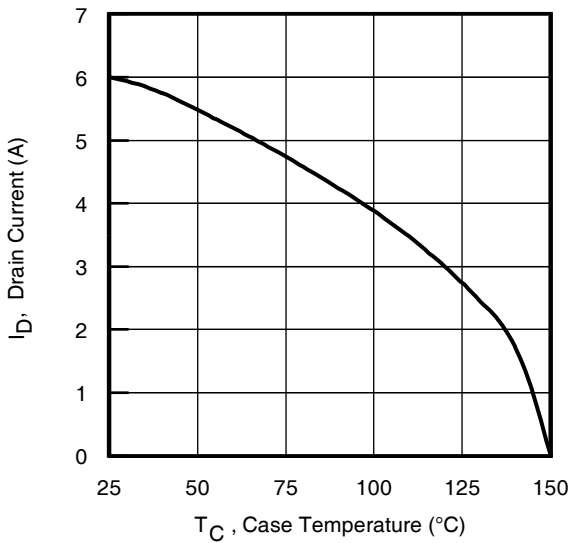


**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

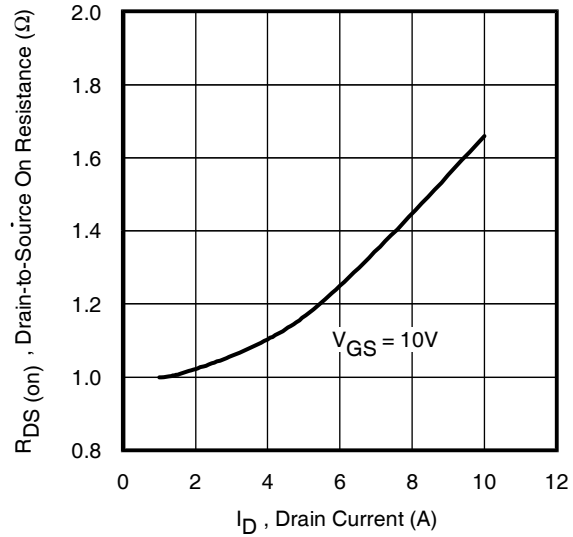


**Fig 6.** Typ. Breakdown Voltage vs. Temperature

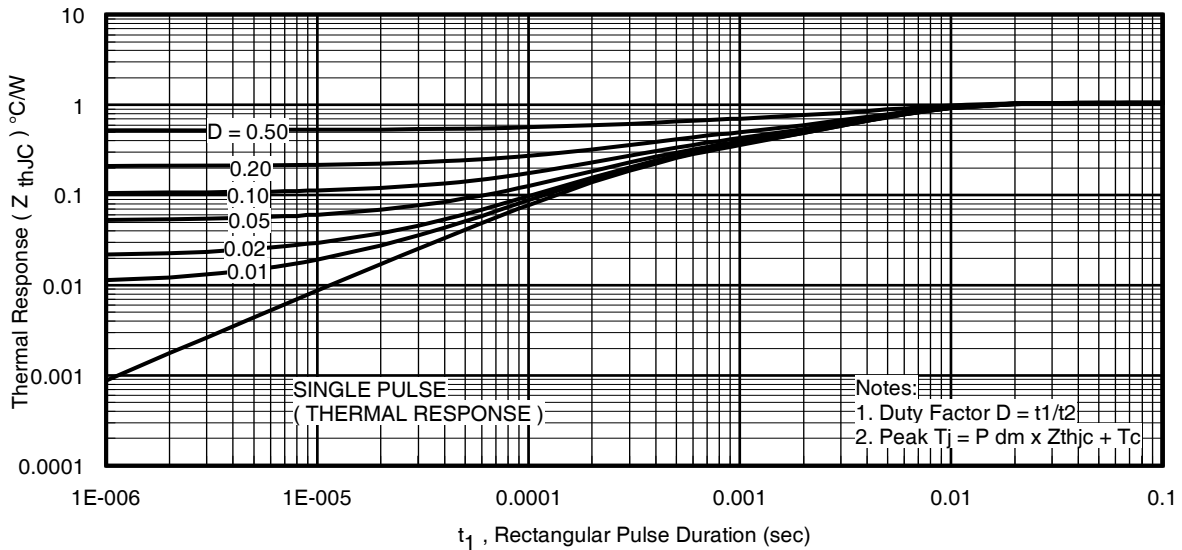




**Fig 9.** Maximum Drain Current Vs. Case Temperature



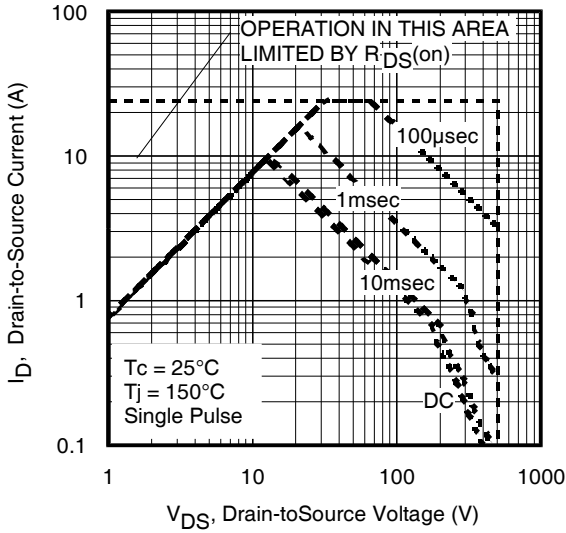
**Fig 9.** Typical  $R_{DS(on)}$  Vs. Drain Current



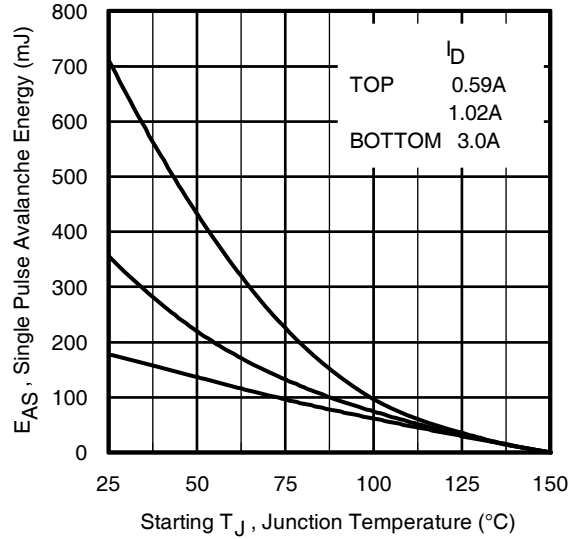
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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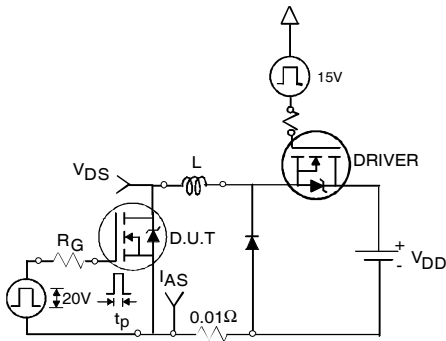
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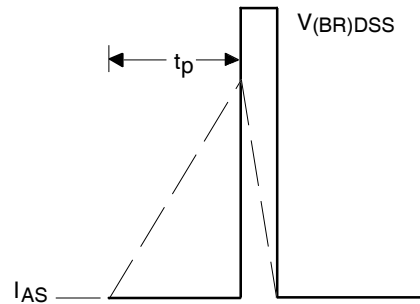
**Fig 12.** Maximum Safe Operating Area



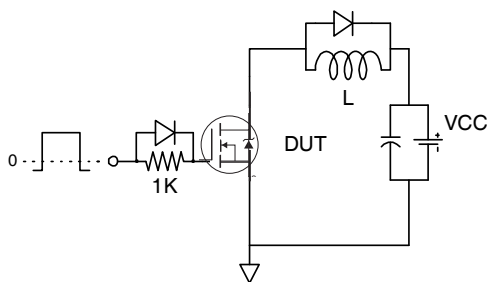
**Fig 13.** Maximum Avalanche Energy vs. Drain Current



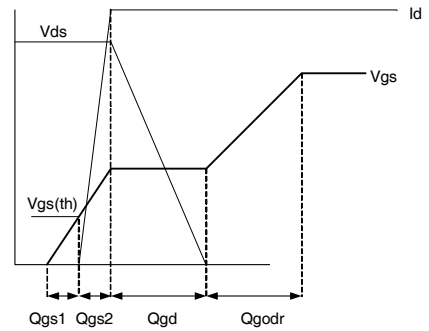
**Fig 13a.** Unclamped Inductive Test Circuit



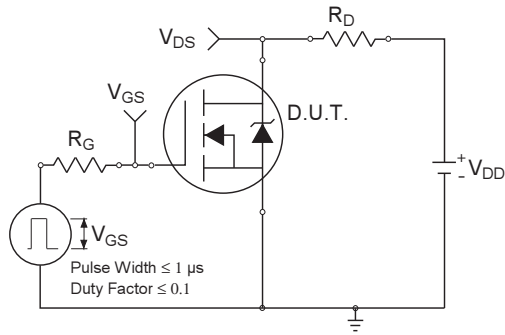
**Fig 13b.** Unclamped Inductive Waveforms



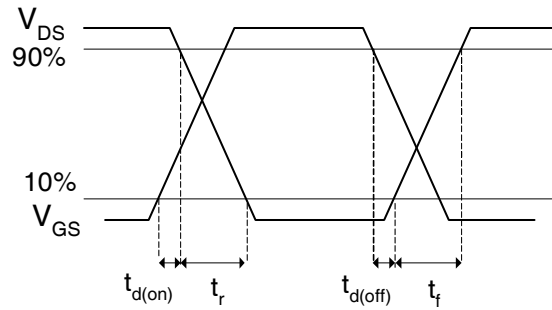
**Fig 14a.** Gate Charge Test Circuit



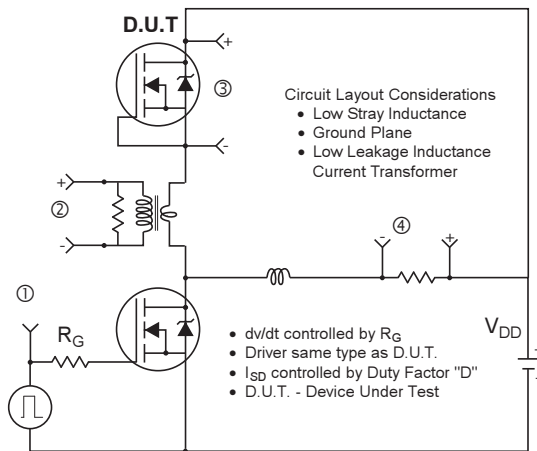
**Fig 14b.** Gate Charge Waveform



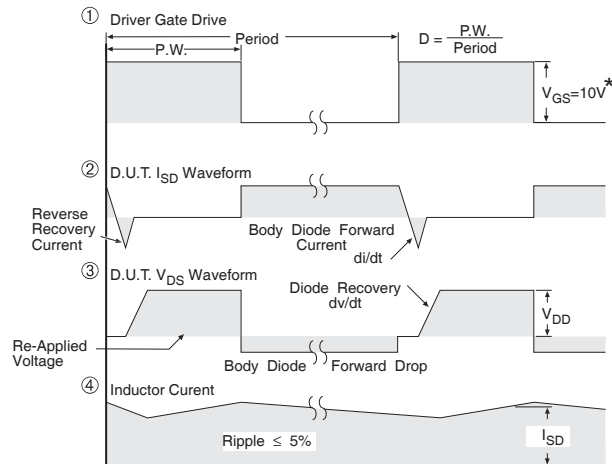
**Fig 15a.** Switching Time Test Circuit



**Fig 15b.** Switching Time Waveforms



**Fig 16.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs



\*  $V_{GS} = 5V$  for Logic Level Devices

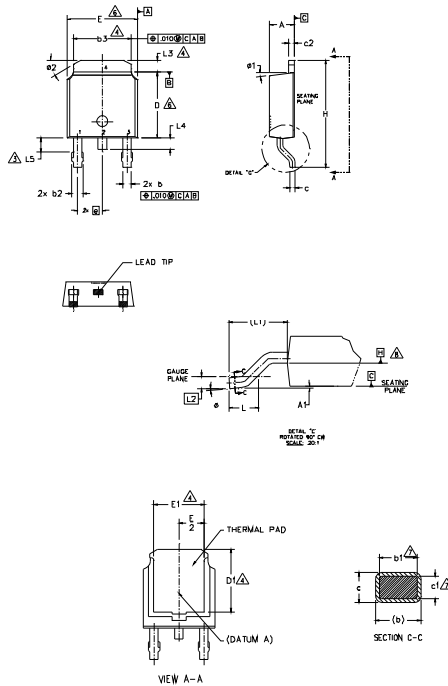


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## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS)
  - 3- LEAD DIMENSION UNCONTROLLED IN L5.
  - 4- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 (0.13 AND 0.25) FROM THE LEAD TIP.
  - 6- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 7- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
  - 8- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - 9- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	7
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.216	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	1.02	-	.040	-	
L5	1.14	1.52	.045	.060	3
#	0"	10"	0"	10"	
#1	0"	15"	0"	15"	
#2	25"	35"	25"	35"	

### LEAD ASSIGNMENTS

### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

### IGBT & CoPAK

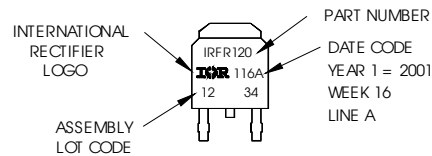
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

"P" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level



OR



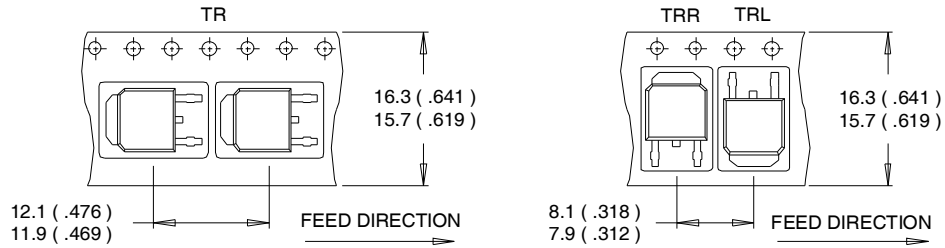
PART NUMBER  
DATE CODE  
P = DESIGNATES LEAD-FREE  
PRODUCT (OPTIONAL)  
P̄ = DESIGNATES LEAD-FREE  
PRODUCT QUALIFIED TO THE  
CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001  
WEEK 16  
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

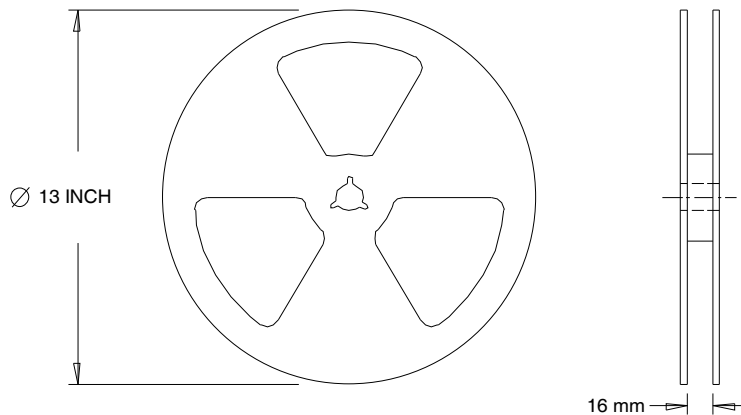
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.