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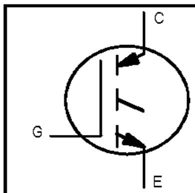
PD- 95657

International
IOR Rectifier

IRG4P254SPbF

Standard Speed IGBT

INSULATED GATE BIPOLAR TRANSISTOR



n-channel

$V_{CES} = 250V$

$V_{CE(on)\,typ.} = 1.32V$

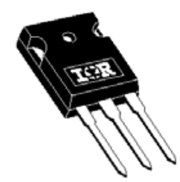
$@V_{GE} = 15V, I_C = 55A$

Features

- Standard: Optimized for minimum saturation voltage and operating frequencies up to 10kHz
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard TO-247AC package
- Lead-Free

Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- High Power density
- Lower conduction losses than similarly rated MOSFET
- Lower Gate Charge than equivalent MOSFET
- Simple Gate Drive characteristics compared to Thyristors



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	250	V
I_C @ T_C = 25°C	Continuous Collector Current	98*	A
I_C @ T_C = 100°C	Continuous Collector Current	55	
I_{CM}	Pulsed Collector Current ①	196	
I_{LM}	Clamped Inductive Load Current ②	196	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	160	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	----	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	----	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	----	40	
Wt	Weight	6.0 (0.21)	----	g (oz)

* Package limited to 70A

7/26/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	250	—	—	V	V_{GE} = 0V, I_C = 250µA	
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A	
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.33	—	V/°C	V_{GE} = 0V, I_C = 1.0mA	
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.32	1.5	V	I_C = 55A	V_{GE} = 15V
		—	1.69	—		I_C =98A	See Fig.2, 5
		—	1.31	—		I_C =55A , T_J = 150°C	
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA	
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-12	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA	
g_{fe}	Forward Transconductance ⑤	43	63	—	S	V_{CE} = 100V, I_C = 55A	
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 250V	
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C	
		—	—	1000		V_{GE} = 0V, V_{CE} = 250V, T_J = 150°C	
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	200	300	nC	I_C =55A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	29	44		V_{CC} = 200V See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	66	99		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	40	—	ns	
t_r	Rise Time	—	44	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	270	400		I_C = 55A, V_{CC} = 200V
t_f	Fall Time	—	510	760		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.38	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	3.50	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	3.88	5.3		
$t_{d(on)}$	Turn-On Delay Time	—	38	—	ns	T_J = 150°C,
t_r	Rise Time	—	45	—		I_C = 55A, V_{CC} = 200V
$t_{d(off)}$	Turn-Off Delay Time	—	400	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	940	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	6.52	—	mJ	See Fig. 11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	4500	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	510	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	100	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

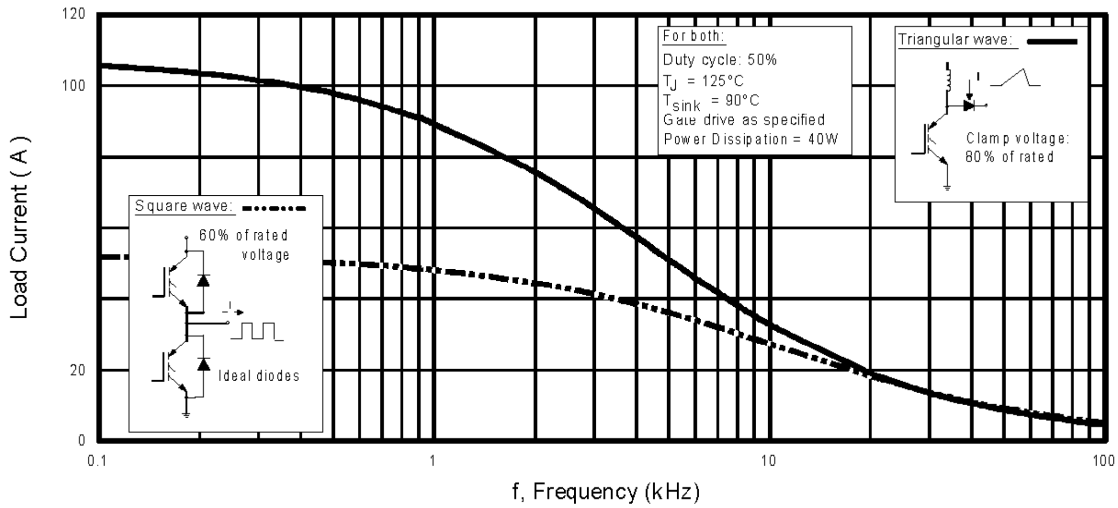


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

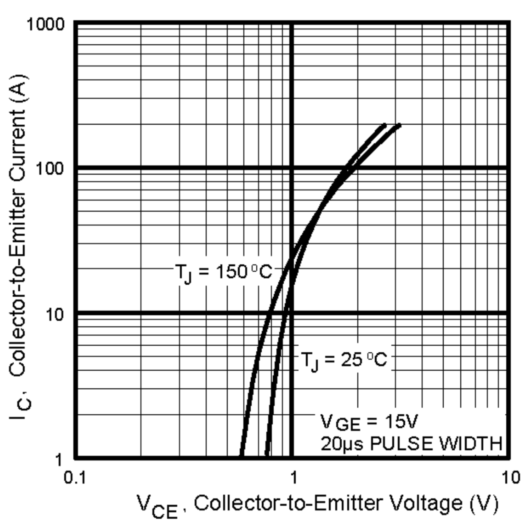


Fig. 2 - Typical Output Characteristics

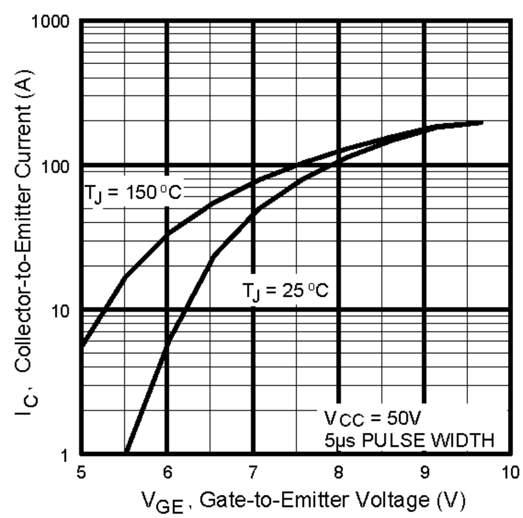


Fig. 3 - Typical Transfer Characteristics

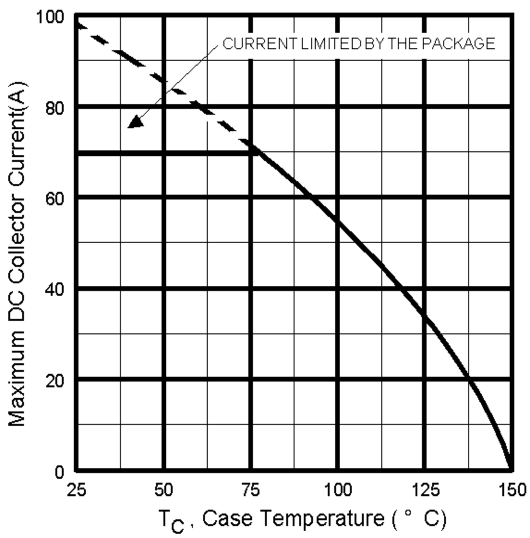


Fig. 4 - Maximum Collector Current vs. Case Temperature

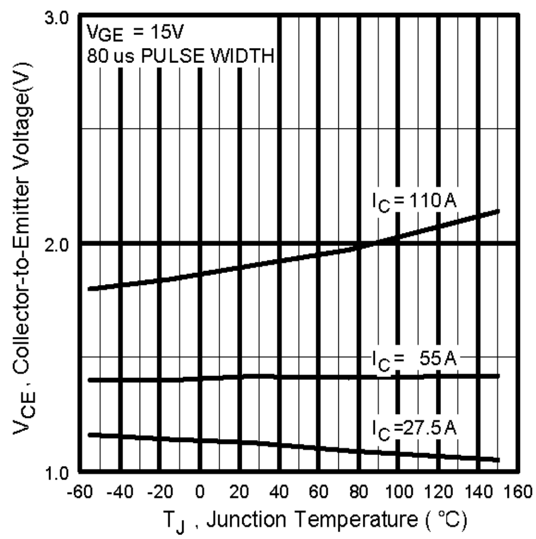


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

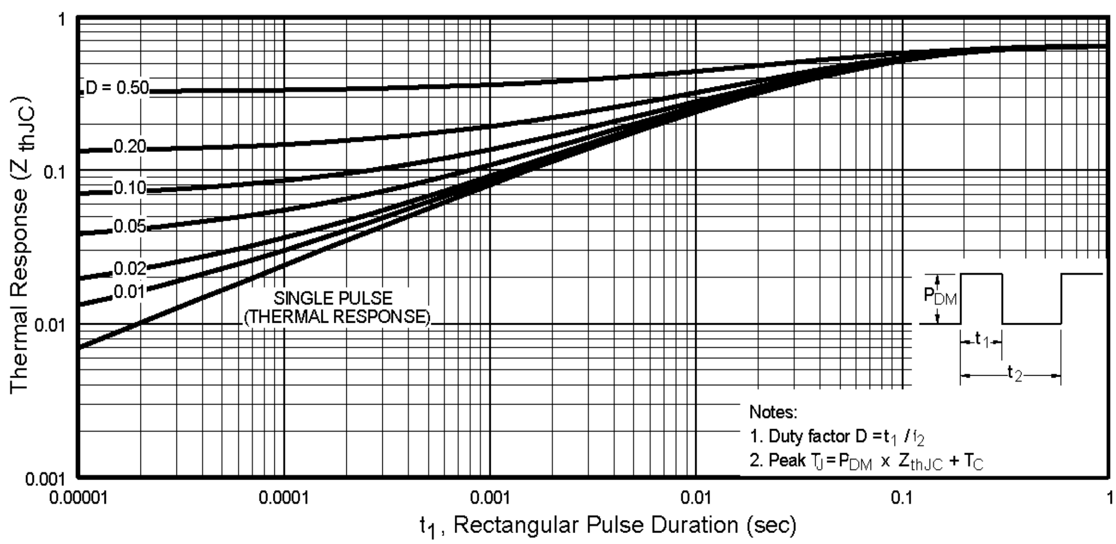


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

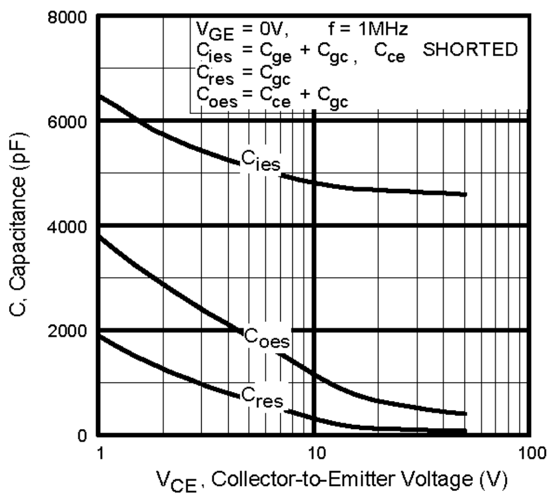


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

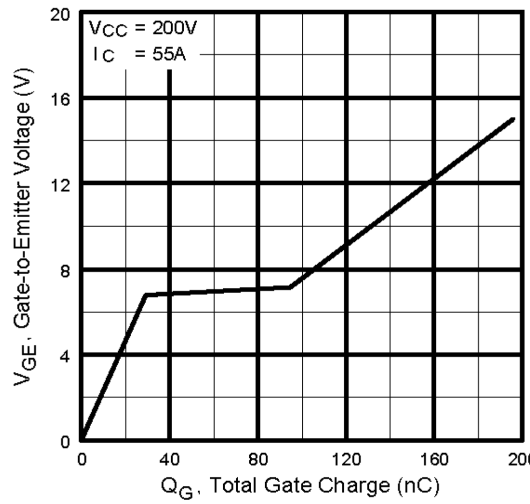


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

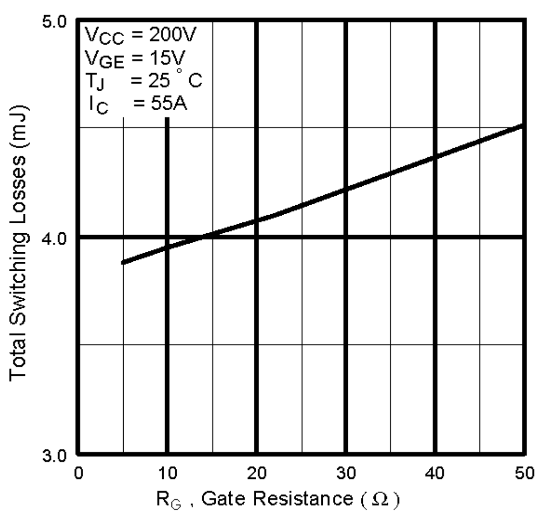


Fig. 9 - Typical Switching Losses vs. Gate Resistance

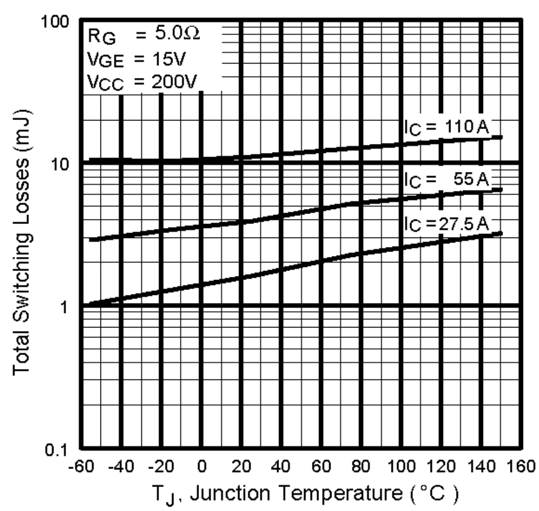


Fig. 10 - Typical Switching Losses vs. Junction Temperature

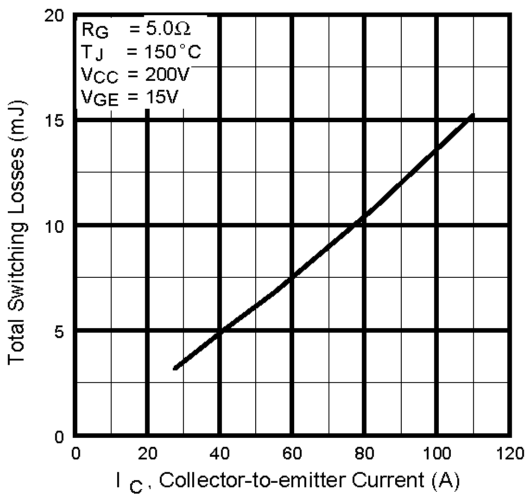


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

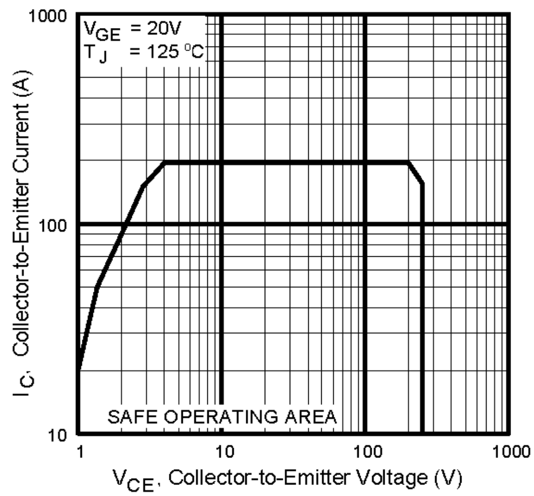
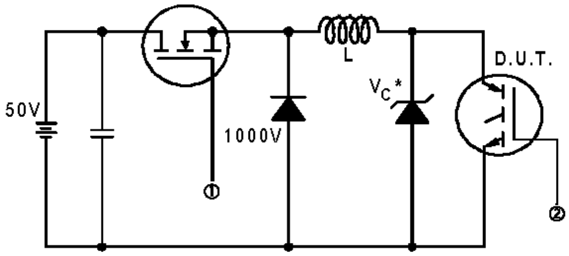


Fig. 12 - Turn-Off SOA



* Driver same type as D.U.T.; Vc = 80% of Vce(max)
* Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated Id.

Fig. 13a - Clamped Inductive Load Test Circuit

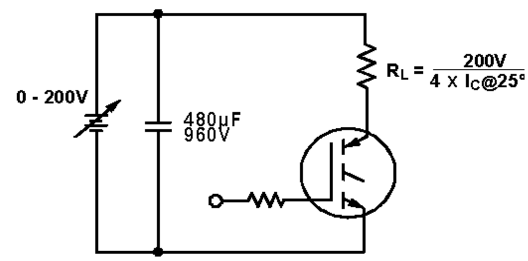


Fig. 13b - Pulsed Collector Current Test Circuit

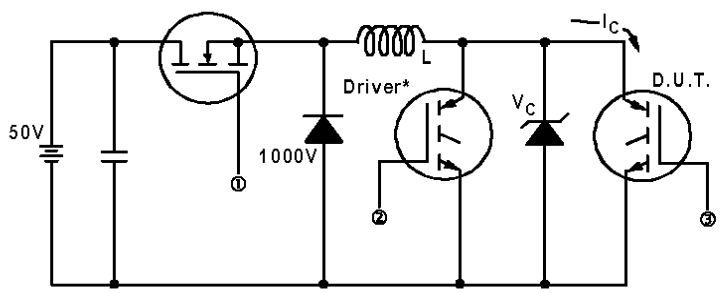


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 200V**

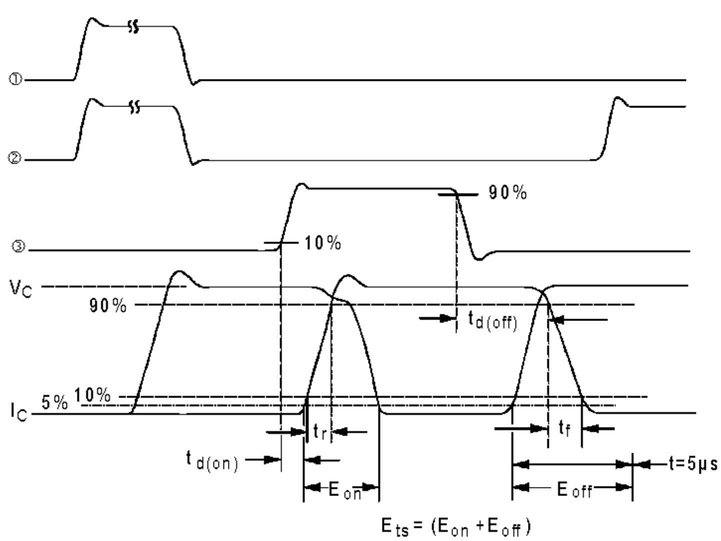
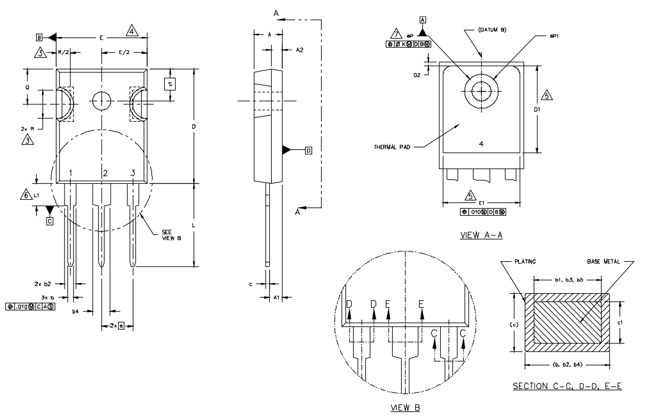


Fig. 14b - Switching Loss Waveforms

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENISONS D1 & E1
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF 154" [3 91]
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN	MAX	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	020	030	0.51	0.76	
E	602	625	15.29	15.87	4
E1	540	–	15.72	–	
e	215 BSC		5.46 BSC		
Øk	010		2.54		
L	.559	.634	14.20	16.10	
L1	146	.169	3.71	4.29	
N	3		7.62 BSC		
ØP	.140	.144	3.56	3.66	
ØP1	–	.275	–	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1 – GATE
2.– DRAIN
3.– SOURCE
4 – DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3 – EMITTER
4.– COLLECTOR

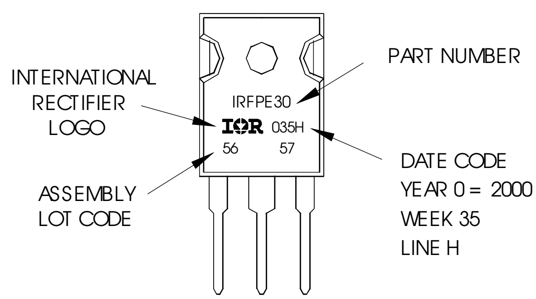
DIODES

1 – ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

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http://www.irf.com/package/