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IRG4PC50SDPbF

INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE

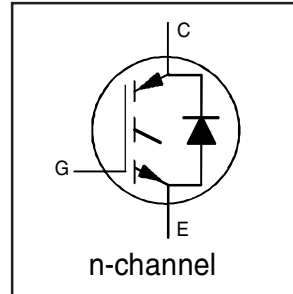
Standard Speed CoPack IGBT

Features

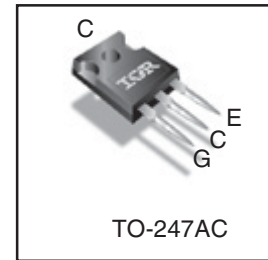
- Standard: Optimized for minimum saturation voltage and low operating frequencies (<1kHz)
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard TO-247AC package

Benefits

- Generation -4 IGBT's offer highest efficiencies available
- IGBT's optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBT's. Minimized recovery characteristics require less/no snubbing



$V_{CES} = 600V$
$V_{CE(on) typ.} = 1.28V$
@ $V_{GE} = 15V, I_C = 41A$



G	C	E
Gate	Collector	Emitter

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	70	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	41	
I_{CM}	Pulsed Collector Current ①	140	
I_{LM}	Clamped Inductive Load Current ②	140	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	25	
I_{FM}	Diode Maximum Forward Current ③	280	
V_{GE}	Continuous Gate-to-Emitter Voltage	± 20	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	200	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	78	
T_J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T_{STG}			
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT)	—	—	0.64	°C/W
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode)	—	—	0.83	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$	
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.75	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 1mA (25^\circ\text{C}-150^\circ\text{C})$	
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.28	1.36	V	$I_C = 41A, V_{GE} = 15V, T_J = 25^\circ\text{C}$	2
		—	1.62	—		$I_C = 80A, V_{GE} = 15V, T_J = 25^\circ\text{C}$	
		—	1.25	—		$I_C = 41A, V_{GE} = 15V, T_J = 150^\circ\text{C}$	
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	$V_{CE} = V_{GE}, I_C = 250\mu A$	3
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage temp. coefficient	—	-9.3	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 250\mu A (25^\circ\text{C} - 150^\circ\text{C})$	
g_{fe}	Forward Transconductance	17	34	—	S	$V_{CE} = 100V, I_C = 41A$	
I_{CES}	Collector-to-Emitter Leakage Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$	
		—	—	2.0		$V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$	
		—	—	1000		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$	
V_{FM}	Diode Forward Voltage Drop	—	1.3	1.7	V	$I_F = 25A$	13
		—	1.2	1.5		$I_F = 25A, T_J = 150^\circ\text{C}$	
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$	

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
Q_g	Total Gate Charge (turn-on)	—	180	280	nC	$I_C = 41A$ $V_{GE} = 15V$ $V_{CC} = 400V$	8
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	24	37			
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	61	92			
E_{on}	Turn-On Switching Loss	—	0.72	—	mJ	$I_C = 41A, V_{CC} = 480V, V_{GE} = 15V$ $R_G = 5.0\Omega, T_J = 25^\circ\text{C}$ Energy losses include tail & diode reverse recovery	18a, 18b
E_{off}	Turn-Off Switching Loss	—	8.27	—			18c
E_{total}	Total Switching Loss	—	8.99	13			
$t_{d(on)}$	Turn-On delay time	—	33	—	ns	$I_C = 41A, V_{CC} = 480V, V_{GE} = 15V$ $R_G = 5.0\Omega, L = 200\mu H, T_J = 25^\circ\text{C}$	18a, 18b
t_r	Rise time	—	30	—			18c
$t_{d(off)}$	Turn-Off delay time	—	650	980			
t_f	Fall time	—	400	600			
E_{total}	Total Switching Loss	—	15	—	mJ	$I_C = 41A, V_{CC} = 480V, V_{GE} = 15V$ $R_G = 5.0\Omega, L = 200\mu H$ $T_J = 150^\circ\text{C}$	18a, 18b
$t_{d(on)}$	Turn-On delay time	—	31	—			18c
t_r	Rise time	—	31	—			
$t_{d(off)}$	Turn-Off delay time	—	1080	—			
t_f	Fall time	—	620	—			
C_{ies}	Input Capacitance	—	4100	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0Mhz$	7
C_{oes}	Output Capacitance	—	250	—			
C_{res}	Reverse Transfer Capacitance	—	48	—			
t_{rr}	Diode Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	14
		—	105	160		$T_J = 125^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	18a, 18d
I_{rr}	Peak Reverse Recovery Current	—	4.5	10	A	$T_J = 25^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	15
		—	8.0	15		$T_J = 125^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	18a, 18d
Q_{rr}	Peak Reverse Recovery Current	—	112	375	nC	$T_J = 25^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	16
		—	420	1200		$T_J = 125^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	18a, 18d
$di_{(rec)M}/dt$	Peak Rate of Fall of Recovery During t_b	—	250	—	A/ μs	$T_J = 25^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	17
		—	160	—		$T_J = 125^\circ\text{C}, V_R = 200V, I_F = 25A, di/dt=200A/\mu s$	

Notes:

- ① Repetitive rating: $V_{GE}=15V$; pulse width limited by maximum junction temperature. (See figure 20)
- ② $V_{CC}=80\%(V_{CES}), V_{GE}=15V, R_G = 5.0\Omega$. (See figure 19)
- ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.

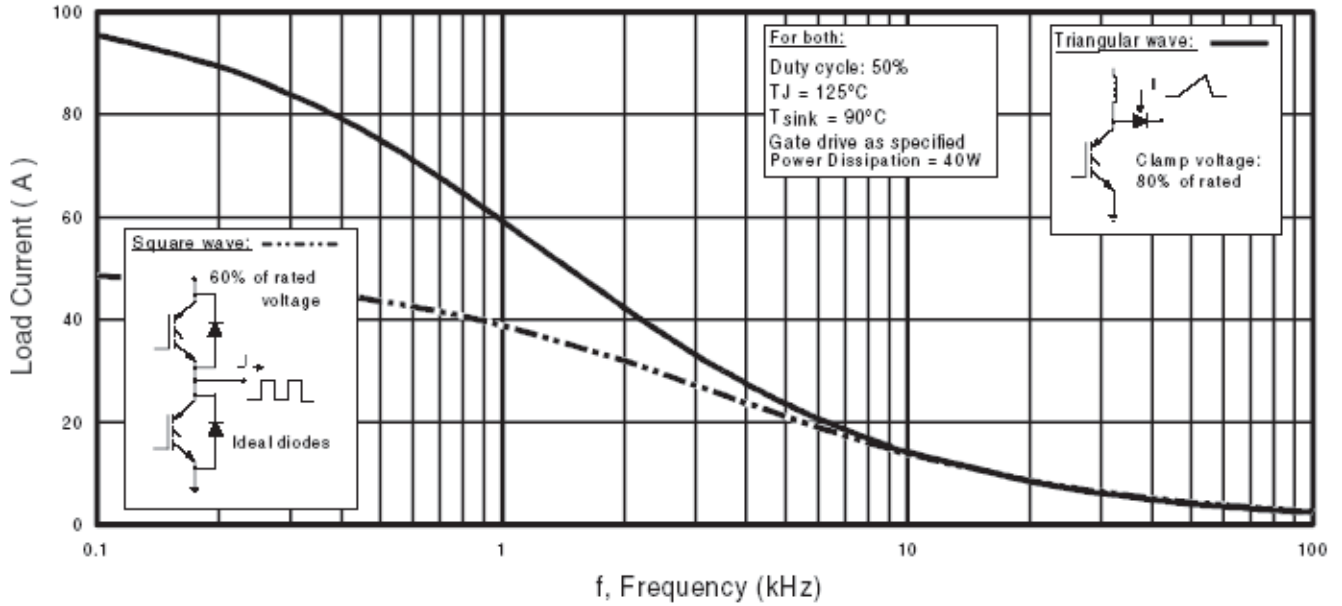


Fig. 1 - Typical Load Current vs. Frequency
 (Load Current = I_{RMS} of fundamental)

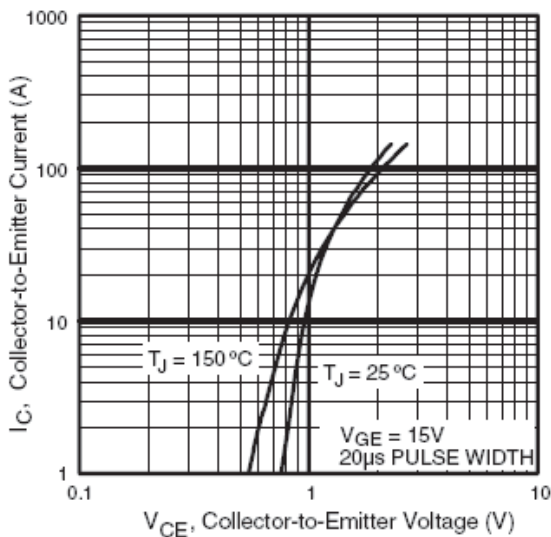


Fig. 2 - Typical Output Characteristics

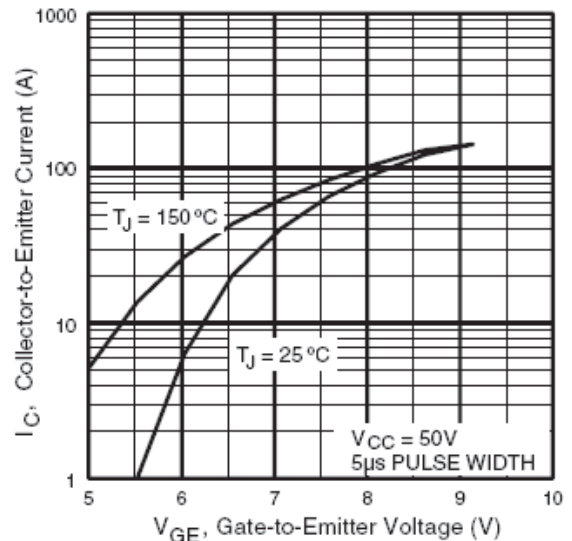


Fig. 3 - Typical Transfer Characteristics

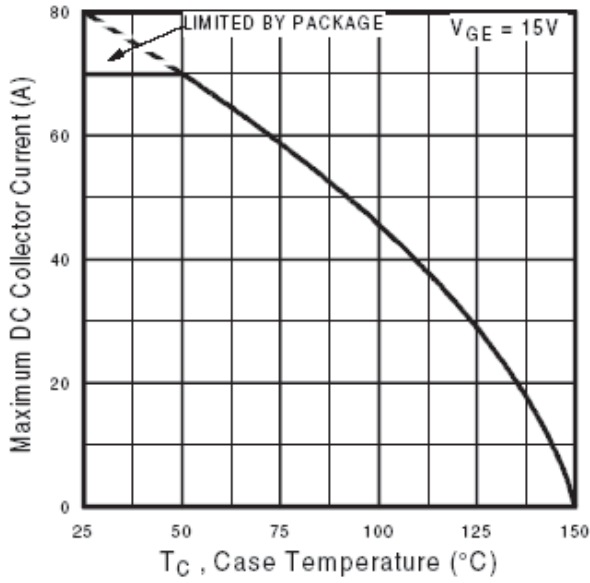


Fig. 4 - Maximum Collector Current vs. Case Temperature

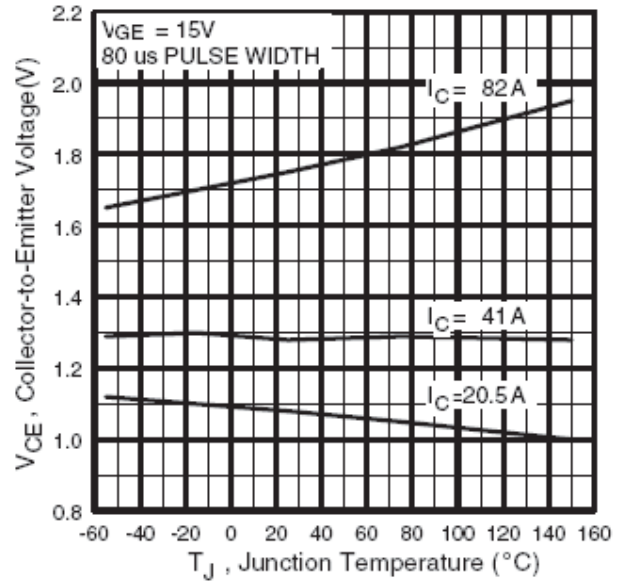


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

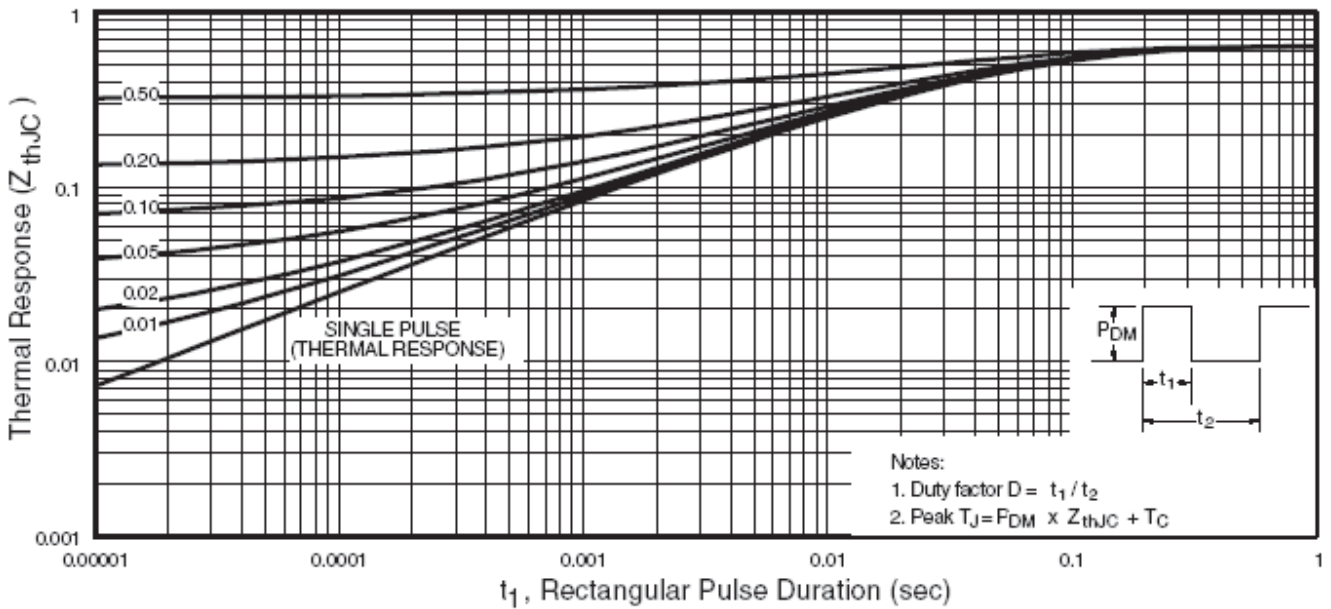


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

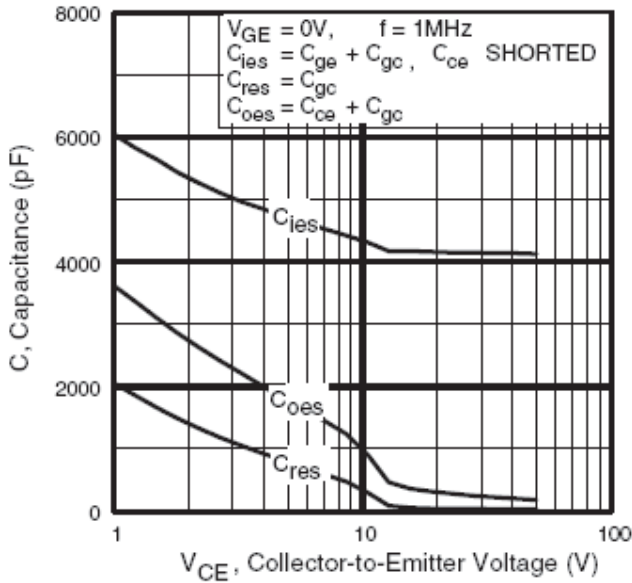


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

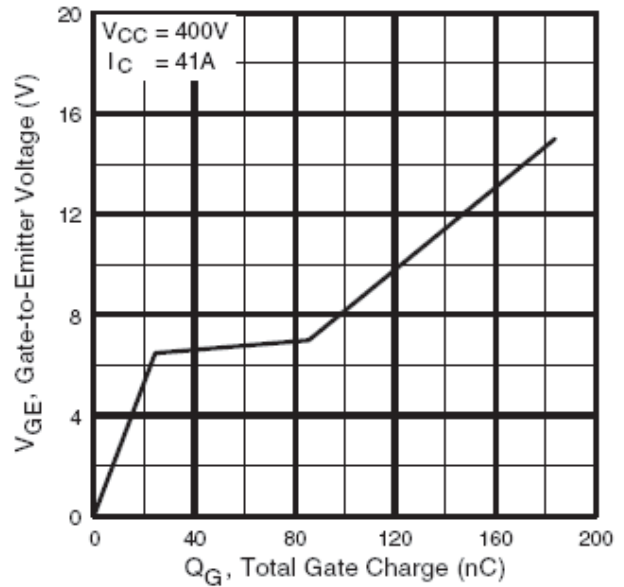


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

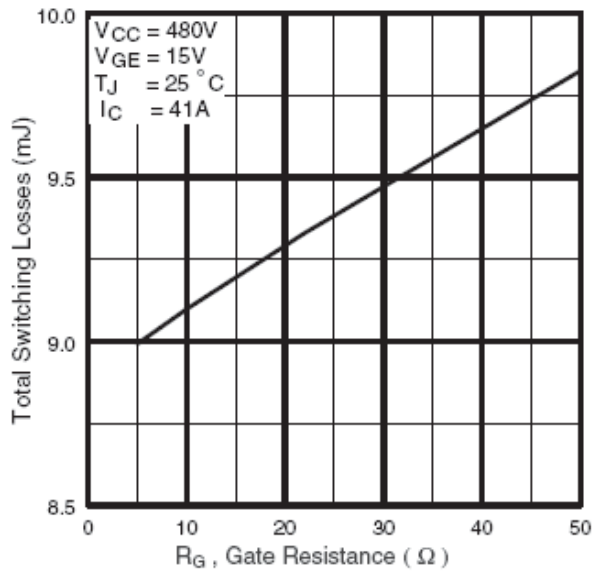


Fig. 9 - Typical Switching Losses vs. Gate Resistance

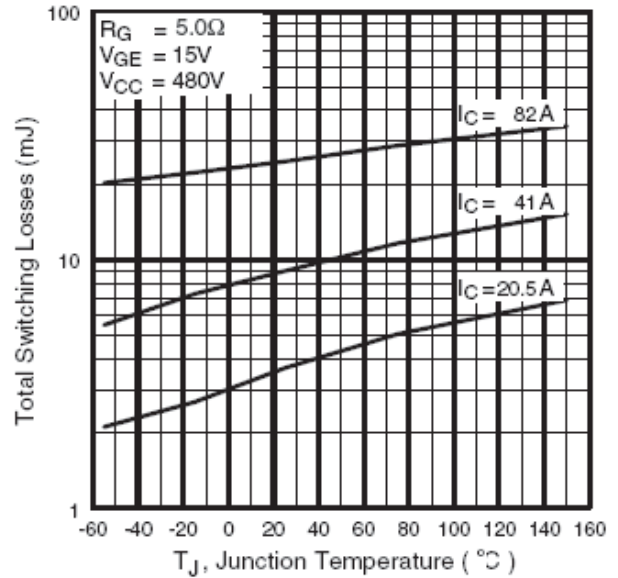


Fig. 10 - Typical Switching Losses vs. Junction Temperature

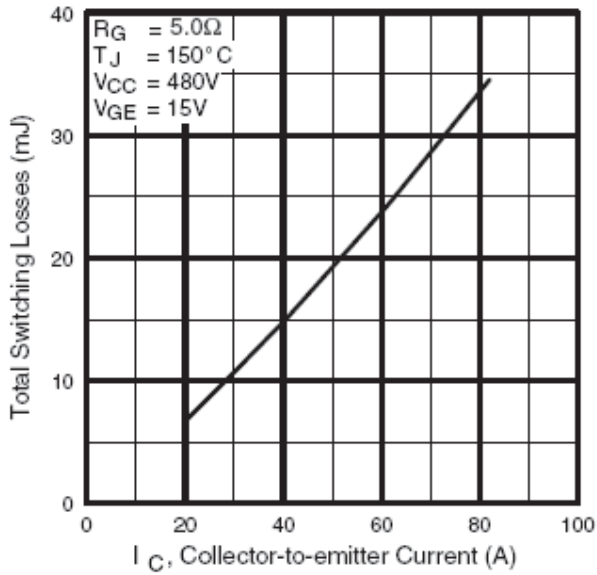


Fig. 11 - Typical Switching Losses vs. Collector-to-emitter Current

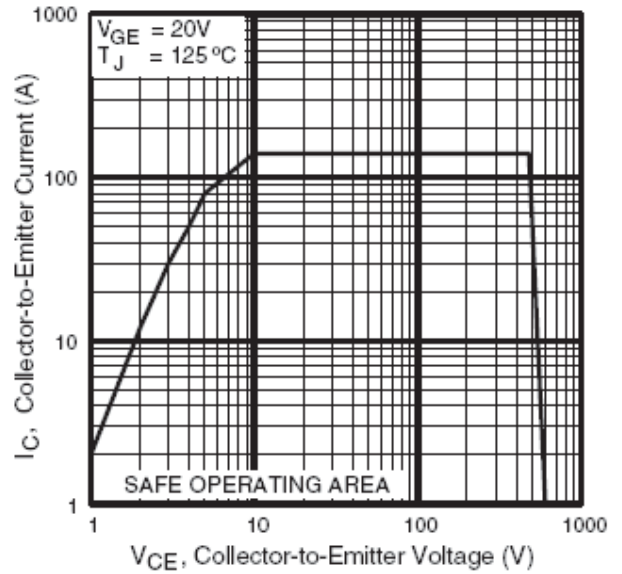


Fig. 12 - Turn-Off SOA

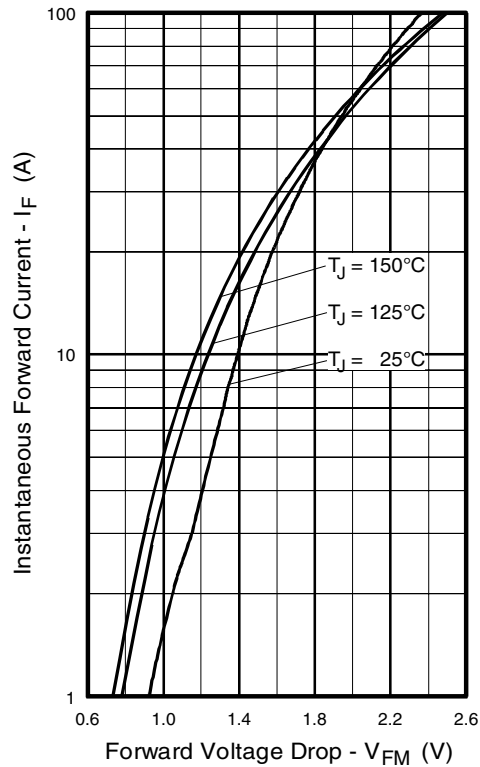


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

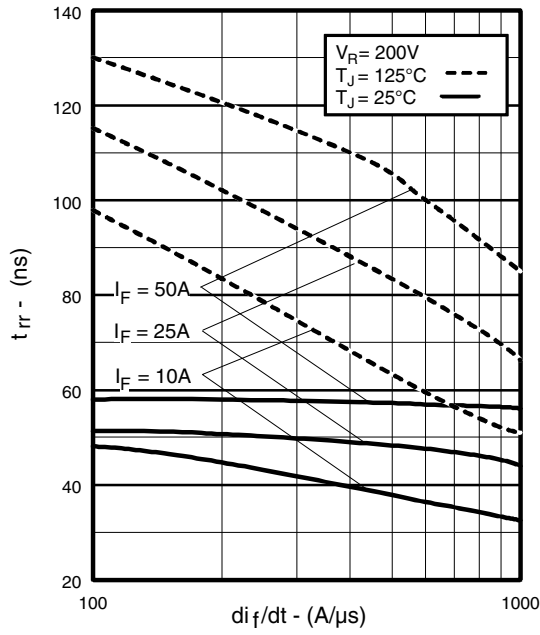


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

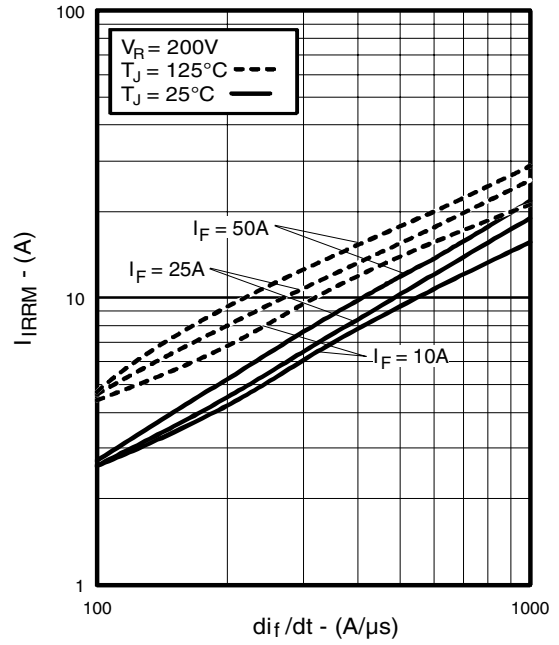


Fig. 15 - Typical Recovery Current vs. di_f/dt

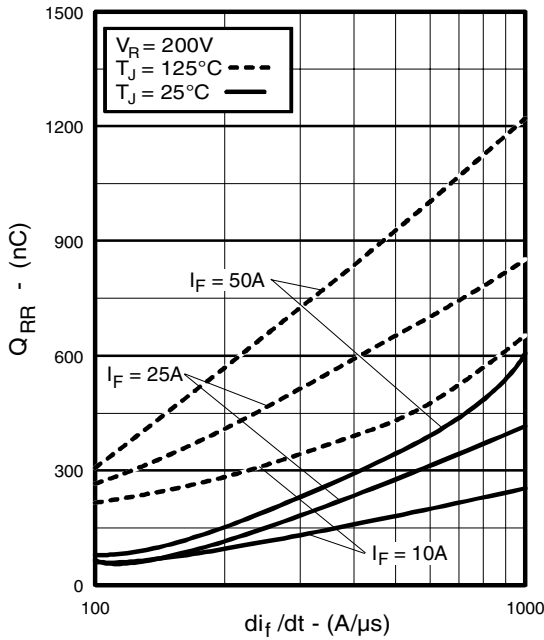


Fig. 16 - Typical Stored Charge vs. di_f/dt

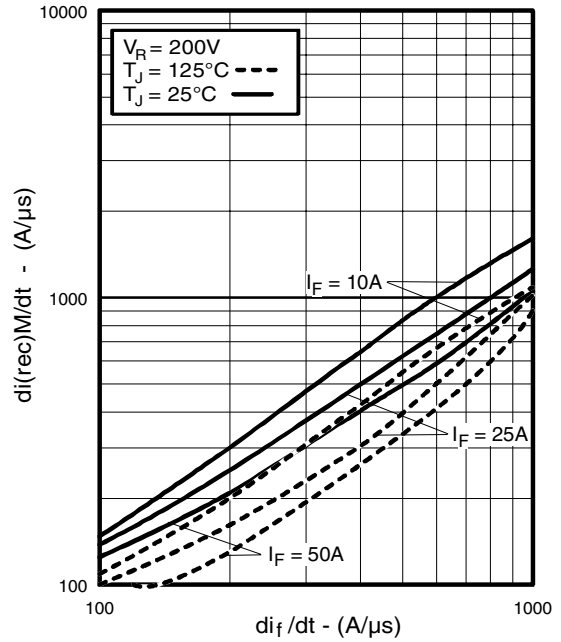


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

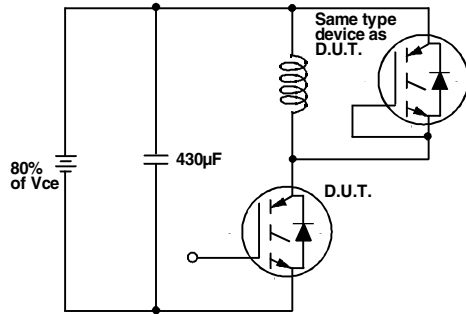


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

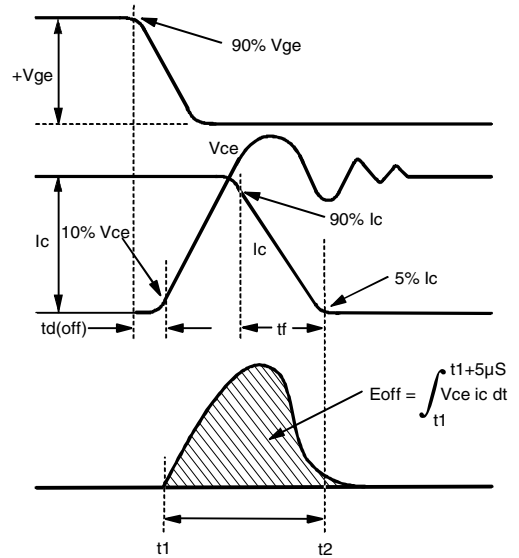


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

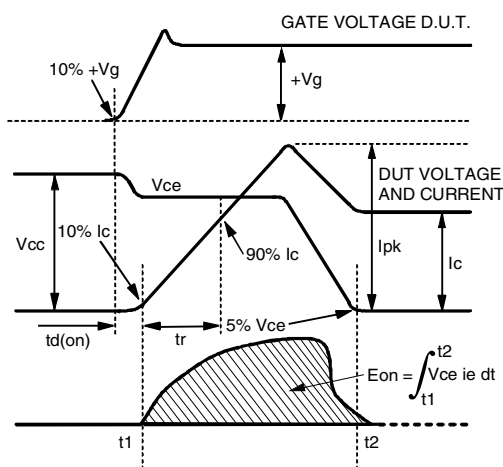


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

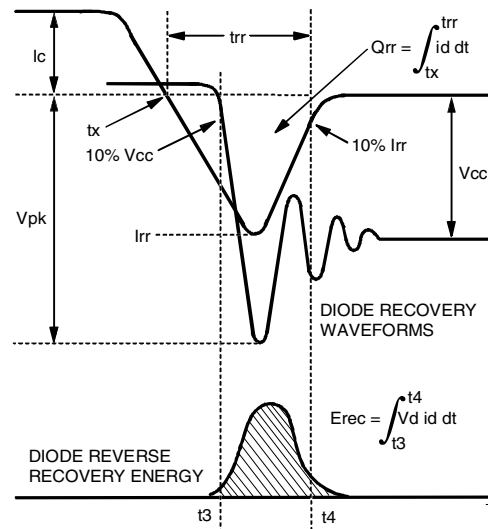


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

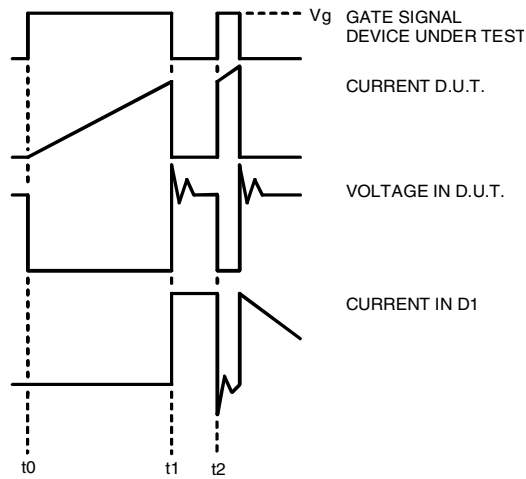


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

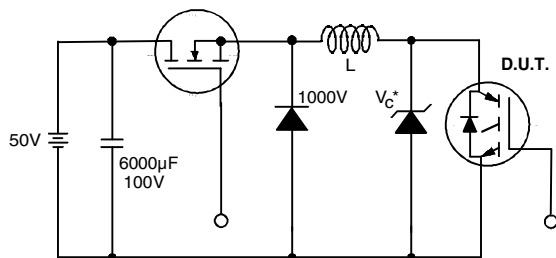


Figure 19. Clamped Inductive Load Test Circuit

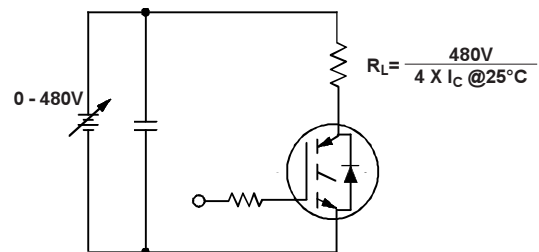
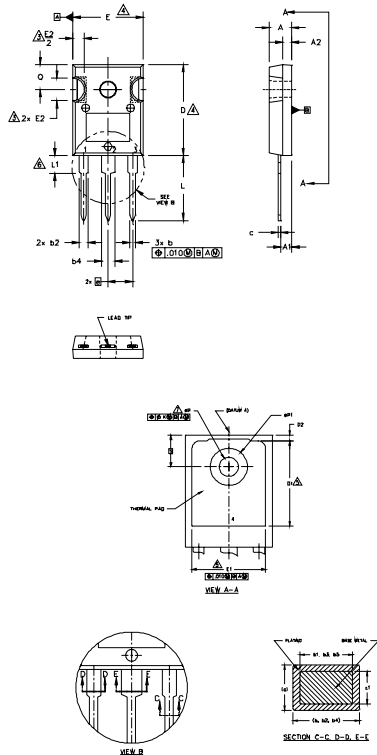


Figure 20. Pulsed Collector Current Test Circuit

IRG4PC50SDPbF

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN LI.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

IGBTs, CoPACK

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER
- 4 - COLLECTOR

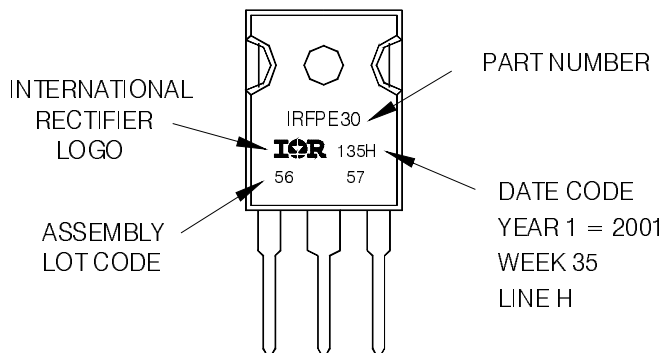
DIODES

- 1 - ANODE/OPEN
- 2 - CATHODE
- 3 - ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.