



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

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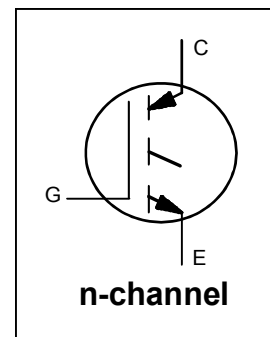
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**INSULATED GATE BIPOLAR TRANSISTOR**

|  |
|--|
| $V_{CES} = 600V$<br>$I_C = 30A, T_C = 100^\circ C$<br>$T_{J(max)} = 175^\circ C$<br>$V_{CE(on)} \text{ typ} = 1.65V @ I_C = 18A$ |
|--|



**Applications**

- Industrial Motor Drives
- Inverter
- UPS
- Welding

|          |           |          |
|----------|-----------|----------|
| <b>G</b> | <b>C</b>  | <b>E</b> |
| Gate     | Collector | Emitter  |

| Features  | Benefits  |
|---|---|
| Low $V_{CE(ON)}$ and switching losses               | High efficiency in a wide range of applications and switching frequencies                 |
| Square RBSOA and maximum junction temperature 175°C | Improved reliability due to rugged hard switching performance and higher power capability |
| Positive $V_{CE(ON)}$ temperature coefficient       | Excellent current sharing in parallel operation   |
| 5µs short circuit SOA                               | Enables short circuit protection scheme   |
| Lead-free, RoHS compliant                           | Environmentally friendly  |

| Base part number | Package Type | Standard Pack |          | Orderable part number |
|------------------|--------------|---------------|----------|-----------------------|
|                  |              | Form          | Quantity |                       |
| IRGC4630B        | Wafer        | Wafer         | 1        | IRGC4630B             |

**Mechanical Parameters**

|                                      |  |                 |
|--------------------------------------|--|-----------------|
| Die Size                             | 3.302 x 3.302                              | mm <sup>2</sup> |
| Minimum Street Width                 | 75   | µm              |
| Emitter Pad Size (Included Gate Pad) | See Die Drawing                            | mm <sup>2</sup> |
| Gate Pad Size                        | 0.5 x 0.6                                  |                 |
| Area Total / Active                  | 10.9 / 6.4                                 |                 |
| Thickness                            | 70   | µm              |
| Wafer Size                           | 150  | mm              |
| Notch Position                       | 0  | Degrees         |
| Maximum-Possible Chips per Wafer     | 1408pcs.                                   |                 |
| Passivation Front side               | Silicon Nitride                            |                 |
| Front Metal                          | Al, Si (4µm)                               |                 |
| Backside Metal                       | Al (1kA°), Ti (1kA°), Ni (4kA°), Ag (6kA°) |                 |
| Die Bond                             | Electrically conductive epoxy or solder    |                 |
| Reject Ink Dot Size                  | 0.25 mm diameter minimum                   |                 |

**Maximum Ratings**

|                | Parameter   | Max.        | Units            |
|----------------|---|-------------|------------------|
| $V_{CE}$       | Collector-Emitter Voltage, $T_J=25^\circ\text{C}$ | 600         | V                |
| $I_C$          | DC Collector Current                              | ①           | A                |
| $I_{LM}$       | Clamped Inductive Load Current ④                  | 72          | A                |
| $V_{GE}$       | Gate Emitter Voltage                              | $\pm 20$    | V                |
| $T_J, T_{STG}$ | Operating Junction and Storage Temperature        | -40 to +175 | $^\circ\text{C}$ |

**Static Characteristics (Tested on wafers) .  $T_J=25^\circ\text{C}$** 

|               | Parameter                              | Min. | Typ. | Max.      | Units         | Conditions   |
|---------------|--|------|------|-----------|---------------|--|
| $V_{(BR)CES}$ | Collector-to-Emitter Breakdown Voltage | 600  | —    | —         | V             | $V_{GE} = 0\text{V}, I_C = 100\mu\text{A}$ ⑤                   |
| $V_{CE(sat)}$ | Collector-to-Emitter Saturated Voltage | —    | 1.1  | 1.325     |               | $V_{GE} = 15\text{V}, I_C = 5\text{A}, T_J = 25^\circ\text{C}$ |
| $V_{GE(th)}$  | Gate-Emitter Threshold Voltage         | 4.0  | —    | 6.5       |               | $I_C = 500\mu\text{A}, V_{GE} = V_{CE}$                        |
| $I_{CES}$     | Zero Gate Voltage Collector Current    | —    | 2.0  | 25        | $\mu\text{A}$ | $V_{CE} = 600\text{V}, V_{GE} = 0\text{V}$                     |
| $I_{GES}$     | Gate Emitter Leakage Current           | —    | —    | $\pm 100$ | nA            | $V_{CE} = 0\text{V}, V_{GE} = \pm 20\text{V}$                  |

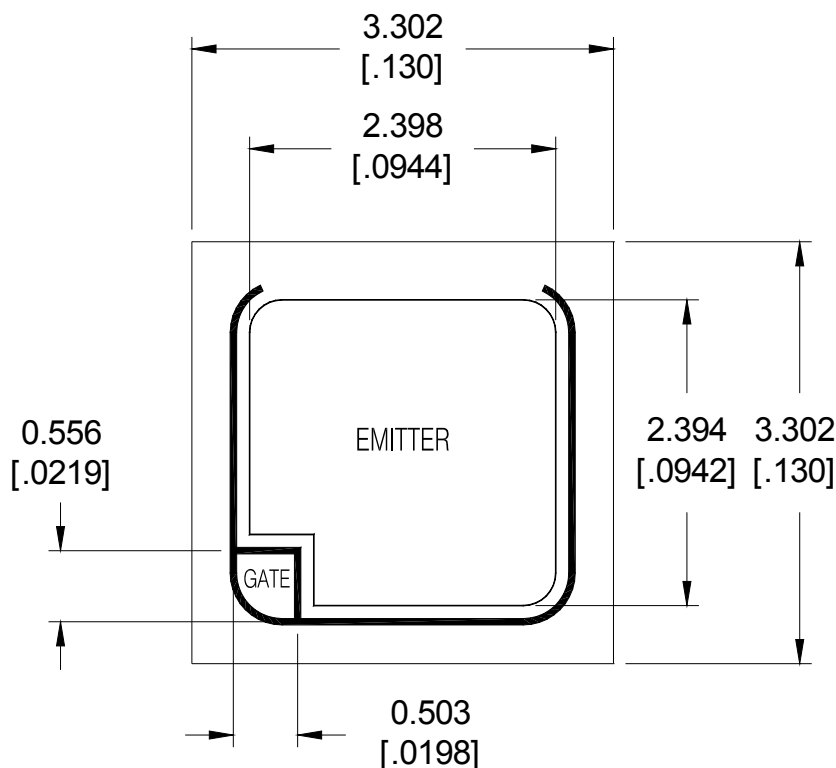
**Electrical Characteristics (Not subject to production test- Verified by design/characterization)**

|               | Parameter                              | Min.        | Typ. | Max. | Units         | Conditions  |
|---------------|--|-------------|------|------|---------------|---|
| $V_{CE(sat)}$ | Collector-to-Emitter Saturated Voltage | —           | 1.65 | 1.95 | V             | $V_{GE} = 15\text{V}, I_C = 18\text{A}, T_J = 25^\circ\text{C}$   |
|               |  | —           | 2.15 | —    |               | $V_{GE} = 15\text{V}, I_C = 18\text{A}, T_J = 175^\circ\text{C}$  |
| SCSOA         | Short Circuit Safe Operating Area      | 5           | —    | —    | $\mu\text{s}$ | $V_{GE}=15\text{V}, V_{CC}=400\text{V},$ ②<br>$R_G=22\Omega, V_P \leq 600\text{V}, T_J=150^\circ\text{C}$   |
| RBSOA         | Reverse Bias Safe Operating Area       | FULL SQUARE |      |      |               | $T_J = 175^\circ\text{C}, I_C = 72\text{A}$<br>$V_{CC} = 480\text{V}, V_P \leq 600\text{V}$<br>$R_g = 22\Omega, V_{GE} = +20\text{V to } 0\text{V}$ |
| $C_{ISS}$     | Input Capacitance                      | —           | 1043 | —    | pF            | $V_{GE} = 0\text{V}$  |
| $C_{OSS}$     | Output Capacitance                     | —           | 87   | —    |               | $V_{CE} = 30\text{V}$   |
| $C_{RSS}$     | Reverse Transfer Capacitance           | —           | 32   | —    |               | $f = 1.0\text{MHz}$   |
| $Q_g$         | Total Gate Charge (turn-on)            | —           | 35   | —    | nC            | $I_C = 18\text{A}$ ⑥  |
| $Q_{ge}$      | Gate-to-Emitter Charge (turn-on)       | —           | 10   | —    |               | $V_{GE} = 15\text{V}$   |
| $Q_{gc}$      | Gate-to-Collector Charge (turn-on)     | —           | 15   | —    |               | $V_{CC} = 400\text{V}$  |

**Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)**

|              | Parameter           | Min. | Typ. | Max. | Units | Conditions ③  |
|--------------|---------------------|------|------|------|-------|---|
| $t_{d(on)}$  | Turn-On delay time  | —    | 40   | —    | ns    | $I_C = 18\text{A}, V_{CC} = 400\text{V}$<br>$R_G = 22\Omega, V_{GE}=15\text{V}, L=200\mu\text{H}$<br>$T_J = 25^\circ\text{C}$   |
| $t_r$        | Rise time           | —    | 25   | —    |       |   |
| $t_{d(off)}$ | Turn-Off delay time | —    | 105  | —    |       |   |
| $t_f$        | Fall time           | —    | 25   | —    |       |   |
| $t_{d(on)}$  | Turn-On delay time  | —    | 40   | —    |       | $I_C = 18\text{A}, V_{CC} = 400\text{V}$<br>$R_G = 22\Omega, V_{GE}=15\text{V}, L= 200\mu\text{H}$<br>$T_J = 175^\circ\text{C}$ |
| $t_r$        | Rise time           | —    | 25   | —    |       |   |
| $t_{d(off)}$ | Turn-Off delay time | —    | 120  | —    |       |   |
| $t_f$        | Fall time           | —    | 40   | —    |       |   |

# Die Drawing


**NOTES:**

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:  
 S = SOURCE    SK = SOURCE KELVIN    E = EMITTER  
 G = GATE      IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:  
 BONDING PADS:    < 0.635 TOLERANCE = +/- 0.013  
                     WIDTH            < [.0250] TOLERANCE = +/- [.0005]  
                     &                    > 0.635 TOLERANCE = +/- 0.025  
                     LENGTH           > [.0250] TOLERANCE = +/- [.0010]  
 OVERALL DIE:    < 1.270 TOLERANCE = +/- 0.102  
                     WIDTH            < [.050] TOLERANCE = +/- [.004]  
                     &                    > 1.270 TOLERANCE = +/- 0.203  
                     LENGTH           > [.050] TOLERANCE = +/- [.008]
5. DIE THICKNESS = 0.070 [.0028]    TOL: = 0.007 [.0003]

**Notes:**

- ① The current in the application is limited by  $T_{JMax}$  and the thermal properties of the assembly.
- ② Not subject to production test- Verified by design / characterization.
- ③ Values influenced by parasitic L and C in measurement.
- ④  $V_{CC} = 80\% (V_{CES})$ ,  $V_{GE} = 20V$ ,  $L = 200\mu H$ ,  $R_G = 22\Omega$ .
- ⑤ Refer to AN-1086 for guidelines for measuring  $V_{(BR)CES}$  safely
- ⑥ Die Level Characterization.

### Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

### Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

### Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

### Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

### Further Information

For further information please contact your local IR Sales office or email your enquiry to <http://die.irf.com>

Data and specifications subject to change without notice.  
This product has been designed and qualified for Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IOR** Rectifier

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