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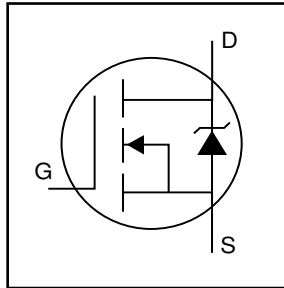
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## IRL2203S

### HEXFET<sup>®</sup> Power MOSFET

- Logic-Level Gate Drive
- Surface Mount
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



$$V_{DSS} = 30V$$

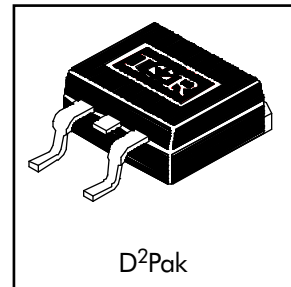
$$R_{DS(on)} = 0.007\Omega$$

$$I_D = 100A\text{⑤}$$

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V\text{⑥}$	100⑤	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V\text{⑥}$	71	
$I_{DM}$	Pulsed Drain Current ①⑥	400	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	130	W
	Linear Derating Factor	0.83	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②⑥	390	mJ
$I_{AR}$	Avalanche Current ①	60	A
$E_{AR}$	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	1.2	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

### Thermal Resistance

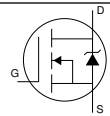
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted, steady-state)**	—	40	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>⑥</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.007		V <sub>GS</sub> = 10V, I <sub>D</sub> = 60A <sup>④</sup>
		—	—	0.01		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 50A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	47	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 60A <sup>⑥</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	110	nC	I <sub>D</sub> = 60A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	31		V <sub>DS</sub> = 24V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	57		V <sub>GS</sub> = 4.5V, See Fig. 6 and 13 <sup>④⑥</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—		V <sub>DD</sub> = 15V
t <sub>r</sub>	Rise Time	—	210	—	ns	I <sub>D</sub> = 60A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	29	—		R <sub>G</sub> = 1.8Ω, V <sub>GS</sub> = 4.5V
t <sub>f</sub>	Fall Time	—	54	—		R <sub>D</sub> = 0.25Ω, See Fig. 10 <sup>④⑥</sup>
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	3500	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1400	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	690	—		f = 1.0MHz, See Fig. 5 <sup>⑥</sup>

## Source-Drain Ratings and Characteristics

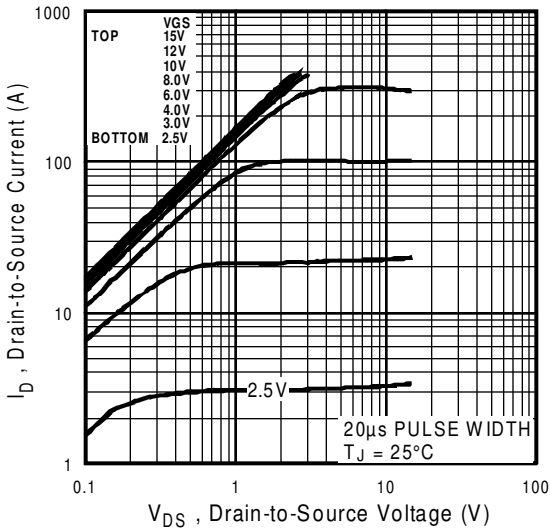
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	100 <sup>⑤</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 60A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	94	140	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 60A
Q <sub>rr</sub>	Reverse Recovery Charge	—	280	410	nC	di/dt = 100A/μs <sup>④⑥</sup>



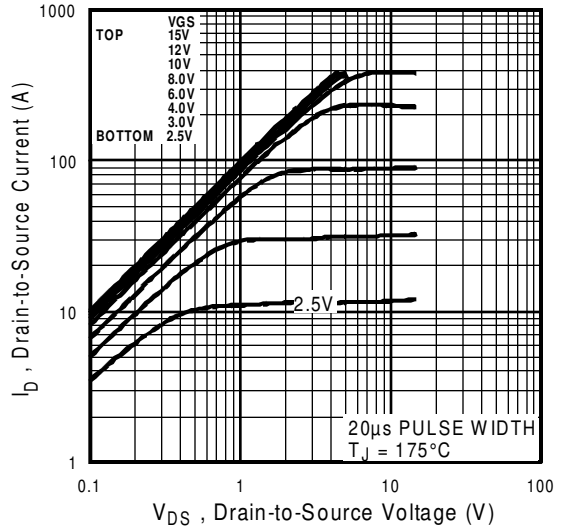
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 15V, starting T<sub>J</sub> = 25°C, L = 220μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 60A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 60A, di/dt ≤ 140A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4
- ⑥ Uses IRL2203N data and test conditions.

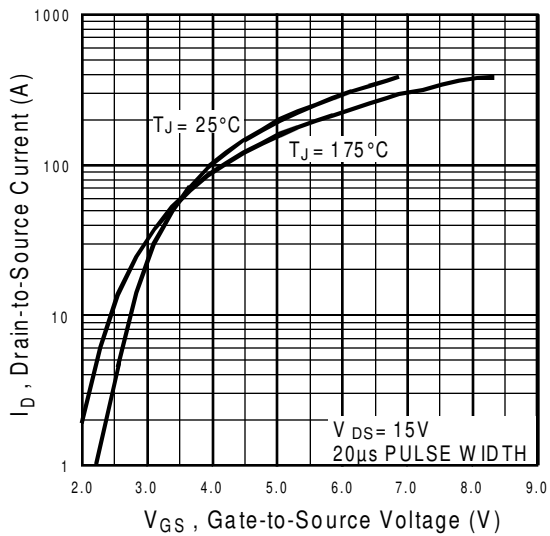
\*\* When mounted on FR-4 board using minimum recommended footprint.  
For recommended footprint and soldering techniques refer to application note #AN-994.



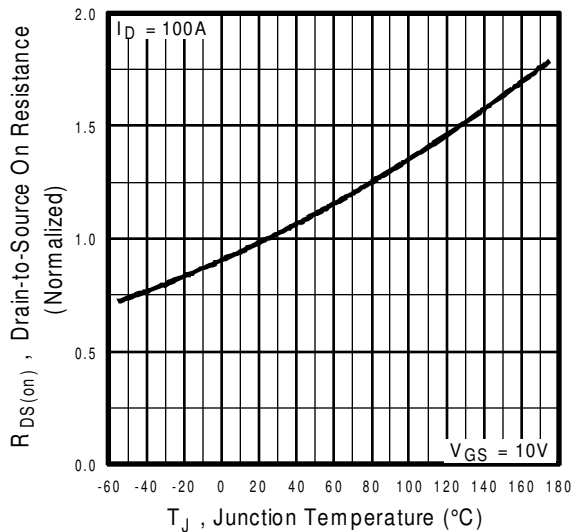
**Fig 1.** Typical Output Characteristics,  
 $T_J = 25^\circ\text{C}$



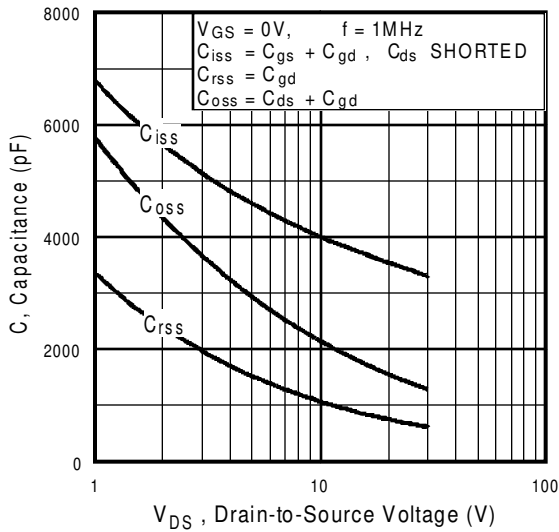
**Fig 2.** Typical Output Characteristics,  
 $T_J = 175^\circ\text{C}$



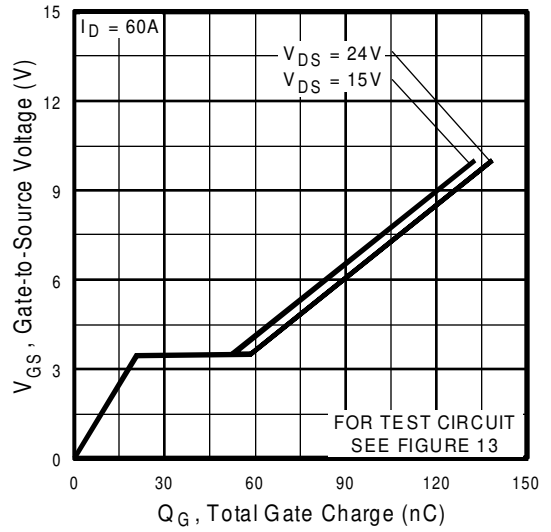
**Fig 3.** Typical Transfer Characteristics



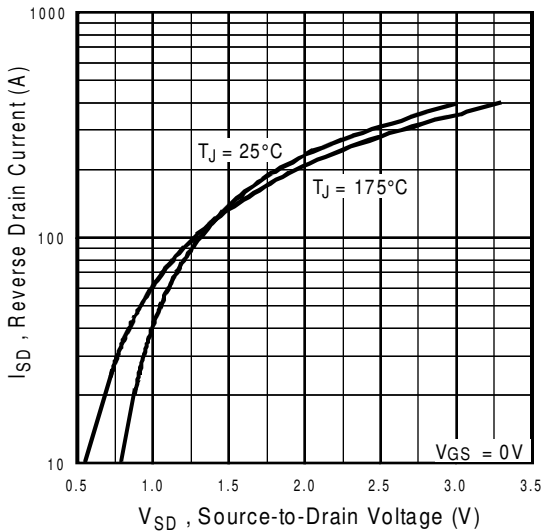
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



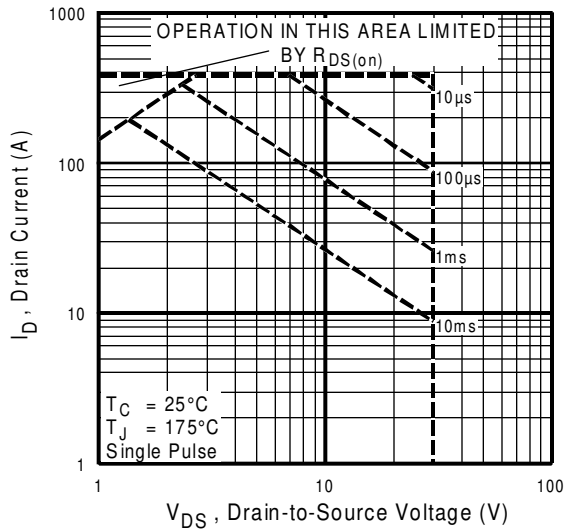
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



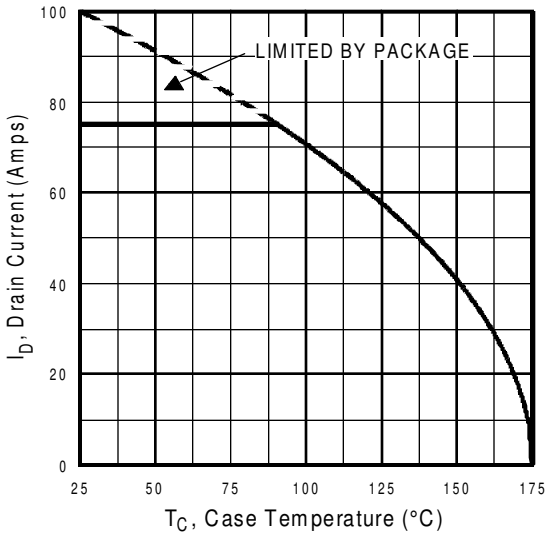
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



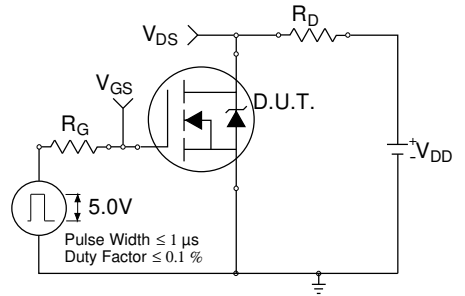
**Fig 7.** Typical Source-Drain Diode Forward Voltage



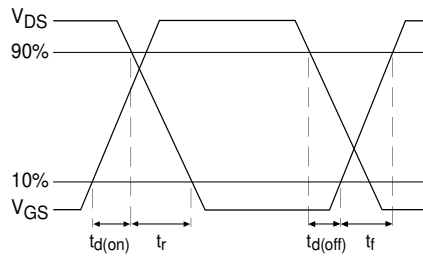
**Fig 8.** Maximum Safe Operating Area



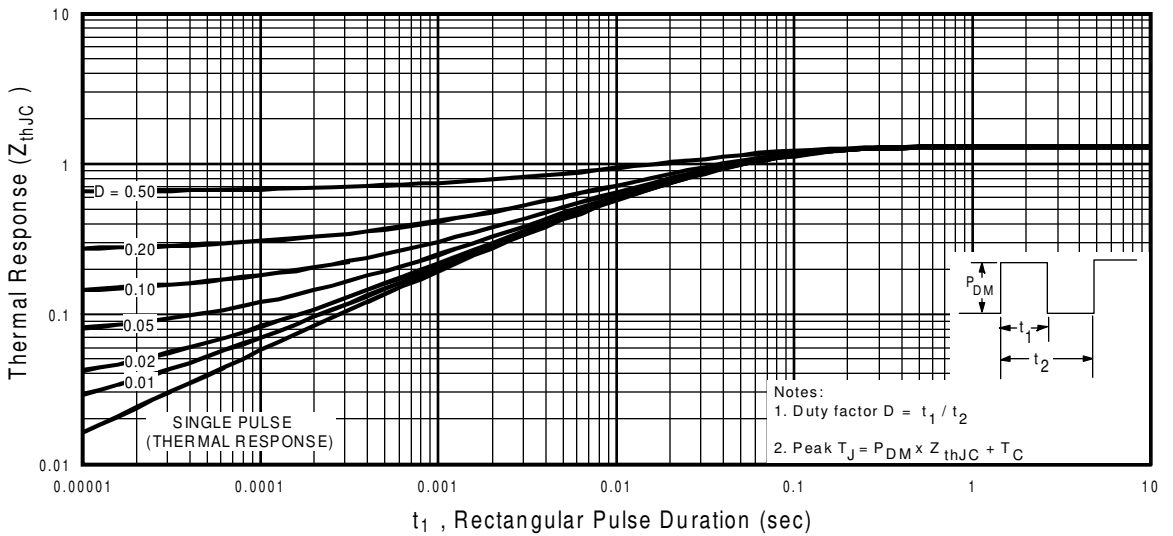
**Fig 9.** Maximum Drain Current Vs. Case Temperature



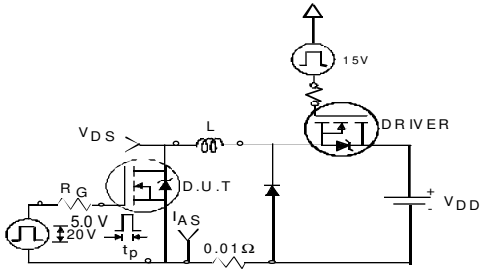
**Fig 10a.** Switching Time Test Circuit



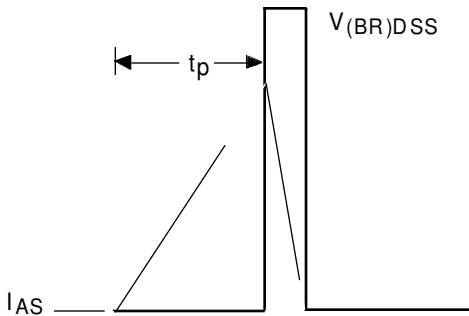
**Fig 10b.** Switching Time Waveforms



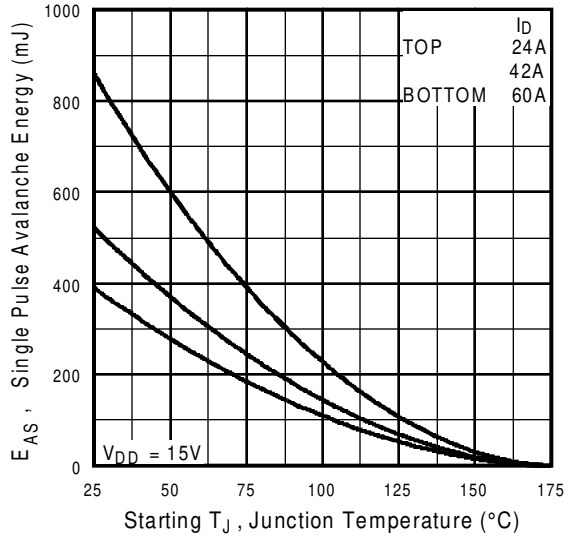
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



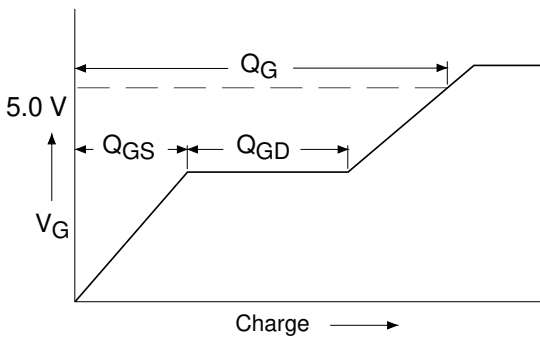
**Fig 12a.** Unclamped Inductive Test Circuit



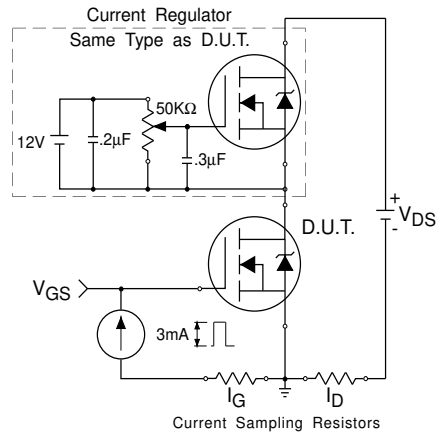
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

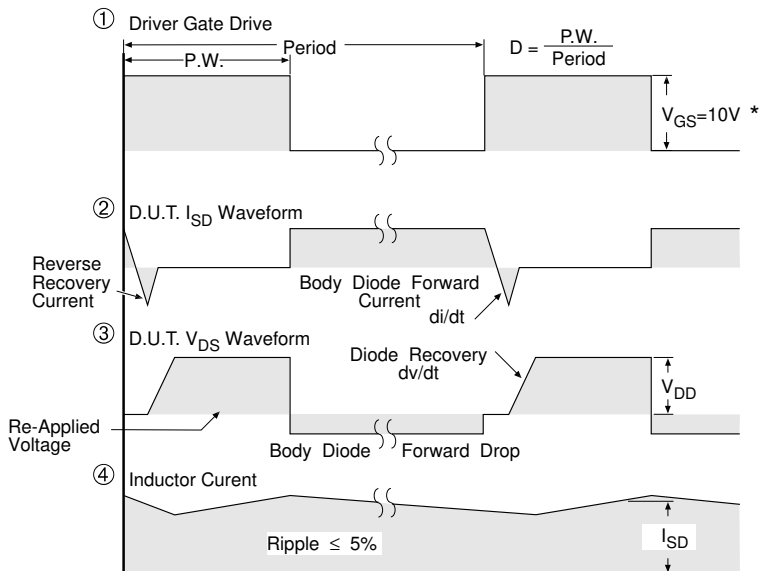
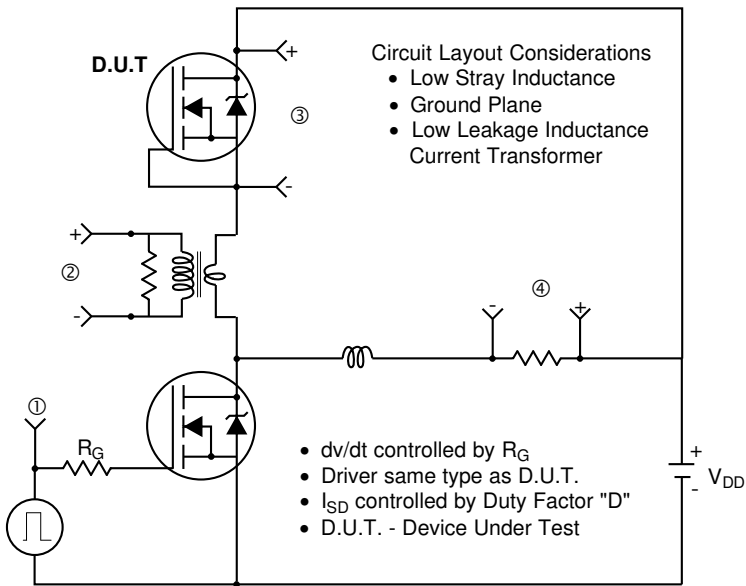


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



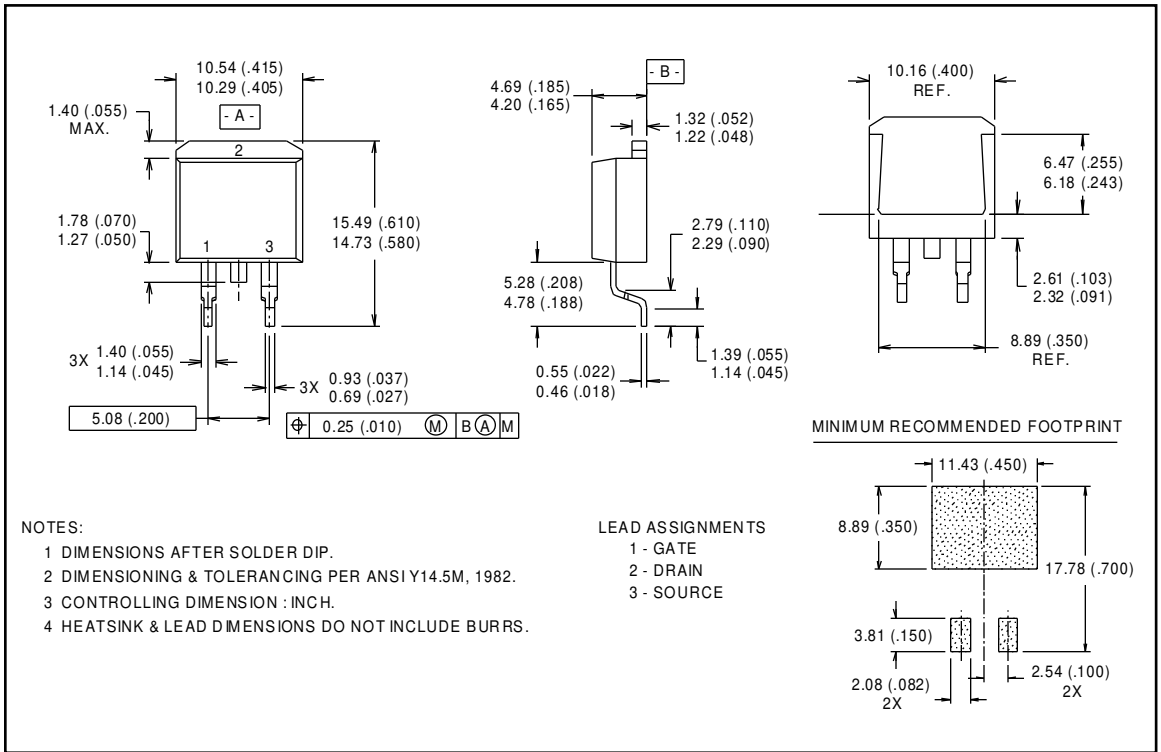
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

# IRL2203S

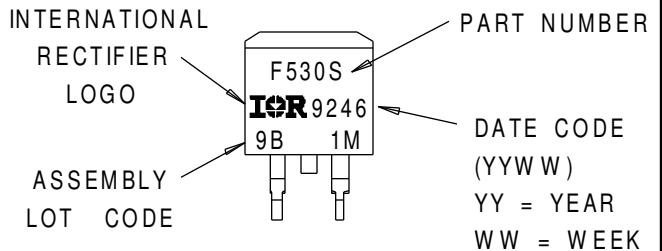
## Package Outline — D<sup>2</sup>Pak

Dimensions are shown in millimeters (inches)



## Part Marking

EXAMPLE : THIS IS AN IRF530S  
WITH ASSEMBLY  
LOT CODE 9B1M



Tape & Reel — D<sup>2</sup>Pak

Dimensions are shown in millimeters (inches)

