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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

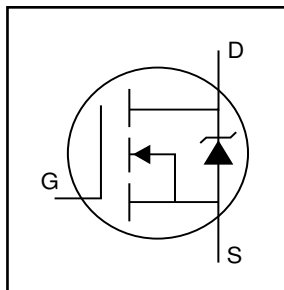
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



- Logic-Level Gate Drive
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

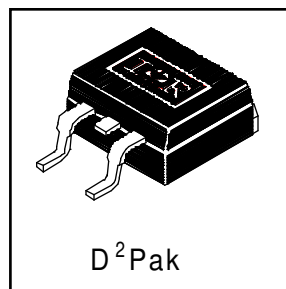


$V_{DSS} = 30V$
$R_{DS(on)} = 0.04\Omega$
$I_D = 24A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	24	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	17	
I_{DM}	Pulsed Drain Current ①	96	
$P_D @ T_C = 25^\circ C$	Power Dissipation	45	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②⑤	77	mJ
I_{AR}	Avalanche Current①	14	A
E_{AR}	Repetitive Avalanche Energy①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	3.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

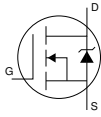
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady-state)**	—	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.030	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	$V_{GS} = 10V, I_D = 14A$ ④
		—	—	0.060		$V_{GS} = 4.5V, I_D = 12A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	6.4	—	—	S	$V_{DS} = 25V, I_D = 14A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	15	nC	$I_D = 14A$
Q_{gs}	Gate-to-Source Charge	—	—	4.6		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.3		$V_{GS} = 4.5V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	8.5	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	140	—		$I_D = 14A$
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		$R_G = 12\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	20	—		$R_D = 1.0\Omega$, See Fig. 10 ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	450	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	210	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	110	—		$f = 1.0\text{MHz}$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	24	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	96		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 14A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	65	97	ns	$T_J = 25^\circ\text{C}, I_F = 14A$
Q_{rr}	Reverse Recovery Charge	—	140	210	nC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $V_{DD} = 15V$, starting $T_J = 25^\circ\text{C}$, $L = 570\mu H$
 $R_G = 25\Omega$, $I_{AS} = 14A$. (See Figure 12)

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

③ $I_{SD} \leq 14A$, $di/dt \leq 140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ Uses IRL2703 data and test conditions.

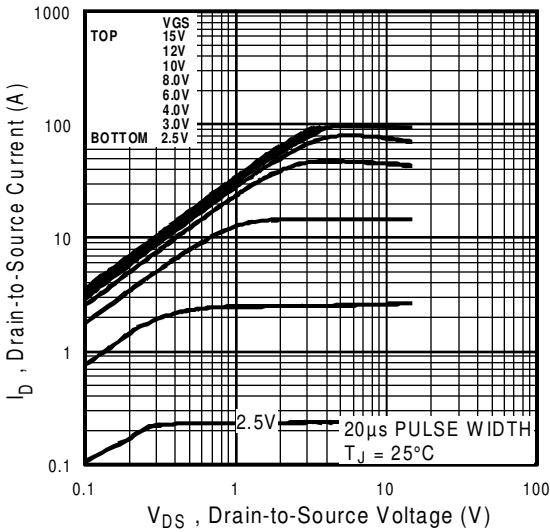


Fig 1. Typical Output Characteristics

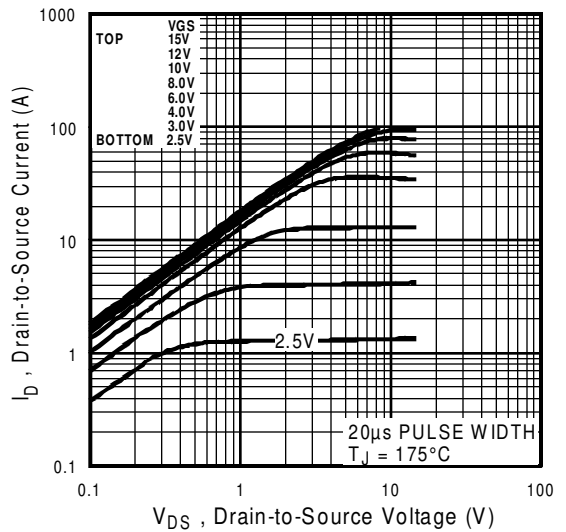


Fig 2. Typical Output Characteristics

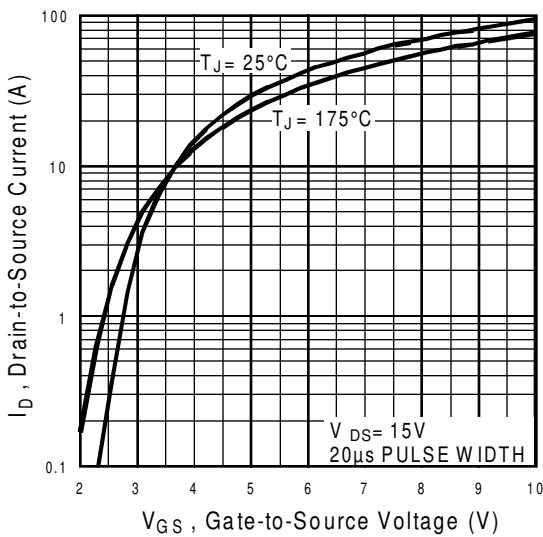


Fig 3. Typical Transfer Characteristics

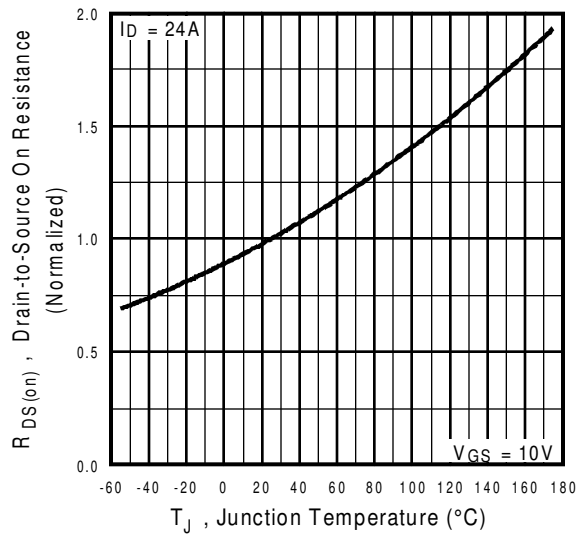


Fig 4. Normalized On-Resistance Vs. Temperature

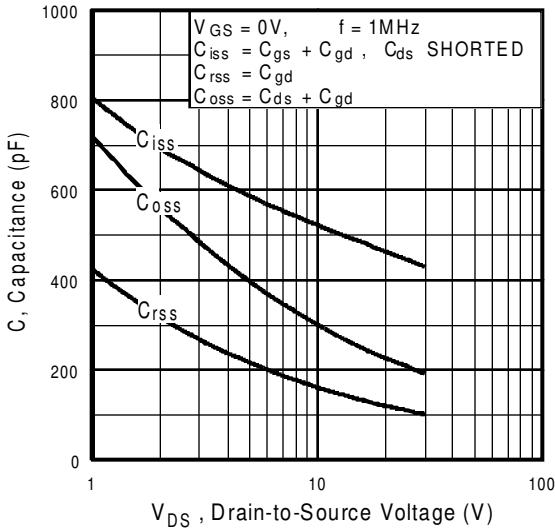


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

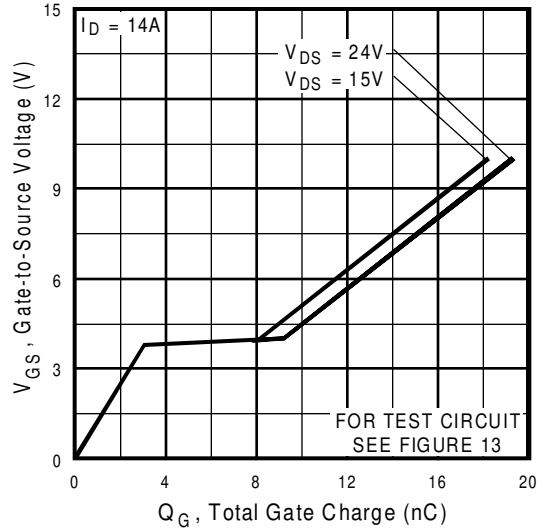


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

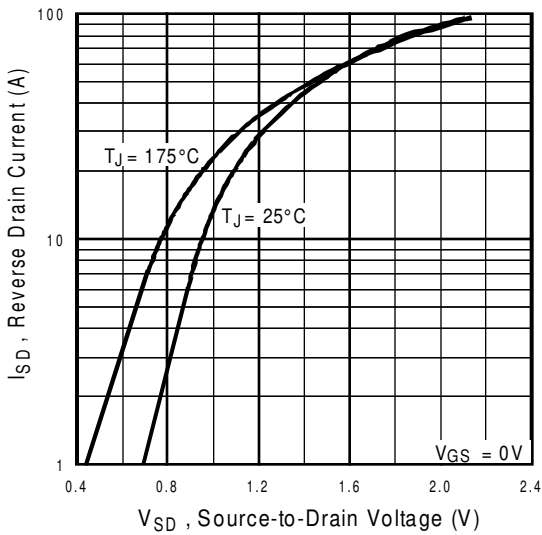


Fig 7. Typical Source-Drain Diode Forward Voltage

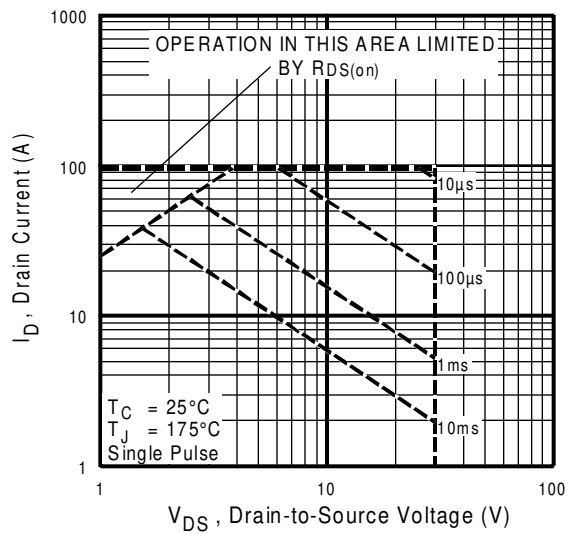


Fig 8. Maximum Safe Operating Area

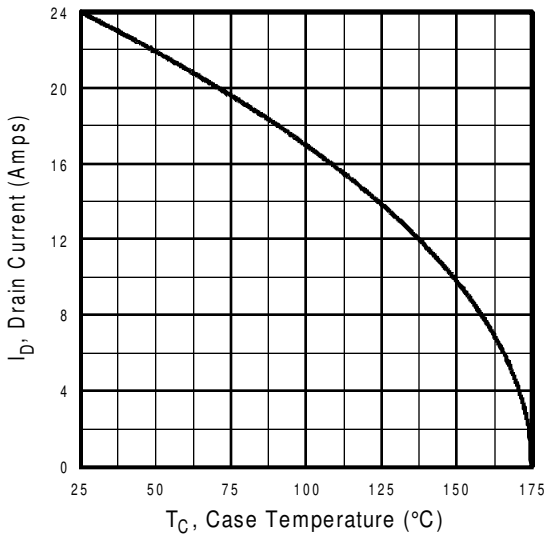


Fig 9. Maximum Drain Current Vs. Case Temperature

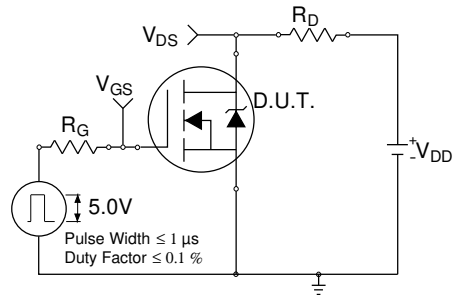


Fig 10a. Switching Time Test Circuit

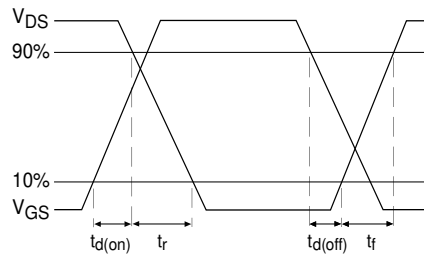


Fig 10b. Switching Time Waveforms

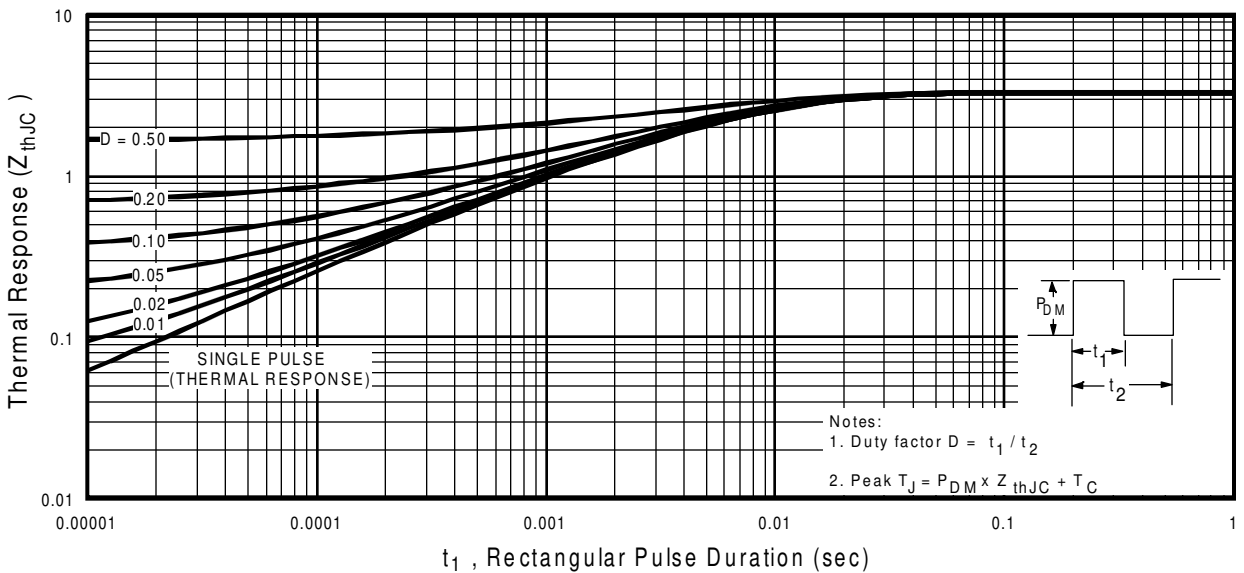


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

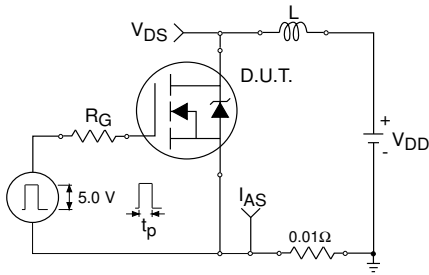


Fig 12a. Unclamped Inductive Test Circuit

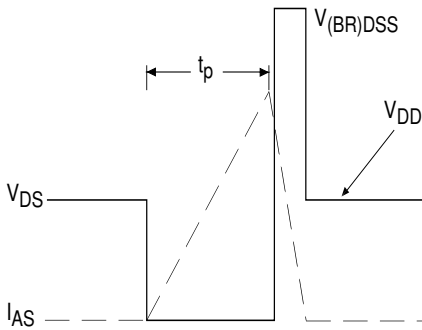


Fig 12b. Unclamped Inductive Waveforms

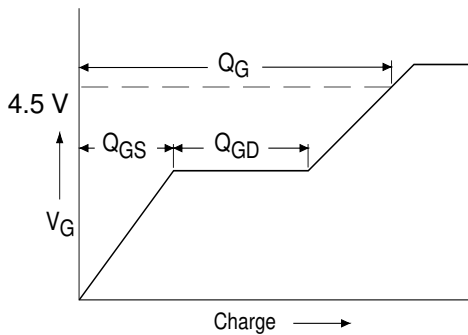


Fig 13a. Basic Gate Charge Waveform

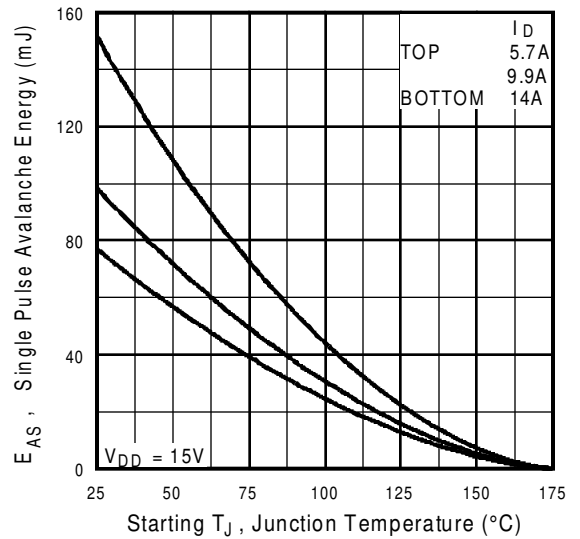


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

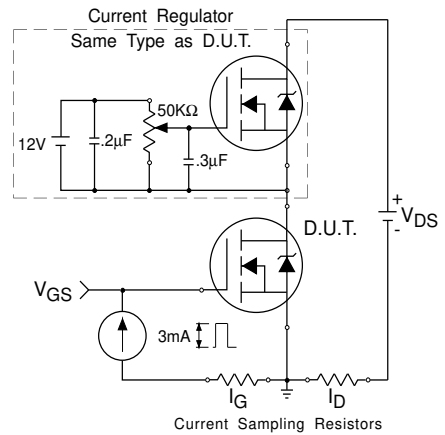
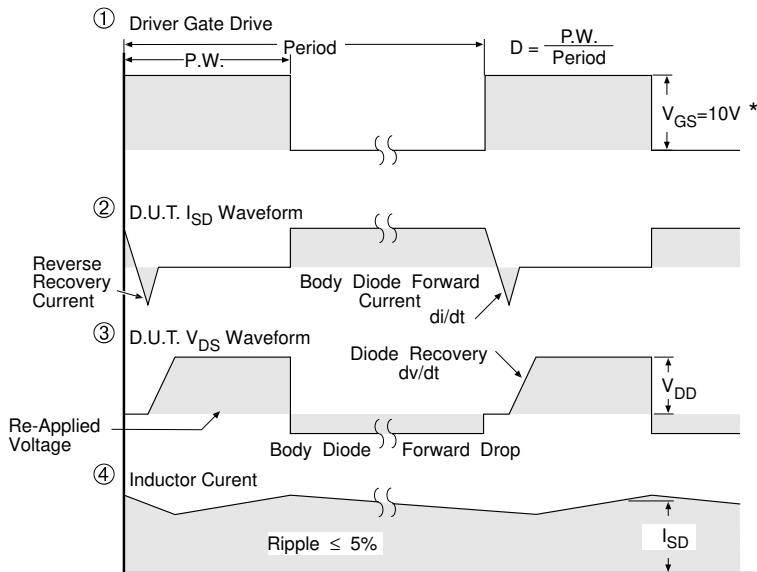
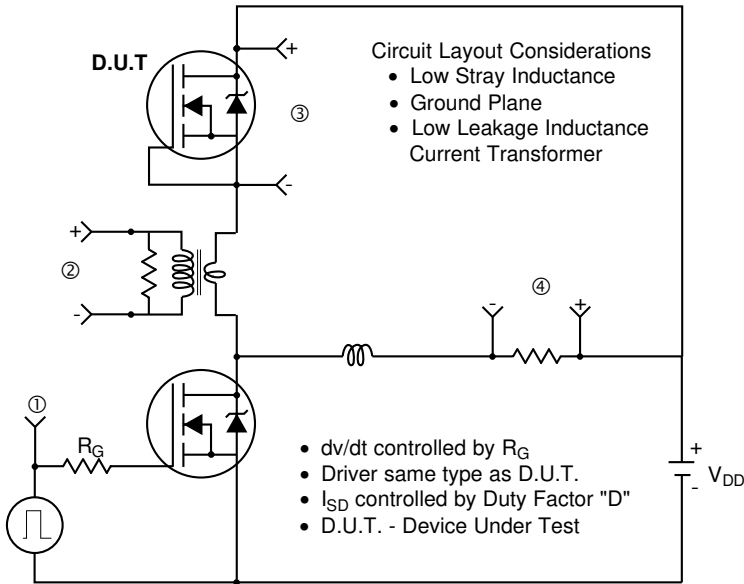


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

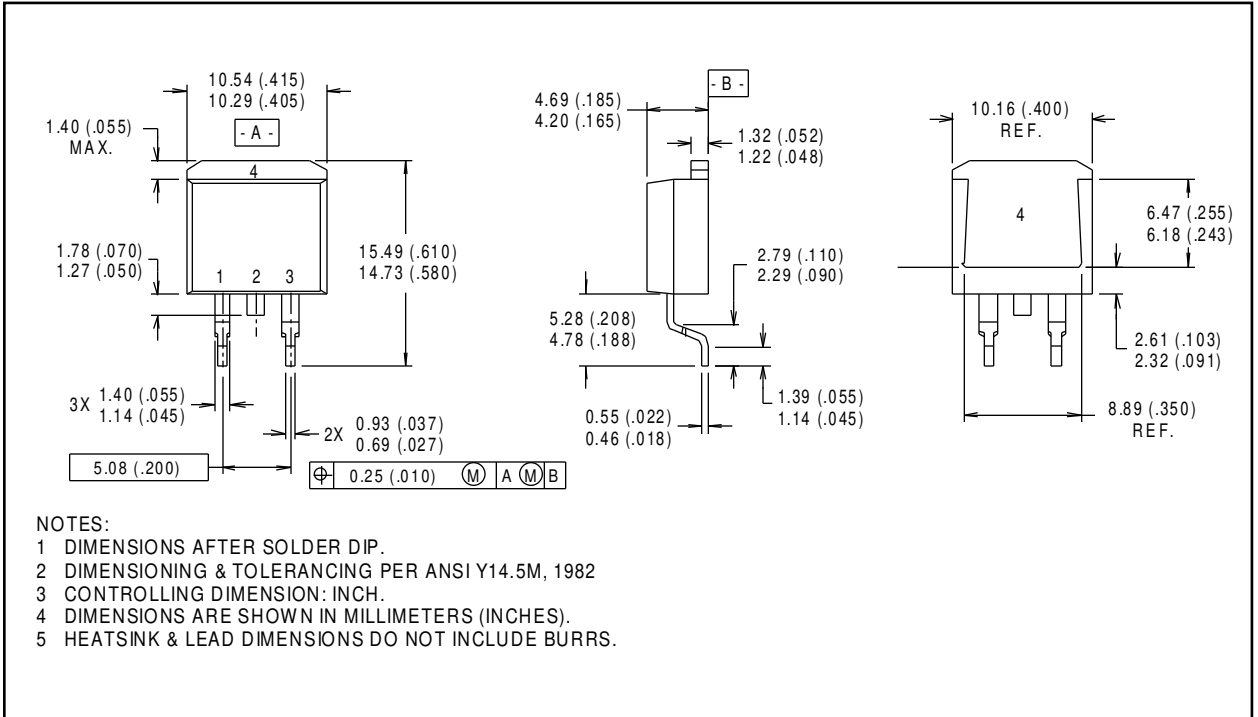
Fig 14. For N-Channel HEXFETS

IRL2703S

Package Outline

D²Pak Outline

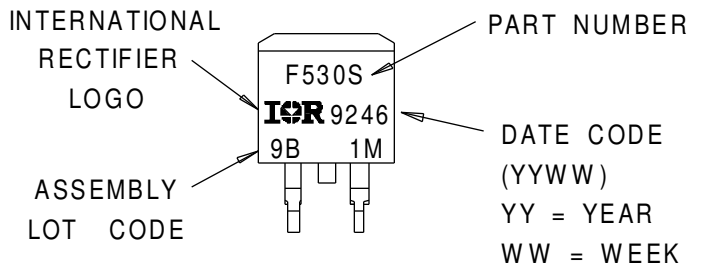
Dimensions are shown in millimeters (inches)



Part Marking Information

D²Pak

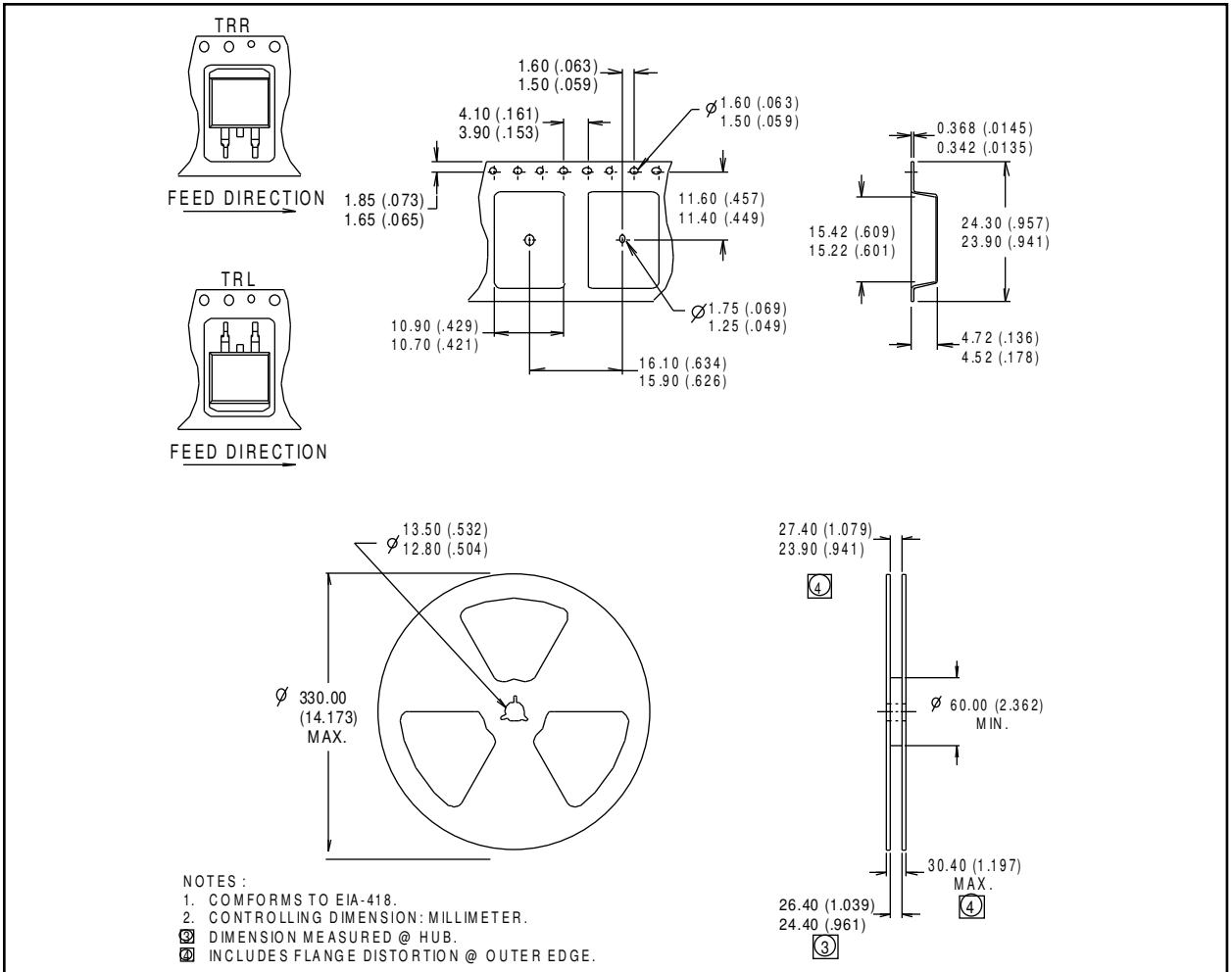
EXAMPLE : THIS IS AN IRF530S
WITH ASSEMBLY
LOT CODE 9B1M



Tape & Reel Information

D²Pak

Dimensions are shown in millimeters (inches)



Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>