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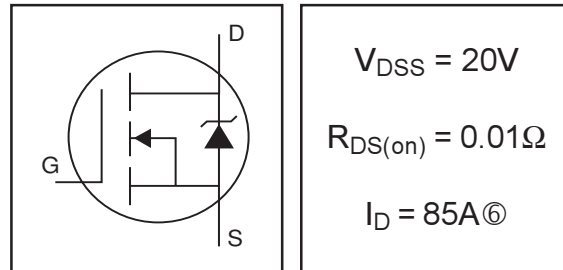
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# IRL3402S

HEXFET® Power MOSFET

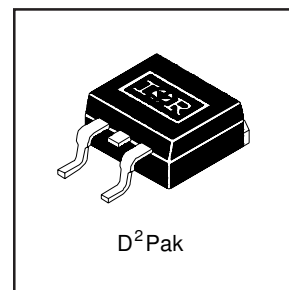
- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching



## Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$ Ⓞ	85Ⓞ	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$ Ⓞ	54	
$I_{DM}$	Pulsed Drain Current ①Ⓞ	340	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.91	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$V_{GSM}$	Gate-to-Source Voltage (Start Up Transient, $t_p = 100\mu\text{s}$ )	14	V
$E_{AS}$	Single Pulse Avalanche Energy②Ⓞ	290	mJ
$I_{AR}$	Avalanche Current③	51	A
$E_{AR}$	Repetitive Avalanche Energy④	11	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ⑤Ⓞ	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted, steady-state)**	---	40	

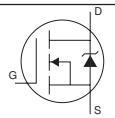
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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>⑤</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 51A <sup>④</sup>
		—	—	0.008		V <sub>GS</sub> = 7.0V, I <sub>D</sub> = 51A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.70	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	65	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 51A <sup>⑤</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>g</sub>	Total Gate Charge	—	—	78	nC	I <sub>D</sub> = 51A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	18		V <sub>DS</sub> = 10V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	30		V <sub>GS</sub> = 4.5V, See Fig. 6 <sup>④⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	10	—	ns	V <sub>DD</sub> = 10V
t <sub>r</sub>	Rise Time	—	140	—		I <sub>D</sub> = 51A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	80	—		R <sub>G</sub> = 5.0Ω, V <sub>GS</sub> = 4.5V
t <sub>f</sub>	Fall Time	—	120	—		R <sub>D</sub> = 0.19Ω, <sup>④⑤</sup>
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	3300	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1400	—		V <sub>DS</sub> = 15V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	510	—		f = 1.0MHz, See Fig. 5 <sup>⑤</sup>

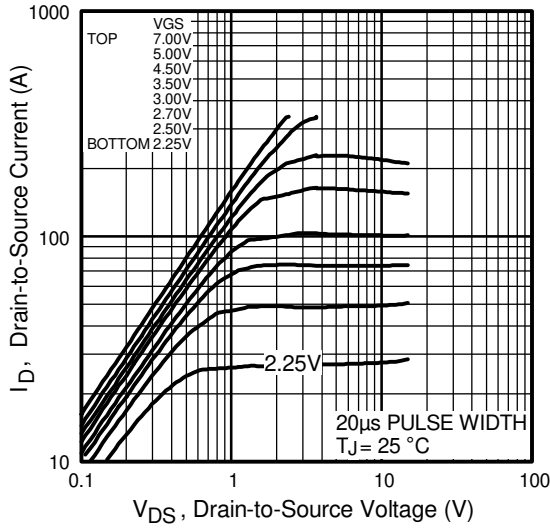
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①⑤</sup>	—	—	340		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 51A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	72	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 51A
Q <sub>rr</sub>	Reverse Recovery Charge	—	160	240	nC	di/dt = 100A/μs <sup>④⑤</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

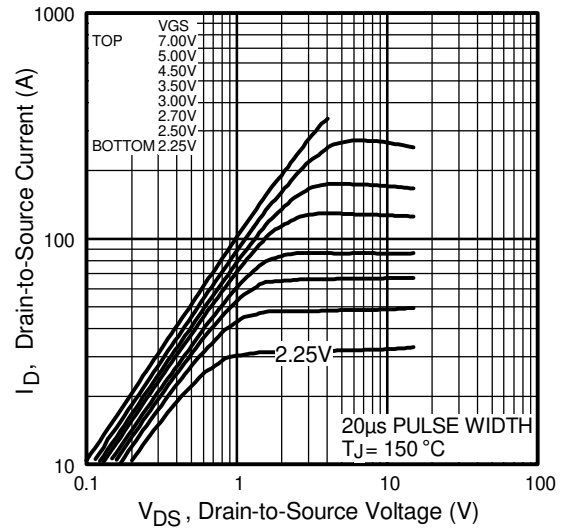
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T<sub>J</sub> = 25°C, L = 220μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 51A.
- ③ I<sub>SD</sub> ≤ 51A, di/dt ≤ 82A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRL3402 data and test conditions
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

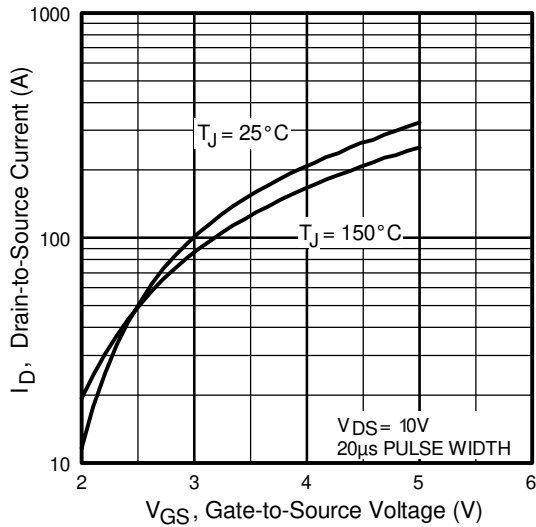
\*\* When mounted on FR-4 board using minimum recommended footprint.  
For recommended footprint and soldering techniques refer to application note #AN-994.



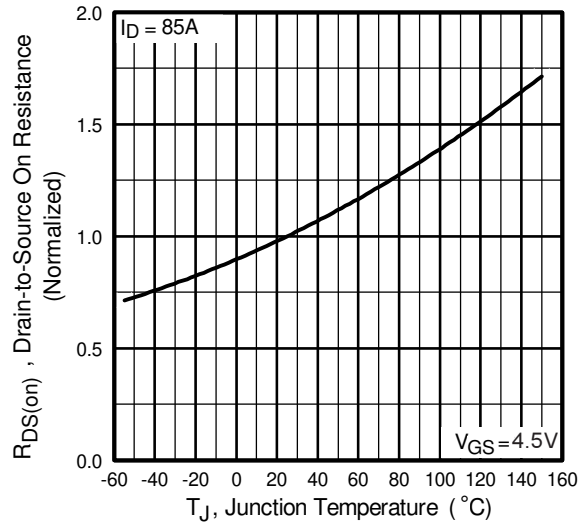
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



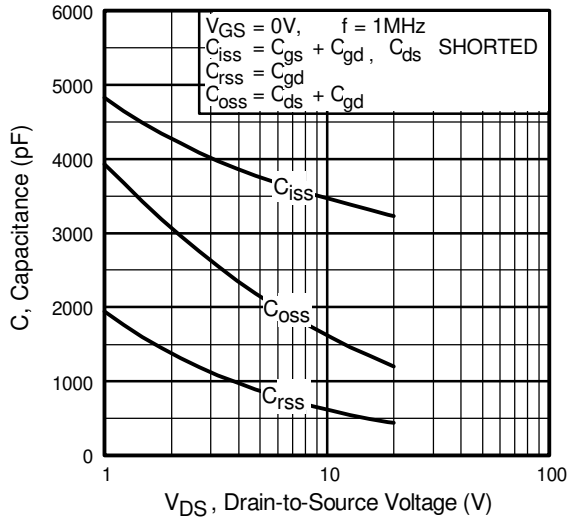
**Fig 3.** Typical Transfer Characteristics



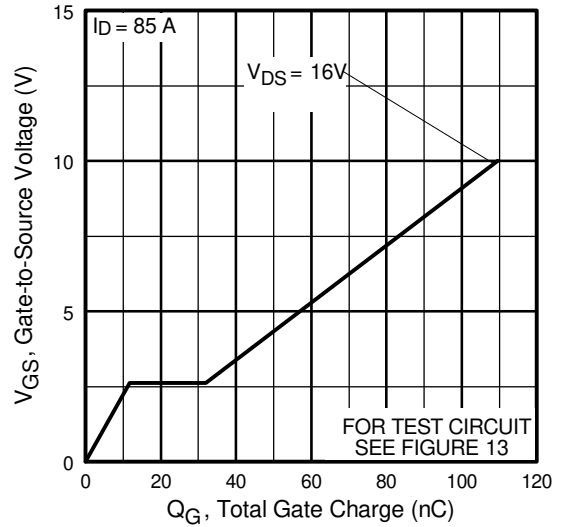
**Fig 4.** Normalized On-Resistance Vs. Temperature

# IRL3402S

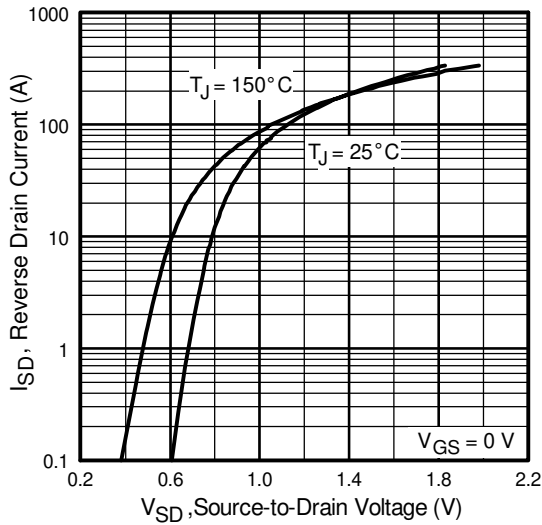
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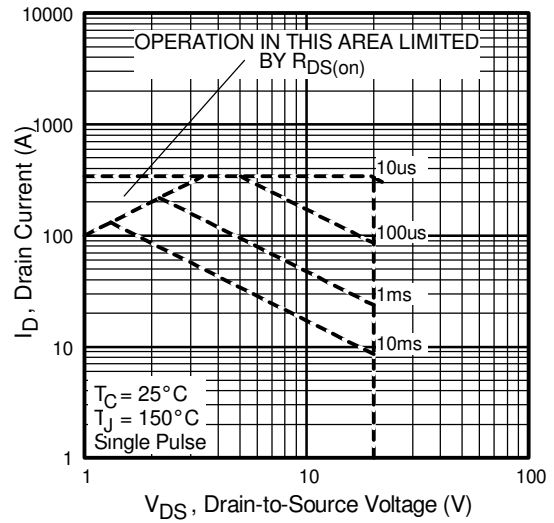
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



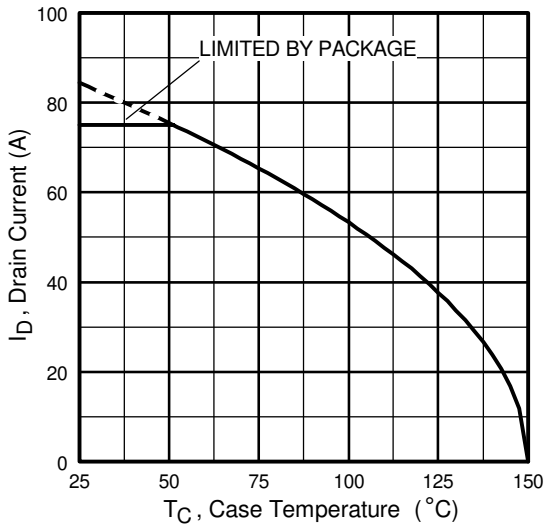
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



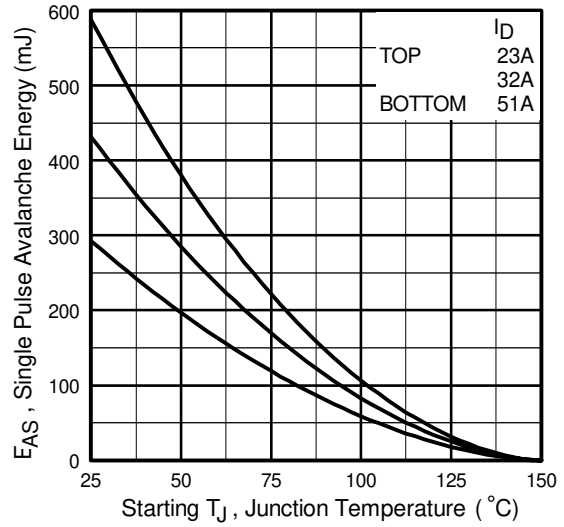
**Fig 7.** Typical Source-Drain Diode Forward Voltage



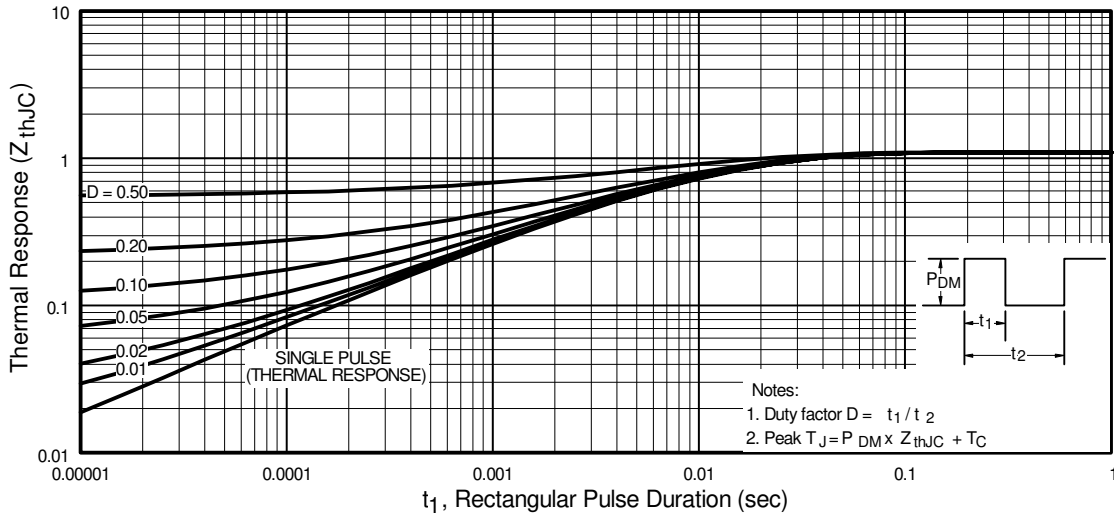
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature



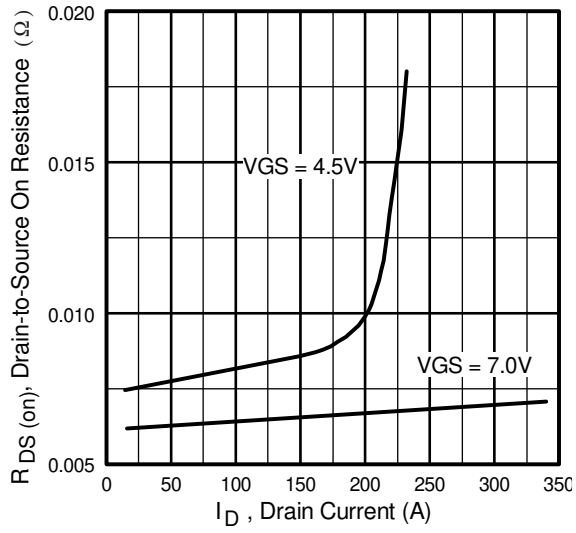
**Fig 10.** Maximum Avalanche Energy Vs. Drain Current



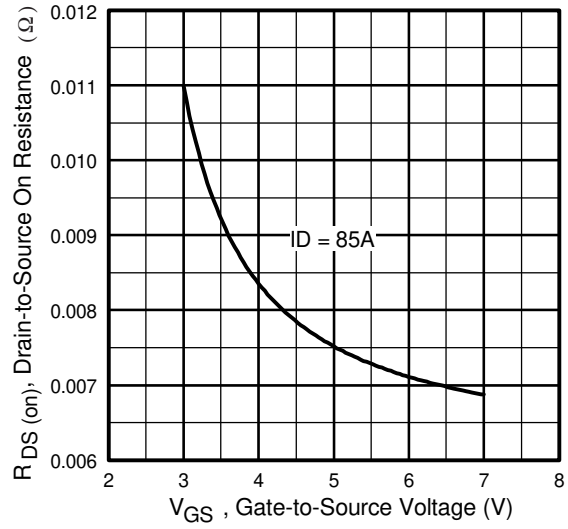
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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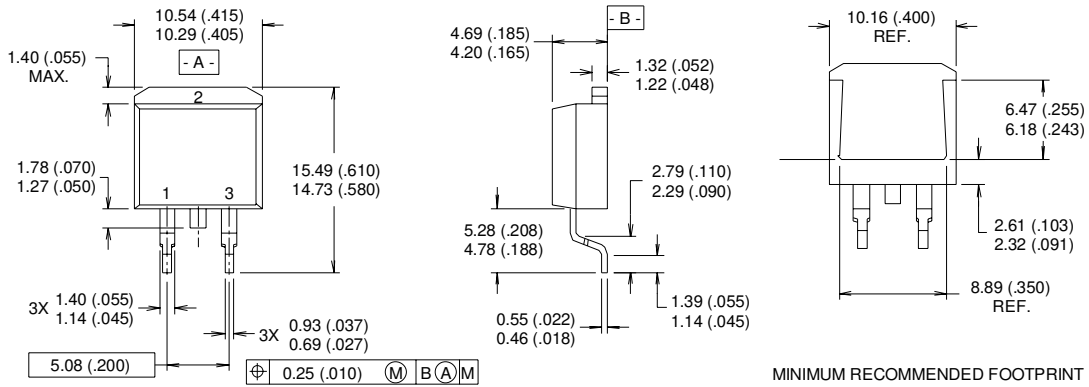


**Fig 12.** On-Resistance Vs. Drain Current



**Fig 13.** On-Resistance Vs. Gate Voltage

## D<sup>2</sup>Pak Package Outline



**NOTES:**

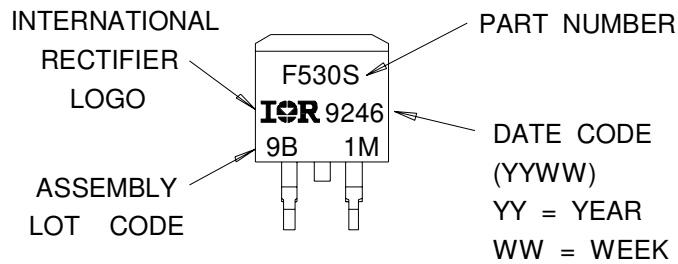
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

## Part Marking Information

D<sup>2</sup>Pak



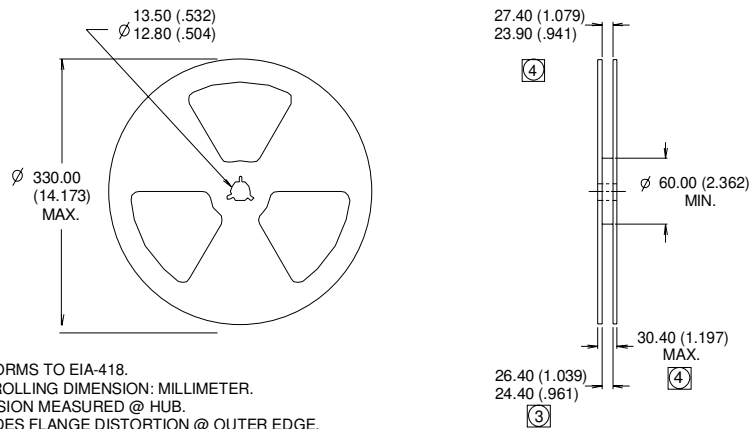
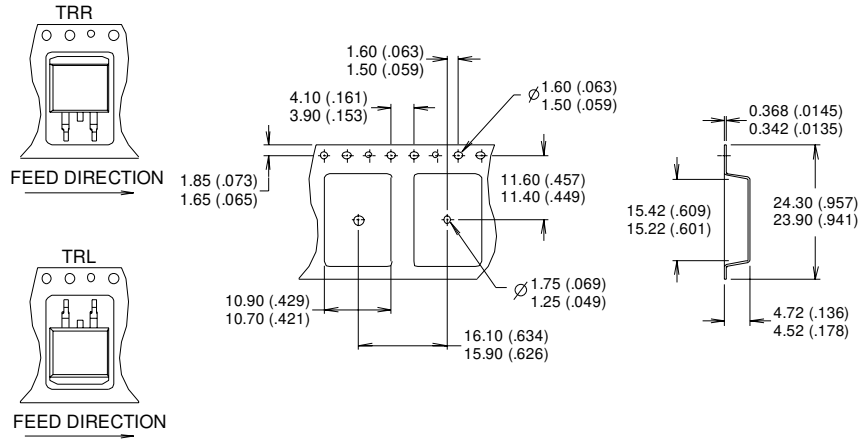


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## Tape & Reel Information

D<sup>2</sup>Pak



Data and specifications subject to change without notice.

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