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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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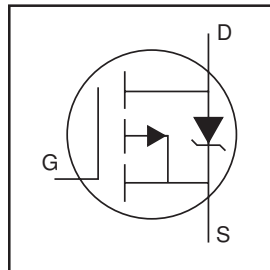
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



IRL5602S

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated

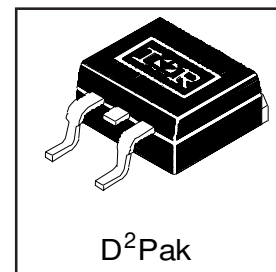


$V_{DSS} = -20V$
$R_{DS(on)} = 0.042\Omega$
$I_D = -24A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-24	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-17	
I_{DM}	Pulsed Drain Current ①	-96	
$P_D @ T_C = 25^\circ C$	Power Dissipation	75	W
	Linear Derating Factor	0.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 8.0	V
E_{AS}	Single Pulse Avalanche Energy②	290	mJ
I_{AR}	Avalanche Current①	-12	A
E_{AR}	Repetitive Avalanche Energy①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-0.81	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.013	—	V/°C	Reference to 25°C, I _D = -1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.042	Ω	V _{GS} = -4.5V, I _D = -12A ^④
		—	—	0.062		V _{GS} = -2.7V, I _D = -10A ^④
		—	—	0.075		V _{GS} = -2.5V, I _D = -10A ^④
V _{GS(th)}	Gate Threshold Voltage	-0.7	—	-1.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	12	—	—	S	V _{DS} = -15V, I _D = -12A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -20V, V _{GS} = 0V
		—	—	-250		V _{DS} = -16V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	500	nA	V _{GS} = -8.0V
	Gate-to-Source Reverse Leakage	—	—	-500		V _{GS} = 8.0V
Q _g	Total Gate Charge	—	—	44	nC	I _D = -12A
Q _{gs}	Gate-to-Source Charge	—	—	8.7		V _{DS} = -16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		V _{GS} = -4.5V, See Fig. 6 and 13 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	9.7	—	ns	V _{DD} = -10 V
t _r	Rise Time	—	73	—		I _D = -12A
t _{d(off)}	Turn-Off Delay Time	—	53	—		R _G = 6.0Ω, V _{GS} = 4.5V
t _f	Fall Time	—	84	—		R _D = 0.8Ω, See Fig. 10 ^{④⑤}
L _S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	1460	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	790	—		V _{DS} = -15V
C _{rss}	Reverse Transfer Capacitance	—	370	—		f = 1.0MHz, See Fig. 5 ^⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-24	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	-96		
V _{SD}	Diode Forward Voltage	—	—	-1.4	V	T _J = 25°C, I _S = -12A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	58	88	ns	T _J = 25°C, I _F = -12A
Q _{rr}	Reverse Recovery Charge	—	54	81	nC	di/dt = -100A/μs ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 3.0mH
R_G = 25Ω, I_{AS} = -14A. (See Figure 12)
- ③ I_{SD} ≤ -12A, di/dt ≤ 120A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

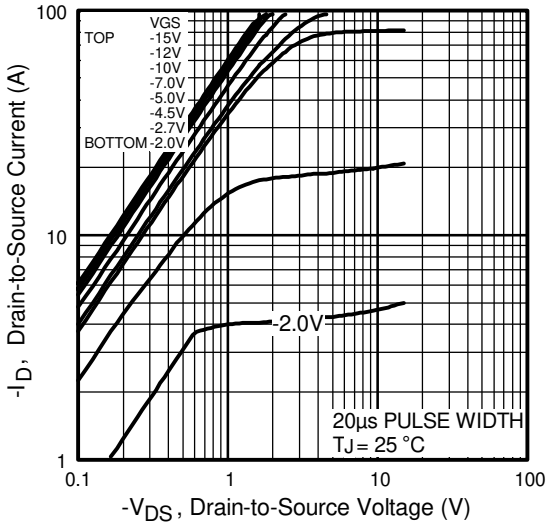


Fig 1. Typical Output Characteristics

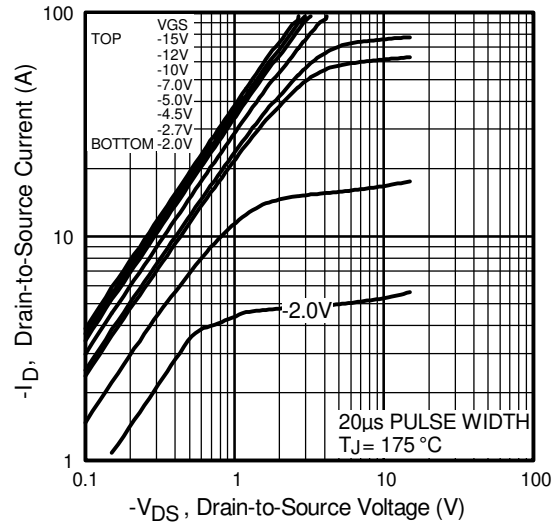


Fig 2. Typical Output Characteristics

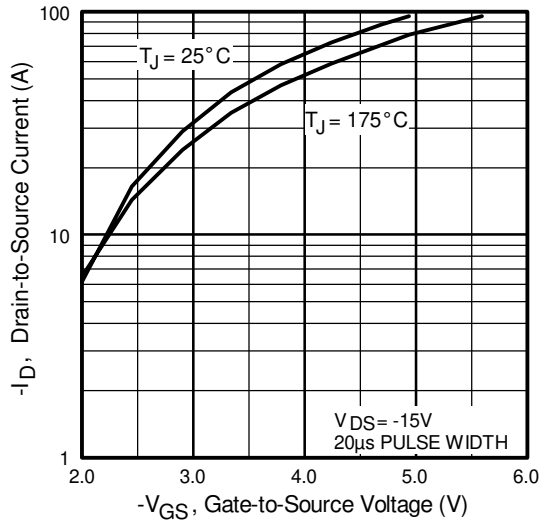


Fig 3. Typical Transfer Characteristics

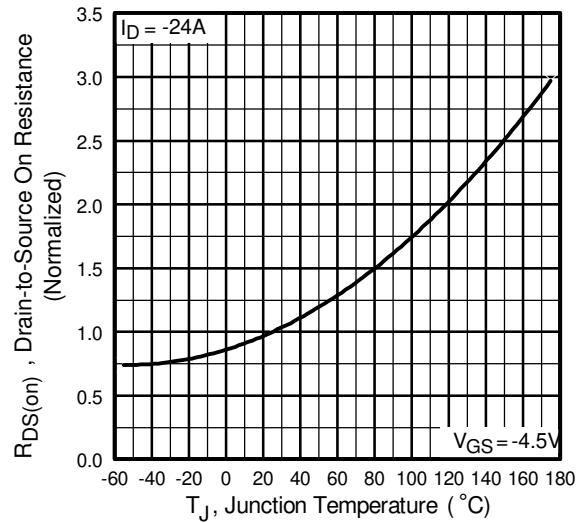


Fig 4. Normalized On-Resistance Vs. Temperature

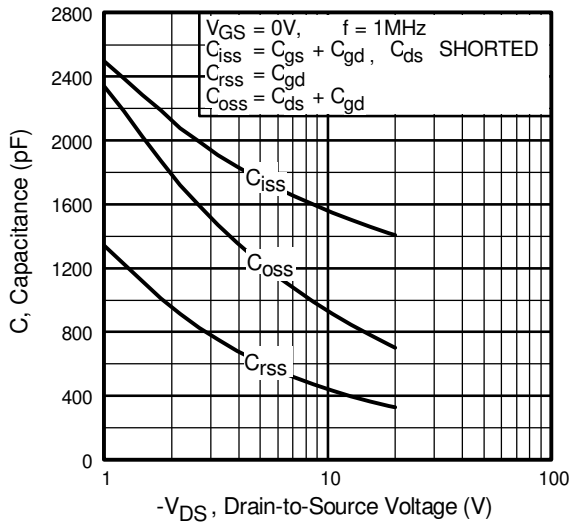


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

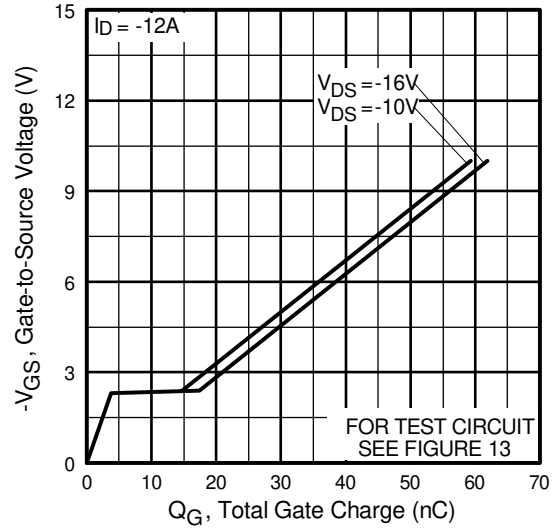


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

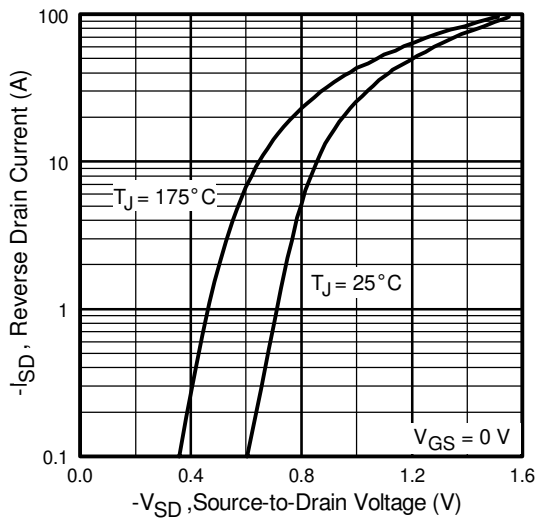


Fig 7. Typical Source-Drain Diode Forward Voltage

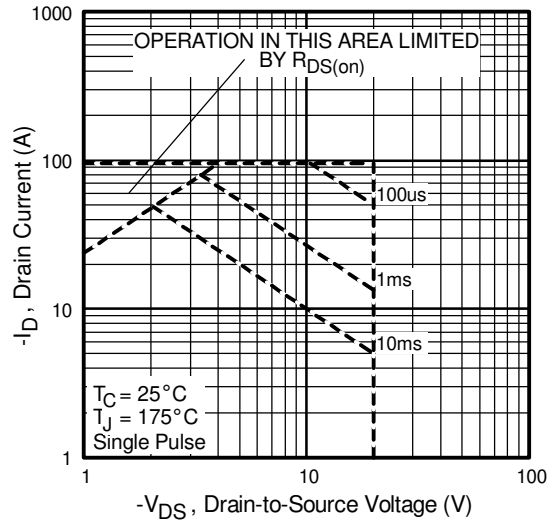


Fig 8. Maximum Safe Operating Area

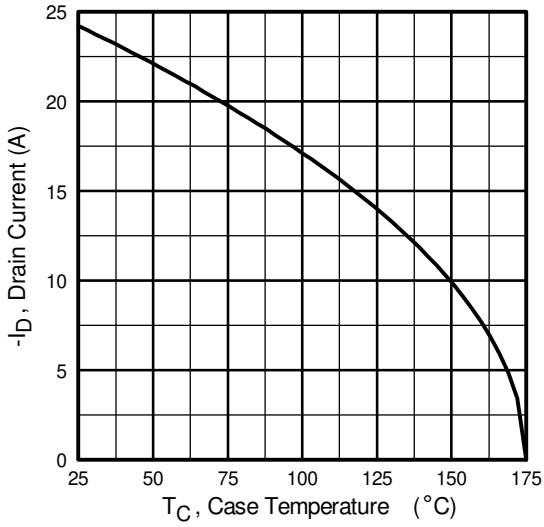


Fig 9. Maximum Drain Current Vs. Case Temperature

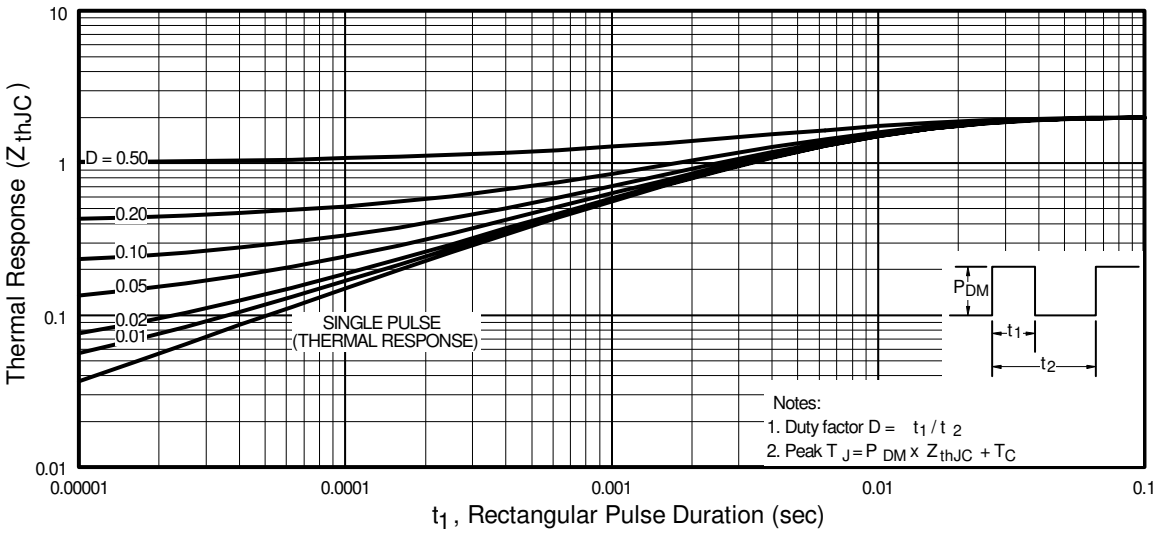
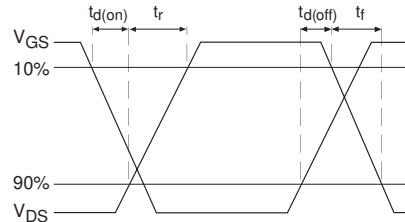
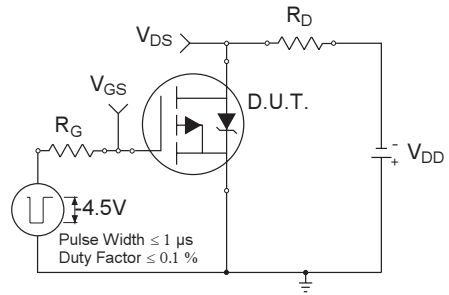


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

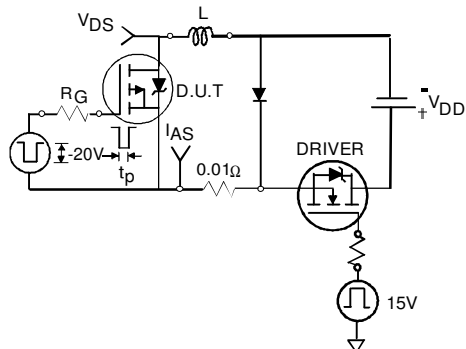


Fig 12a. Unclamped Inductive Test Circuit

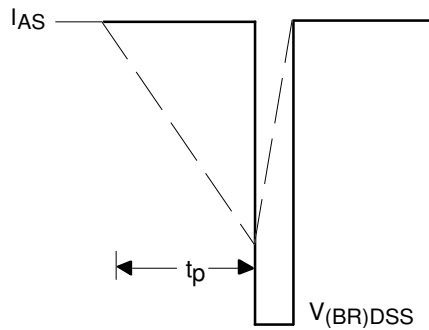


Fig 12b. Unclamped Inductive Waveforms

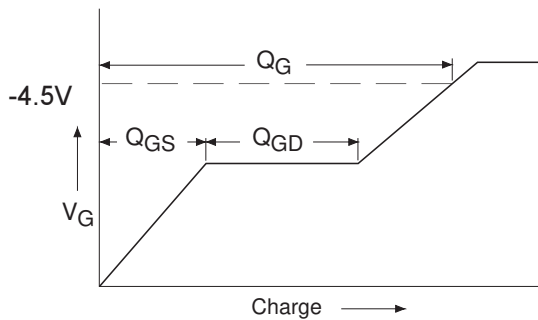


Fig 13a. Basic Gate Charge Waveform

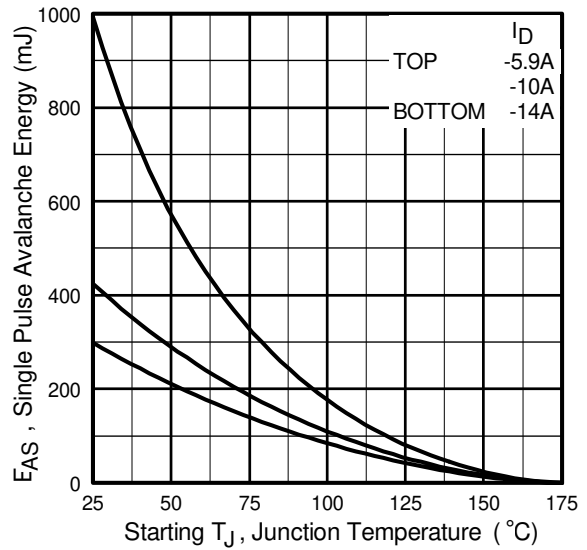


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

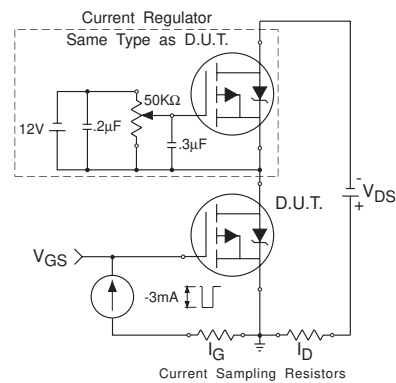
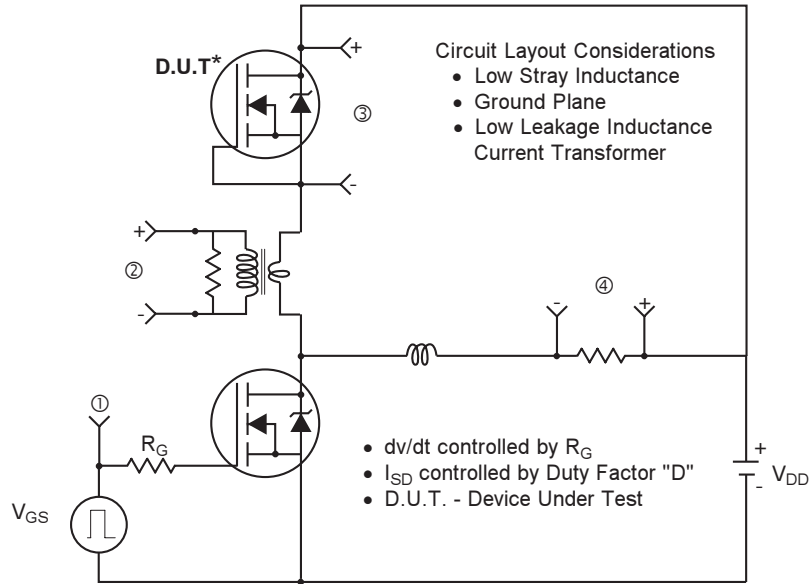
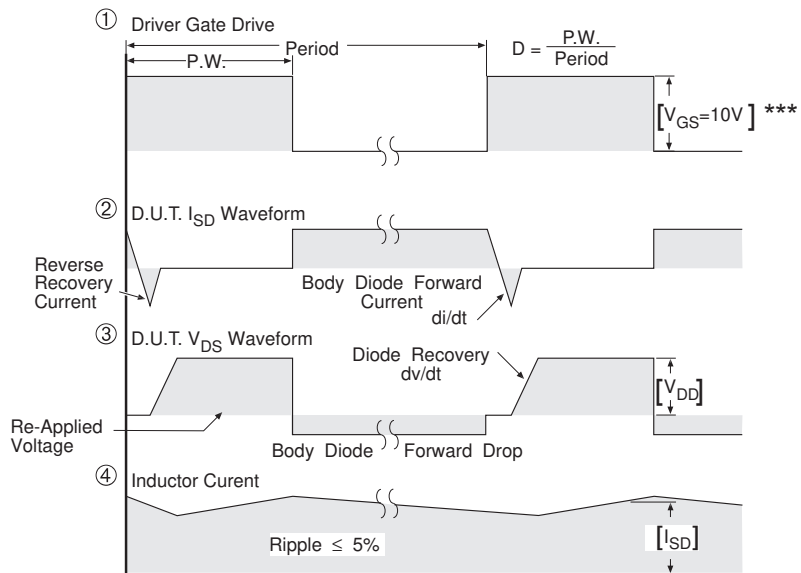


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

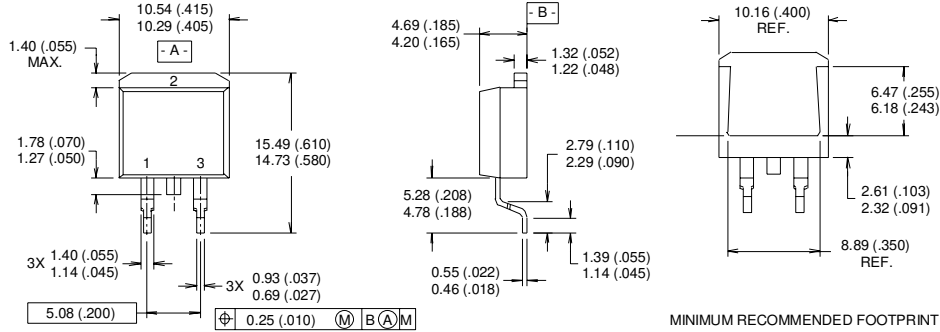


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

IRL5602S TO-263AB Package Details

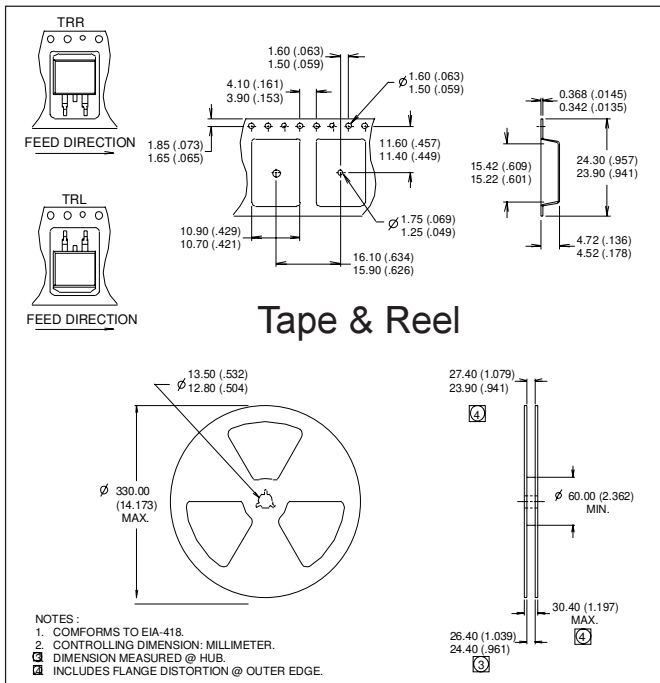
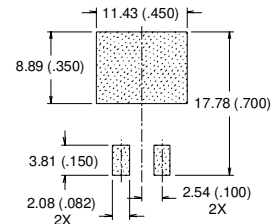
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- NOTES:
- 1 DIMENSIONS AFTER SOLDER DIP.
 - 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 3 CONTROLLING DIMENSION : INCH.
 - 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

- LEAD ASSIGNMENTS
- 1 - GATE
 - 2 - DRAIN
 - 3 - SOURCE

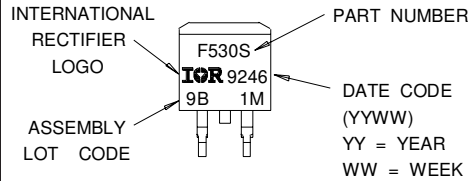
MINIMUM RECOMMENDED FOOTPRINT



- NOTES:
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Part Marking

(This is an IRF530S with assembly lot code 9B1M)



International
IR Rectifier

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<http://www.irf.com/> Data and specifications subject to change without notice. 5/99

Note: For the most current drawings please refer to the IR website at:
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