



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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**IRLR3802PbF**  
**IRLU3802PbF**

HEXFET® Power MOSFET

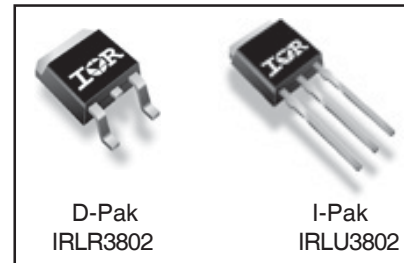
**Applications**

- High Frequency 3.3V and 5V input Point-of-Load Synchronous Buck Converters
- Power Management for Netcom, Computing and Portable Applications.
- Lead-Free

$V_{DSS}$	$R_{DS(on)}$ max	$Q_g$
12V	8.5m $\Omega$	27nC

**Benefits**

- Ultra-Low Gate Impedance
- Very Low  $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$V_{DS}$	Drain-Source Voltage	12	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	84 ④	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	60 ④	
$I_{DM}$	Pulsed Drain Current ①	320	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	88	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation	44	W
	Linear Derating Factor	0.59	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Notes ① through ④ are on page 9  
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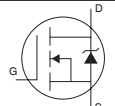
## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	12	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.009	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA ③
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	6.5	8.5	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A ③
		—	—	30		V <sub>GS</sub> = 2.8V, I <sub>D</sub> = 12A
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.6	—	1.9	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-3.2	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	100	μA	V <sub>DS</sub> = 9.6V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 9.6V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 12V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -12V
g <sub>fs</sub>	Forward Transconductance	31	—	—	S	V <sub>DS</sub> = 6.0V, I <sub>D</sub> = 12A
Q <sub>g</sub>	Total Gate Charge	—	27	41	nC	V <sub>DS</sub> = 6.0V V <sub>GS</sub> = 5.0V I <sub>D</sub> = 6.0A See Fig.16
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-Source Charge	—	3.6	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-Source Charge	—	2.0	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	10	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	11	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	12	—		
Q <sub>oss</sub>	Output Charge	—	28	—	nC	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V
t <sub>d(on)</sub>	Turn-On Delay Time	—	11	—	ns	V <sub>DD</sub> = 6.0V, V <sub>GS</sub> = 4.5V③ I <sub>D</sub> = 12A Clamped Inductive Load
t <sub>r</sub>	Rise Time	—	14	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	21	—		
t <sub>f</sub>	Fall Time	—	17	—		
C <sub>iss</sub>	Input Capacitance	—	2490	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 6.0V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	2150	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	530	—		

## Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	300	mJ
I <sub>AR</sub>	Avalanche Current①	—	20	A

## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	84④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	320		
V <sub>SD</sub>	Diode Forward Voltage	—	0.81	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 12A, V <sub>GS</sub> = 0V ③
		—	0.65	—		T <sub>J</sub> = 125°C, I <sub>S</sub> = 12A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	52	78	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 12A, V <sub>R</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge	—	54	81	nC	di/dt = 100A/μs ③
t <sub>rr</sub>	Reverse Recovery Time	—	50	75	ns	T <sub>J</sub> = 125°C, I <sub>F</sub> = 12A, V <sub>R</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge	—	50	75	nC	di/dt = 100A/μs ③

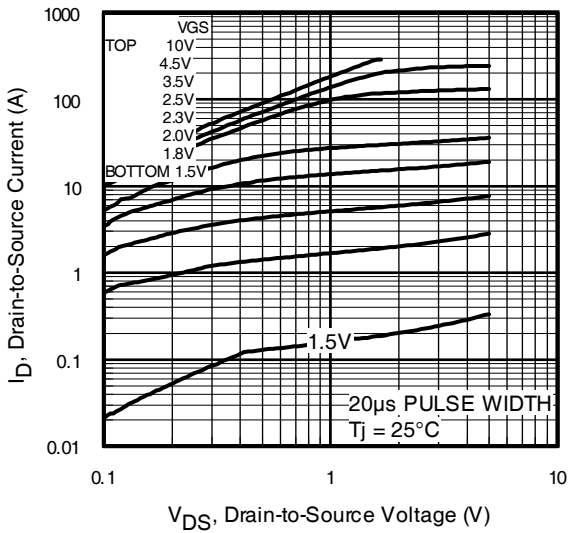


Fig 1. Typical Output Characteristics

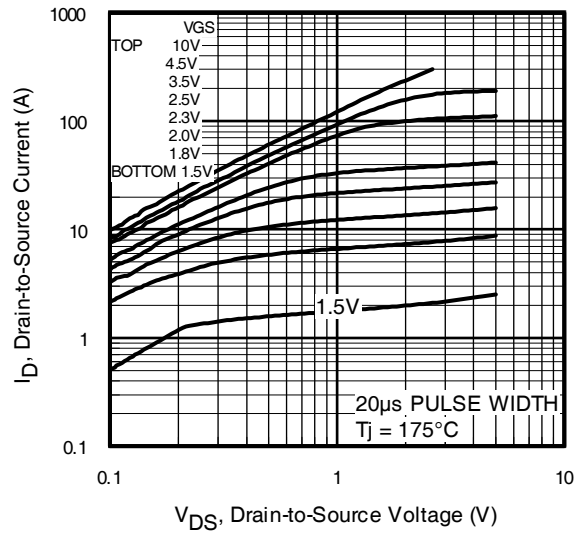


Fig 2. Typical Output Characteristics

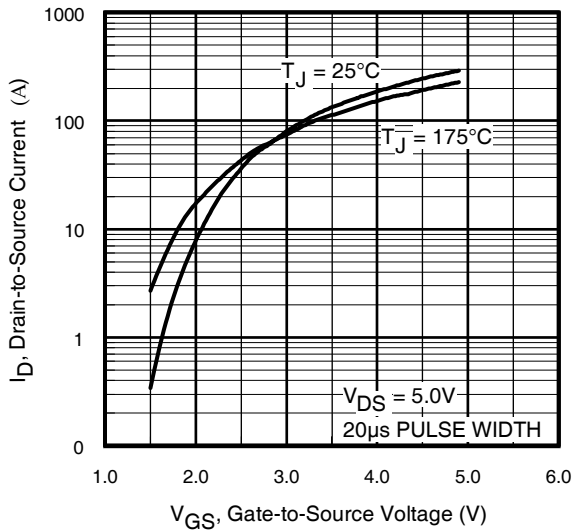


Fig 3. Typical Transfer Characteristics

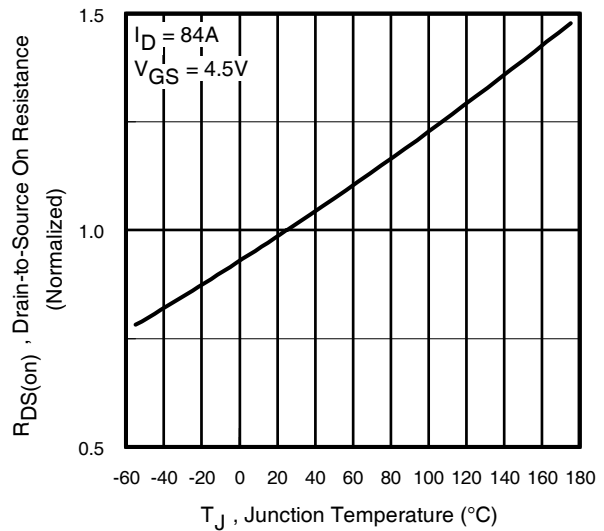
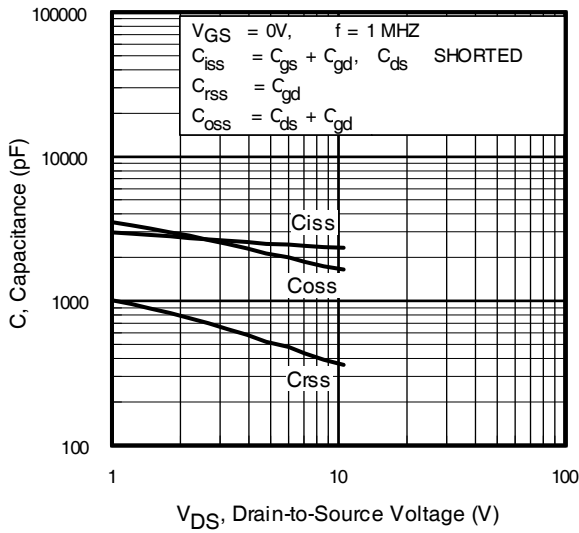


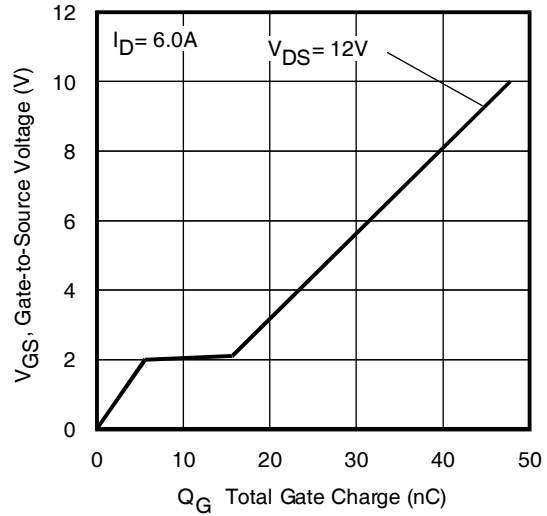
Fig 4. Normalized On-Resistance Vs. Temperature



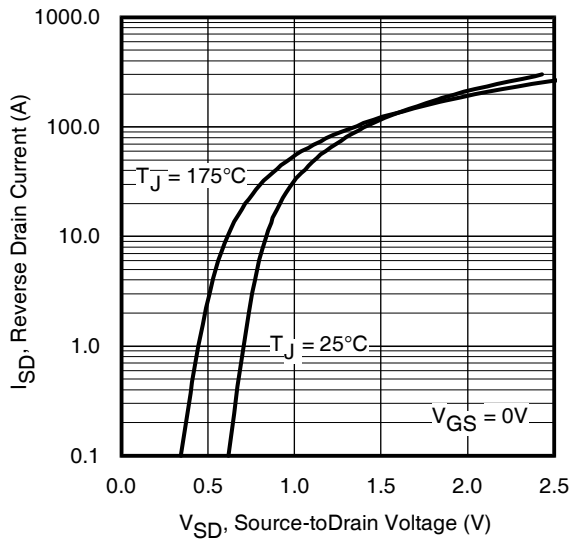
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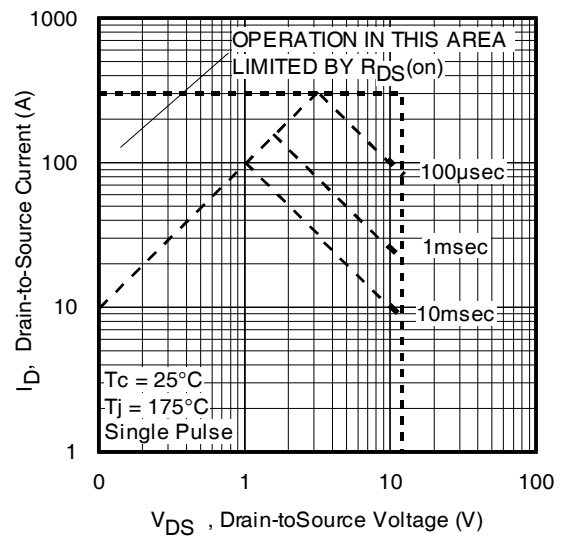
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

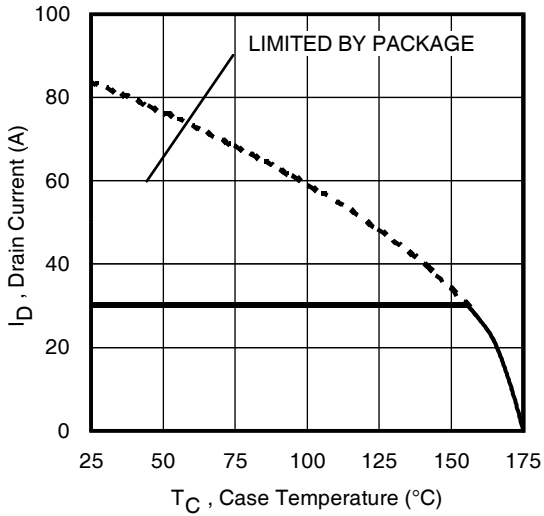


Fig 9. Maximum Drain Current Vs. Case Temperature

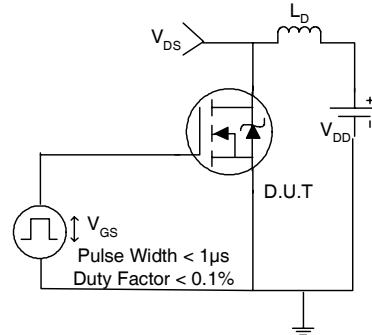


Fig 10a. Switching Time Test Circuit

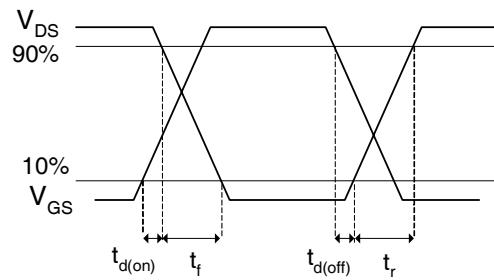


Fig 10b. Switching Time Waveforms

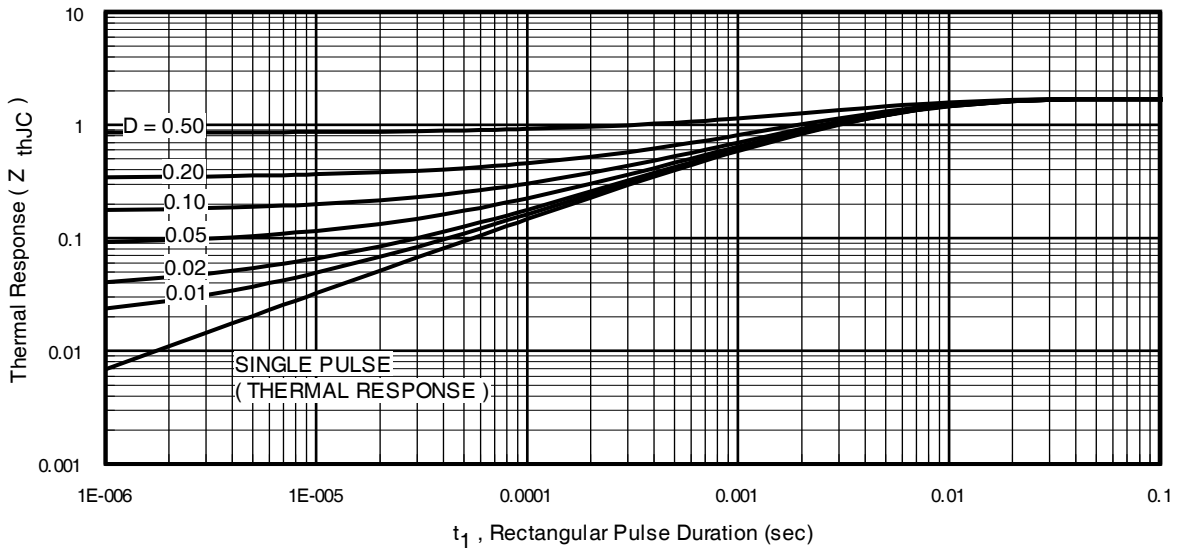
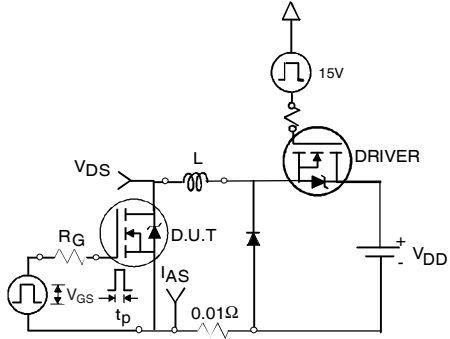
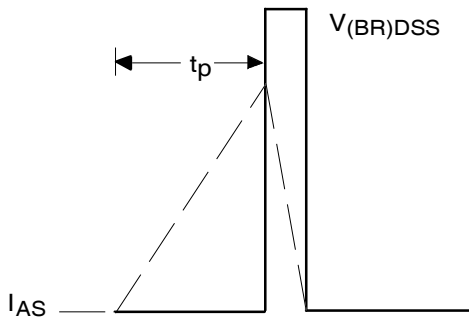


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

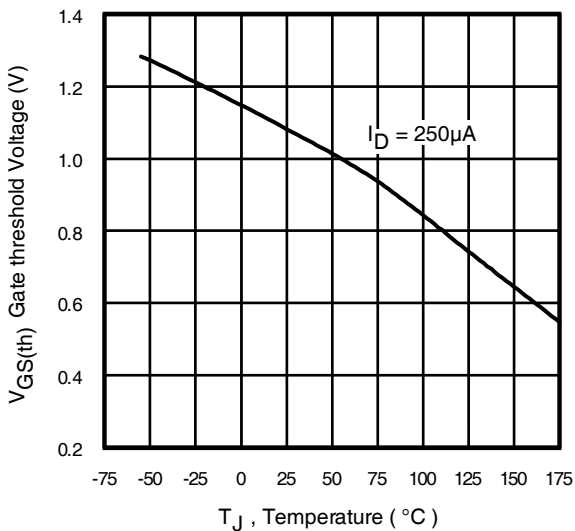
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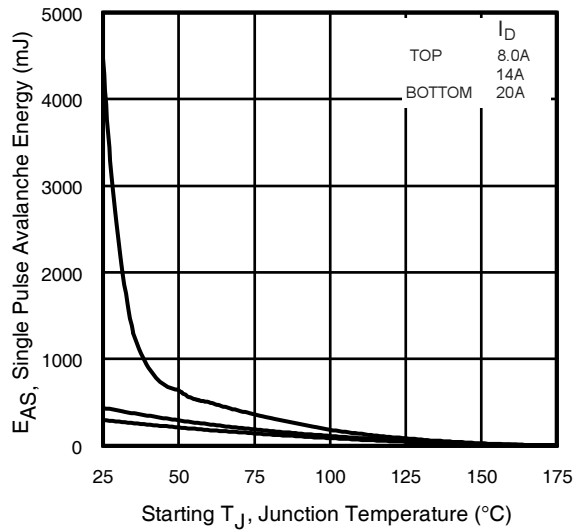
**Fig 12a.** Unclamped Inductive Test Circuit



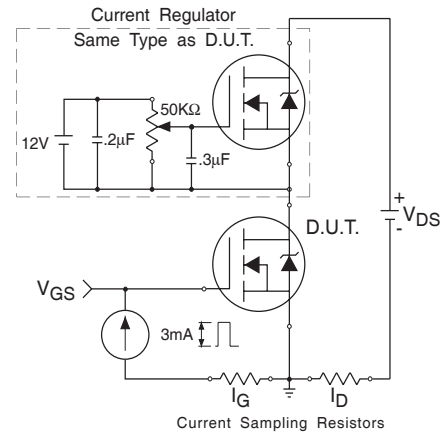
**Fig 12b.** Unclamped Inductive Waveforms



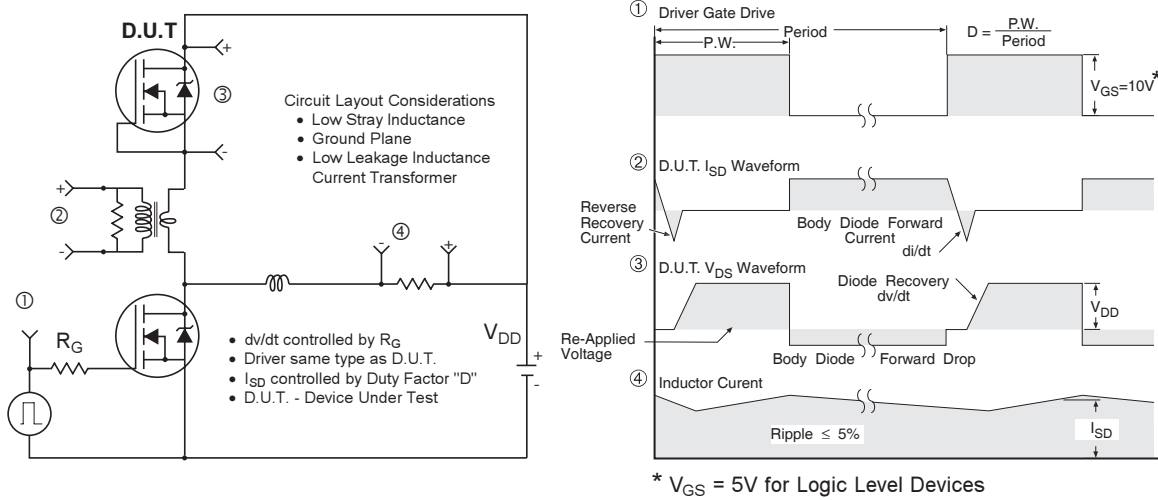
**Fig 13.** Threshold Voltage Vs. Temperature



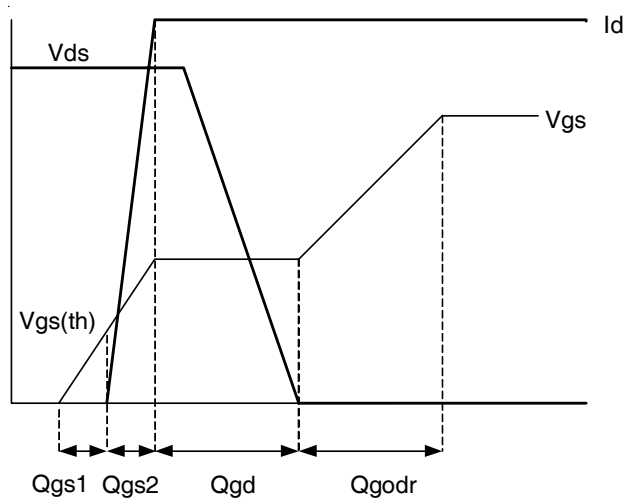
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Gate Charge Test Circuit



**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



**Fig 16. Gate Charge Waveform**

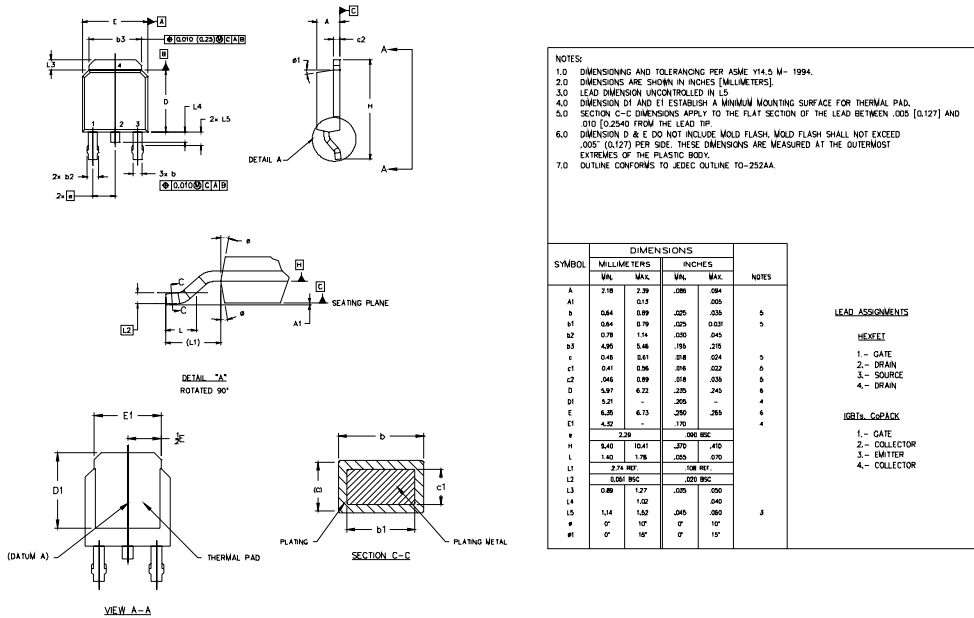


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**IR** Rectifier

## D-Pak (TO-252AA) Package Outline

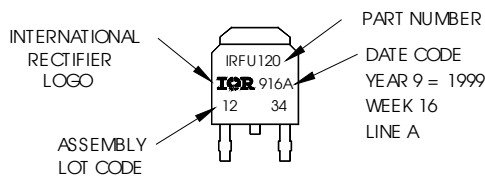
Dimensions are shown in millimeters (inches)



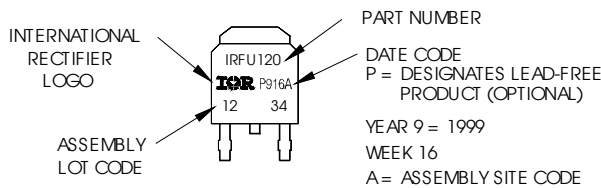
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

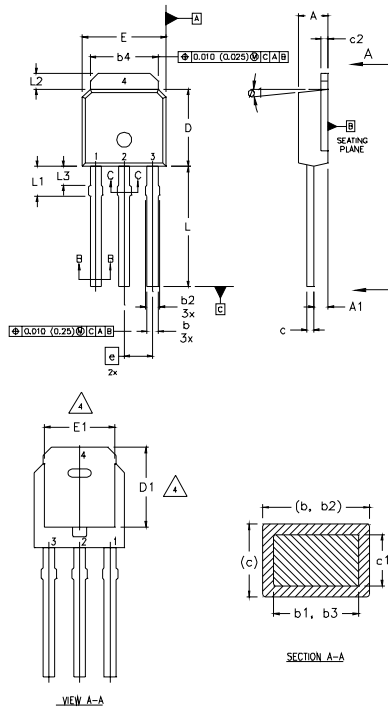


OR



### I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
  - 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - 5 LEAD DIMENSION UNCONTROLLED IN L3.
  - 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
  - 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
  - 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

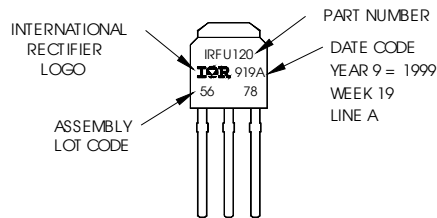
- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15'	Ø	15'	

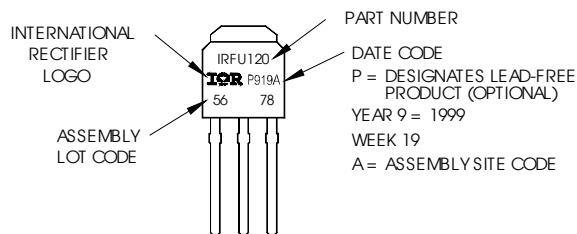
### I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON VW 19, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line  
position indicates "Lead-Free"



OR

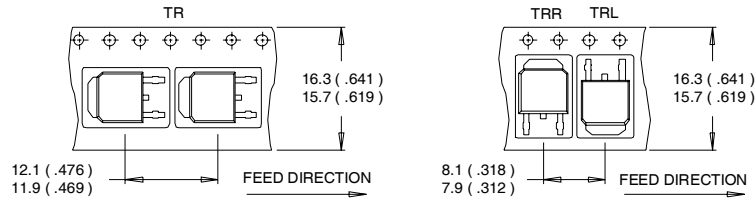


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## D-Pak (TO-252AA) Tape & Reel Information

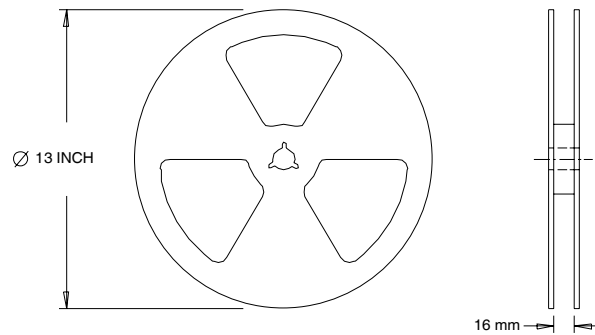
Dimensions are shown in millimeters (inches)

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**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
  - ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.4\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 20\text{A}$ .
  - ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- \* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrialmarket.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>