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iMOTION™

Dual Motor High Performance Sensorless Control IC

Description

IRMCF588 is a high performance Flash based motion control IC designed and optimized for complete air conditioner control which contains two kinds of computation engines integrated into one chip. There are two Motion Control Engines (MCE™) for sensorless control of permanent magnet motors and the other is an 8-bit high-speed microcontroller (8051). The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm fully supports single shunt or leg shunt current reconstruction. IRMCF588 performs a PFC (Power Factor Correction) function in addition to the motor control. IRMCF588 comes in a 100 pin QFP package.

Features

- Dual MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and OP amp analog circuits
- Integrated temperature sensor
- Supports both interior and surface permanent magnet motor sensorless control
- Zero speed sensorless control for ultra-low speed operation
- Dedicated PFC PWM for digital PFC control
- Loss minimization Space Vector PWM
- Five-channel analog output (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Two Serial communication interface (UART)
- I2Cserial interface
- Watchdog timer with independent internal clock
- Internal 64 Kbyte flash plus 16Kbyte OTP memory
- 3.3V single supply
- Factory calibrated analog inputs

Product Summary

Maximum clock input ($f_{crystal}$)	60 MHz
Maximum Internal clock (SYSCLK)	120MHz
Maximum 8051 clock (8051CLK)	30MHz
Sensorless control computation time	35 µsec@100MHz
MCE™ computation data range	16 bit signed
8051 Program Flash	52KB
8051/MCE Data RAM	2 x 4KB
MCE Program RAM	2 x 12KB
MCE Program OTP	16KB
GateKill latency (digital filtered)	2 µsec
PWM carrier frequency	20 bits/ SYSCLK
A/D input channels	15
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6K bps
Number of digital I/O (max)	31
Package (lead free)	QFP100
Typical 3.3V operating current	50mA

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRMCF588	LQFP100	Tray	900	IRMCF588QTY
		Tape & Reel	1000	IRMCF588QTR

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1 Overview

IRMCF588 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete two motor inverterized appliance motor control applications. Particular application includes a full DC inverter Air Conditioner which requires two motor sensorless control plus power factor control. Unlike a traditional microcontroller or DSP, the IRMCF588 provides a built-in two parallel running computation engines for two closed loop sensorless control algorithm using the unique Flexible Motion Control Engine (MCE™). The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCF588 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC, while still supporting leg shunt current sensing. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging. Figure 1 shows a typical application schematic using the IRMCF588 in leg shunt mode.

IRMCF588 contains 64K bytes of Flash program memory plus 16K bytes of OTP memory and comes in a 100-pin QFP package.

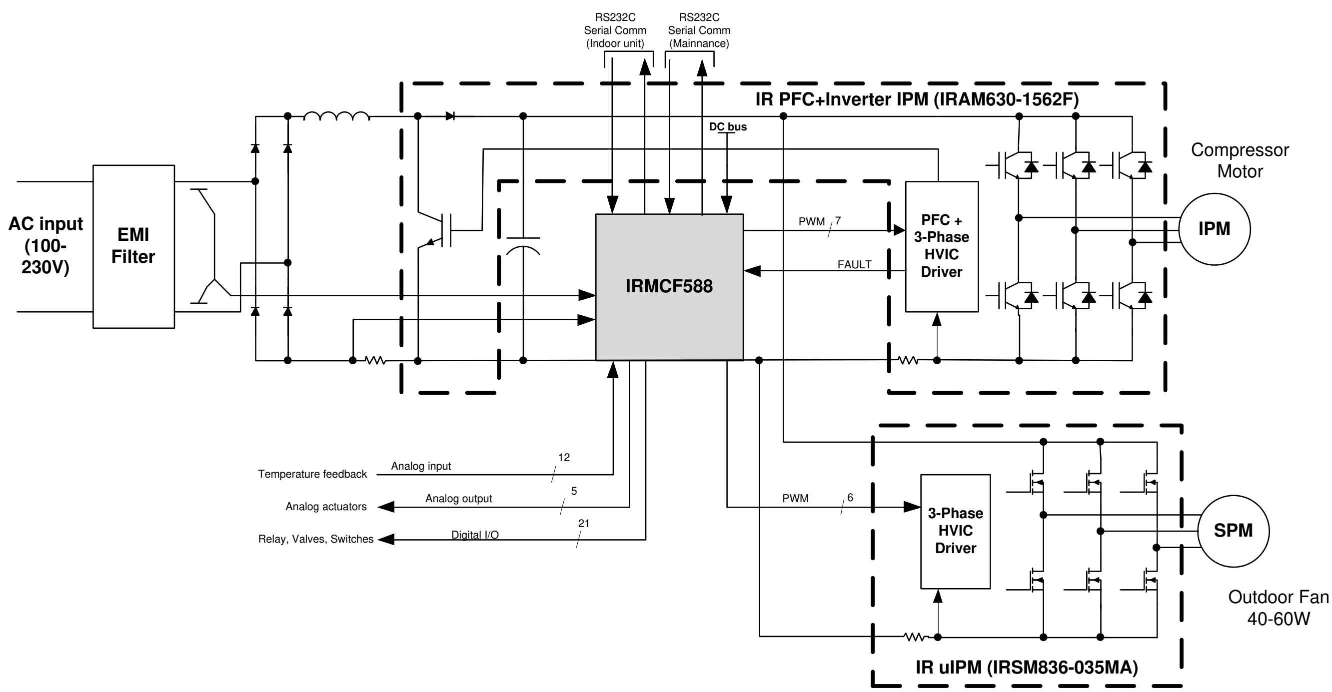

Figure 1. Typical Application Block Diagram Using IRMCF588

2 Pinout

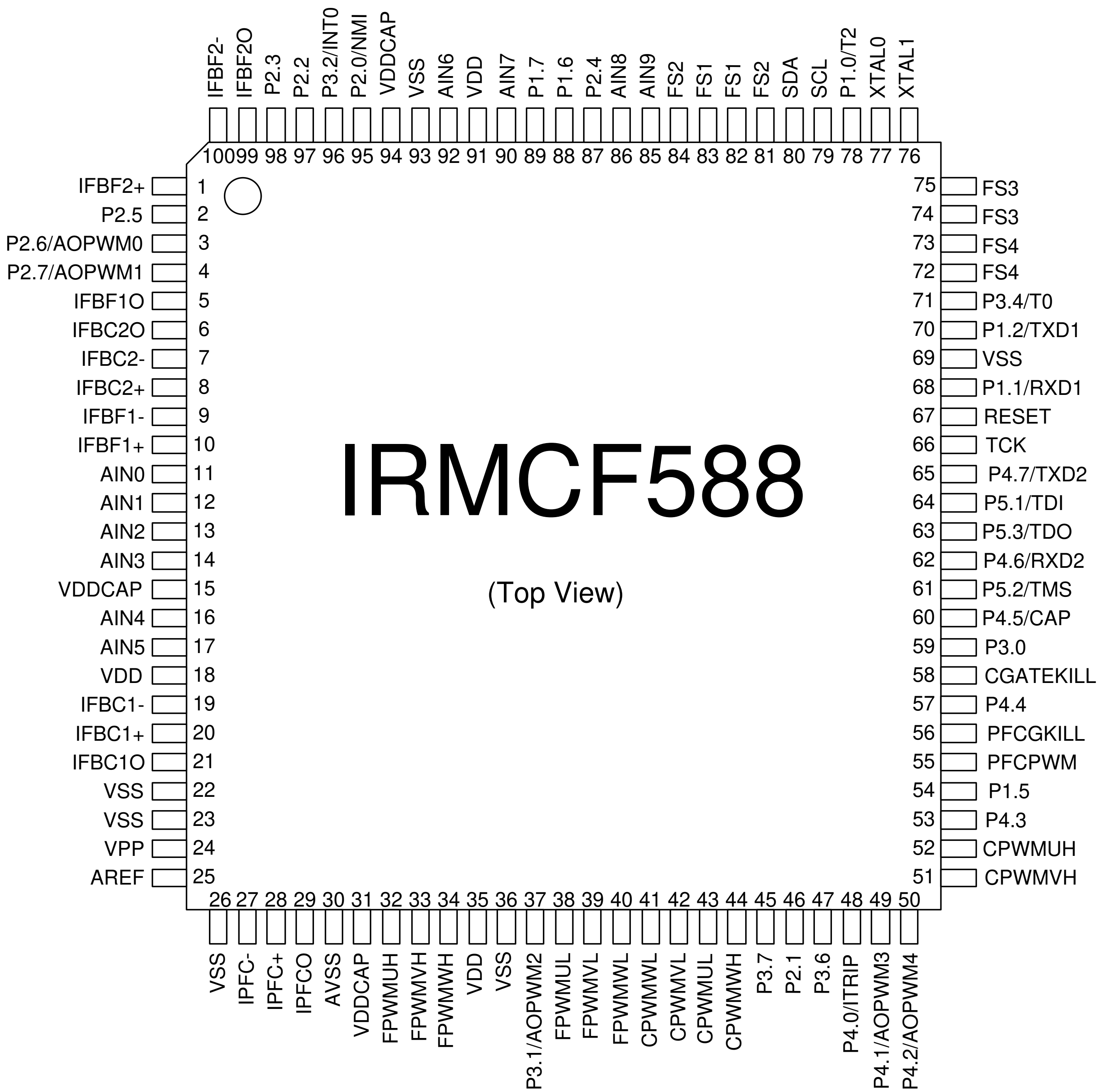

Figure 2. Pinout of IRMCF588

3 IRMCF588 Block Diagram and Main Functions

IRMCF588 block diagram for leg shunt mode is shown in Figure 3.

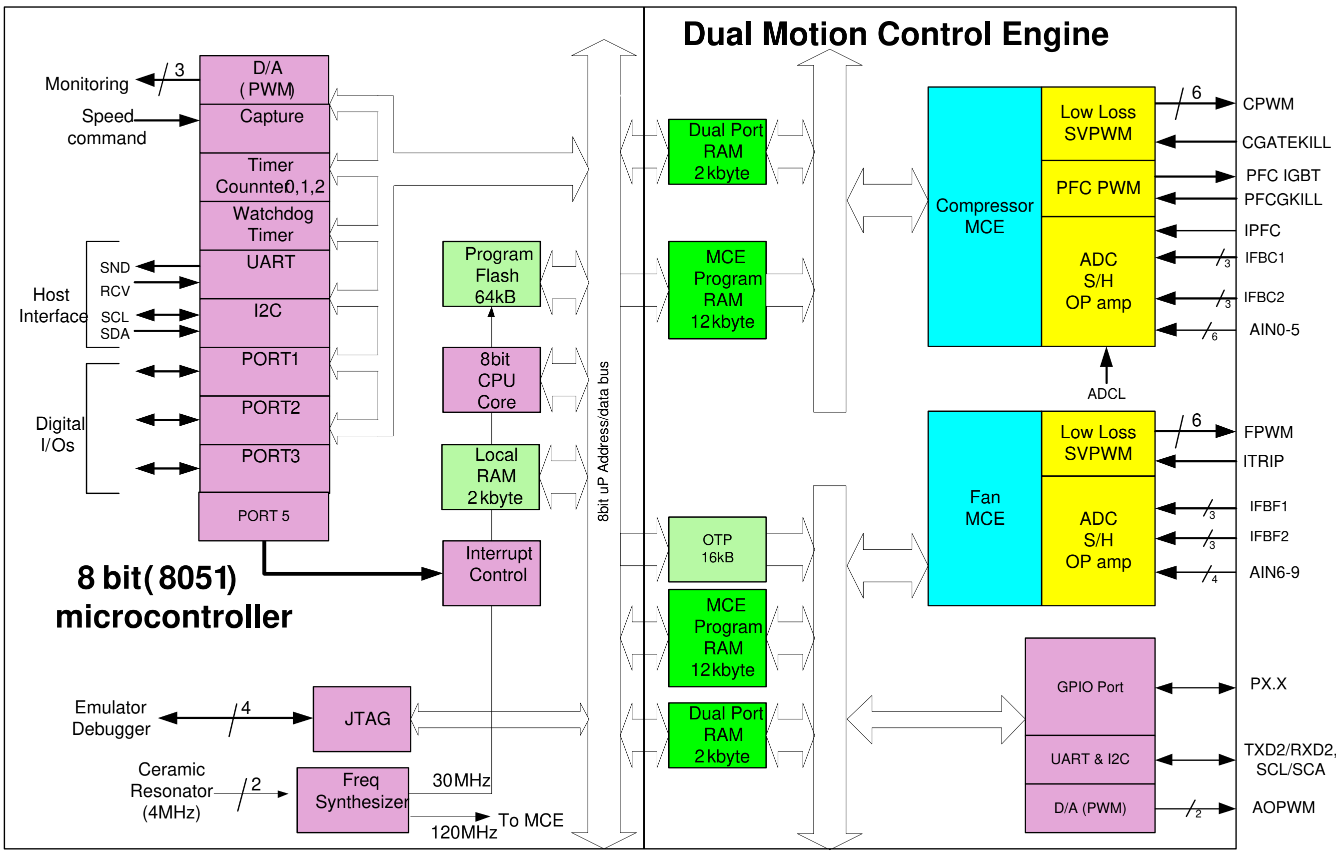

Figure 3. IRMCF588 Block Diagram

IRMCF588 contains the following functions for sensorless AC motor control applications:

Motion Control Engine (MCE™)

- Sensorless FOC (complete sensorless field oriented control)
- Proportional plus Integral block
- Low pass filter
- Differentiator and lag (high pass filter)
- Ramp
- Limit
- Angle estimate (sensorless control)
- Inverse Clark transformation
- Vector rotator
- Bit latch
- Peak detect
- Transition
- Multiply-divide (signed and unsigned)

8051 microcontroller

- Two 16 bit timer/counters
- One 16 bit periodic timer
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 31 discrete digital I/Os
- Ten-channel 12 bit A/D
  - Buffered (current sensing) three channels (0 – 1.2V input)
  - Unbuffered seven channels (0 – 1.2V input)
- JTAG port (4 pins)
- Up to five channels of analog output (8 bit PWM)
- UART

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- I^2C port
- Dual MCE™ control sequencer
- Adder
- MCE™ program memory (12 K byte X 2)
- Divide (signed and unsigned)
- Subtractor
- Comparator
- Counter
- Accumulator
- Switch
- Shift
- ATAN (arc tangent)
- Function block (any curve fitting, nonlinear function)
- 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- 64K byte Flash memory
- 2K byte data RAM

4 Application connection and Pin function

Figure 4 shows the application connections in single shunt mode. Figure 5 shows the analog front end diagram with a single shunt configuration.

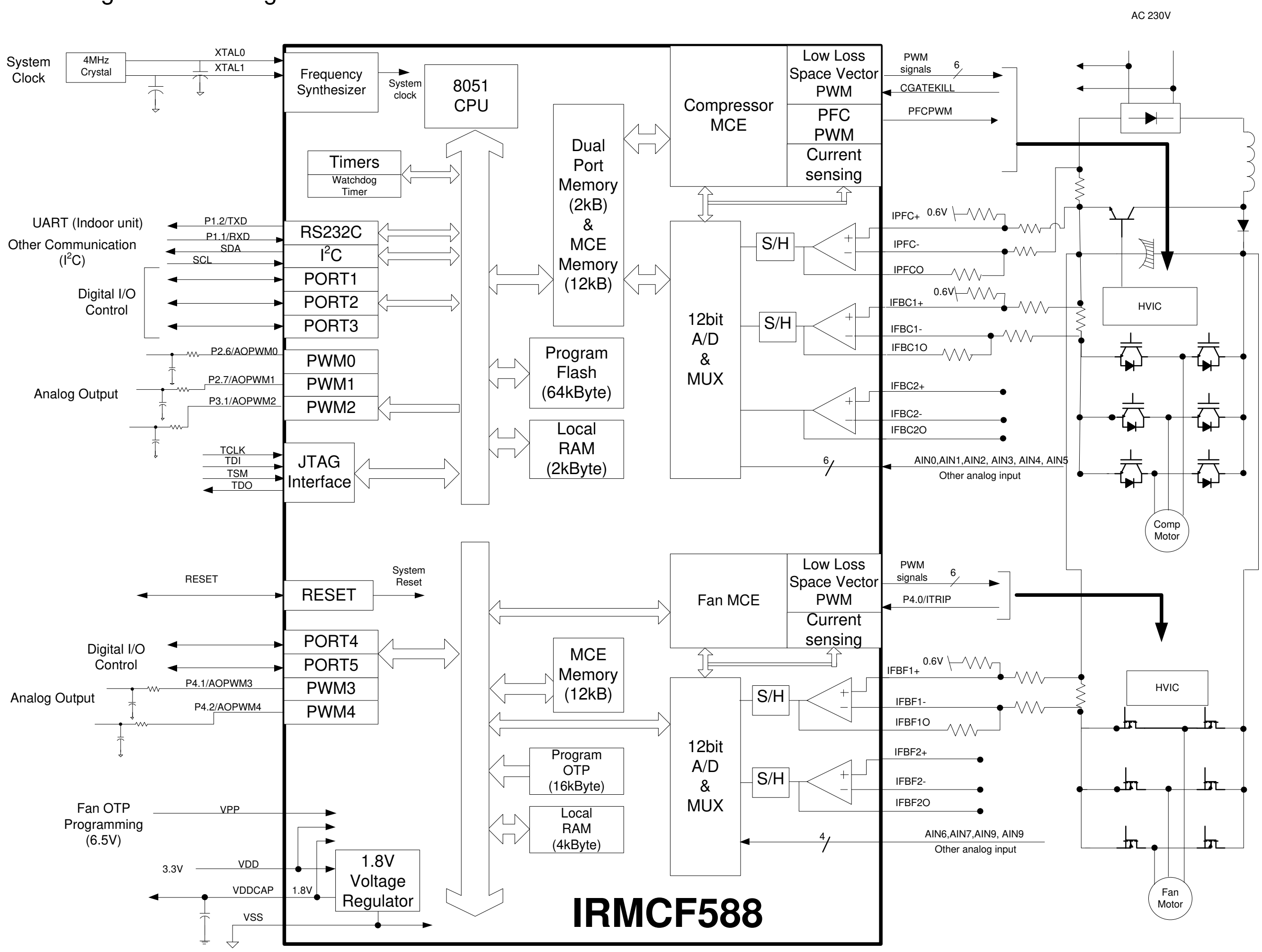

Figure 4. IRMCF588 Single Shunt Connection Diagram

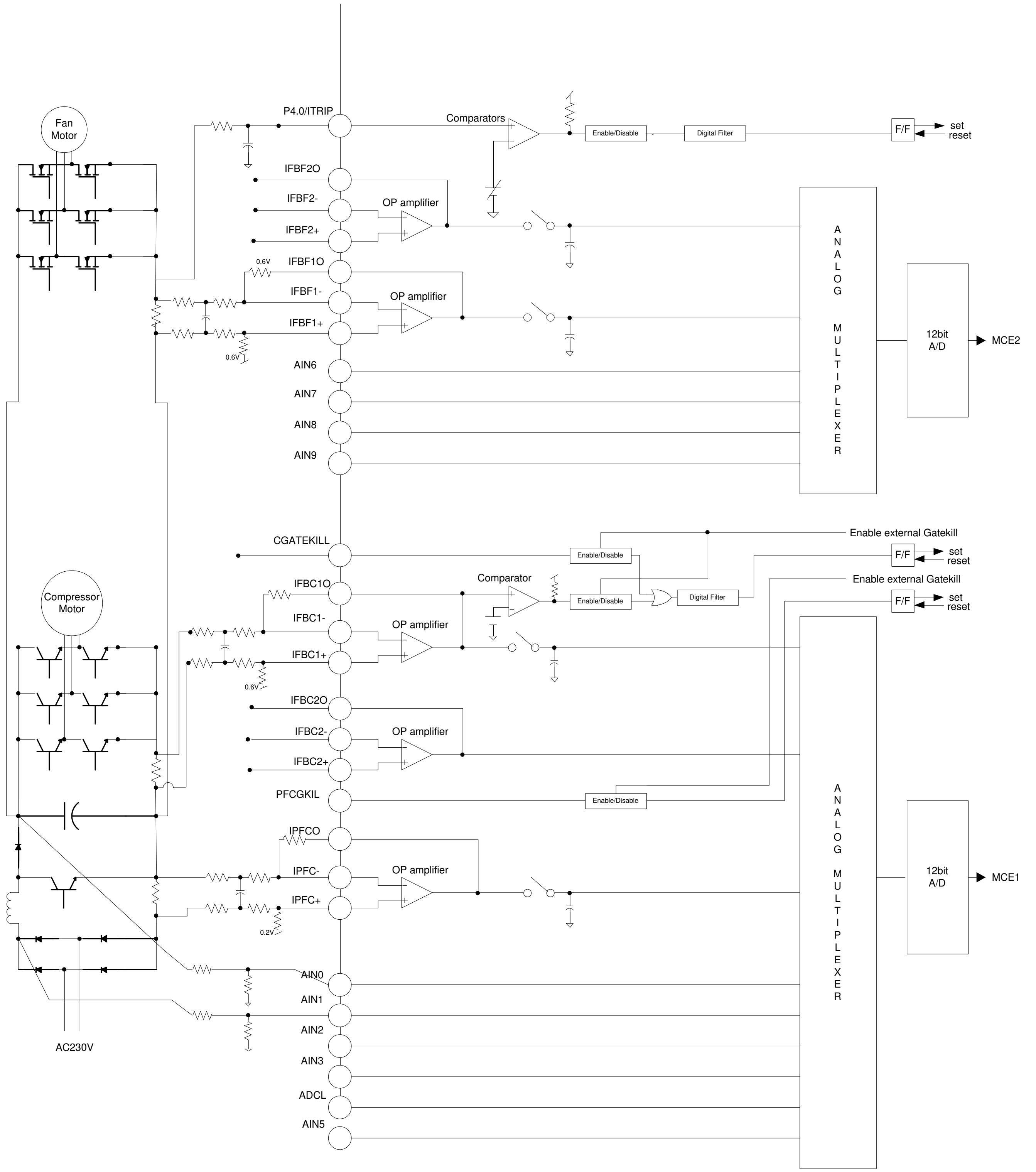

Figure 5. IRMCF588 Analog Front End Diagram

4.1 8051 Peripheral Interface Group

UART Interface

P1.2/TXD	Output, Channel 1 Transmit data from IRMCF588
P1.1/RXD	Input, Channel 1 Receive data to IRMCF588
P4.6/TXD2	Output, Channel 2 Transmit data from IRMCF588
P4.7/RXD2	Input, Channel 2 Receive data to IRMCF588

Discrete I/O Interface

P1.0/T2	Input/output port 1.0, can be configured as Timer/Counter 2 input
P1.1/RXD	Input/output port 1.1, can be configured as RXD input
P1.2/TXD	Input/output port 1.2, can be configured as TXD output
P1.5	Input/output port 1.5
P1.6	Input/output port 1.6
P1.7	Input/output port 1.6
P2.0/NMI	Input/output port 2.0, can be configured as non-maskable interrupt input
P2.1	Input/output port 2.1
P2.2	Input/output port 2.2
P2.3	Input/output port 2.3
P2.4	Input/output port 2.4
P2.5	Input/output port 2.5
P2.6/AOPWM0	Input/output port 2.6, can be configured as AOPWM0 output
P2.7/AOPWM1	Input/output port 2.7, can be configured as AOPWM1 output
P3.0	Input/output port 3.0
P3.1/AOPWM2	Input/output port 3.1, can be configured as AOPWM2 output
P3.2/INT0	Input/output port 3.2, can be configured as INT0 input
P3.4/T0	Input/output port 3.4, can be configured as T0 input for counter mode
P3.6	Input/output port 3.6
P3.7	Input/output port 3.7
P4.0/ITRIP	Input/output port 4.0, can be configured as overcurrent trip input for Fan motor
P4.1/AOPWM3	Input/output port 4.1, can be configured as AOPWM3 analog output
P4.2/AOPWM4	Input/output port 4.2, can be configured as AOPWM4 analog output
P4.3	Input/output port 4.3
P4.4	Input/output port 4.4
P4.5/CAP	Input/output port 4.5, can be configured as Capture Timer input
P4.6/TXD2	Input/output port 4.6, can be configured as UART2 transmit
P4.7/RXD2	Input/output port 4.7, can be configured as UART2 receive
P5.1/TDI	Input port 5.1, configured as JTAG port by default
P5.2/TMS	Input port 5.2, configured as JTAG port by default
P5.3/TDO	Output port 5.3, configured as JTAG port by default

Analog Output Interface

P2.6/AOPWM0	Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency
P2.7/AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency
P3.1/AOPWM2	Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency
P4.1/AOPWM3	Input/output, can be configured as 8-bit PWM output 3 with programmable carrier frequency
P4.2/AOPWM4	Input/output, can be configured as 8-bit PWM output with programmable carrier frequency

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Crystal Interface

XTAL0	Input, connected to crystal
XTAL1	Output, connected to crystal

Reset Interface

RESET	Input and Output, system reset, doesn't require external RC time constant

I²C Interface

SCL	Output, I²C clock output
SDA	Input/output, I²C Data line

4.2 Motion Peripheral Interface Group

PWM

CPWMUH	Output, Compressor motor PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMUL	Output, Compressor motor PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMVH	Output, Compressor motor PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMVL	Output, Compressor motor PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMWH	Output, Compressor motor PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMWL	Output, Compressor motor PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PFCPWM	Output, Compressor motor PFCPWM output signal, internally pulled up by 70kΩ, configured low true at a power up
FPWMUH	Output, Fan motor PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMUL	Output, Fan motor PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMVH	Output, Fan motor PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMVL	Output, Fan motor PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMWH	Output, Fan motor PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMWL	Output, Fan motor PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up

Fault

CGATEKILL	Input, upon assertion this negates all six PWM signals, active low, internally pulled up by 70kΩ
PFCGKILL	Input, upon assertion, this negates PFCPWM signal, active low, internally pulled up by 70kΩ
P4.0/ITRIP	Input/output port 4.0, can be configured as overcurrent trip input for Fan motor according to the setting of active_pol register, pulled up by 49kOhm internal resistor

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4.3 Analog Interface Group

AVSS	Analog power return, (analog internal 1.8V power is shared with VDDCAP)
AREF	0.6V buffered output
IFBC1+	Input, Operational amplifier positive input for compressor motor shunt sensing
IFBC1-	Input, Operational amplifier negative input for compressor motor shunt sensing
IFBC1O	Output, Operational amplifier output for compressor motor shunt sensing
IFBC2+	Input, Operational amplifier positive input for compressor motor leg shunt sensing
IFBC2-	Input, Operational amplifier negative input for compressor motor leg shunt sensing
IFBC2O	Output, Operational amplifier output for compressor motor leg shunt sensing
IPFC+	Input, Operational amplifier positive input for PFC current sensing
IPFC-	Input, Operational amplifier negative input for PFC current sensing
IPFCO	Output, Operational amplifier output for PFC current sensing
IFBF1+	Input, Operational amplifier positive input for Fan motor shunt sensing
IFBF1-	Input, Operational amplifier negative input for Fan motor shunt sensing
IFBF1O	Output, Operational amplifier output for Fan motor shunt sensing
IFBF2+	Input, Operational amplifier positive input for Fan motor leg shunt sensing
IFBF2-	Input, Operational amplifier negative input for Fan motor leg shunt sensing
IFBF2O	Output, Operational amplifier output for Fan motor leg shunt sensing
AIN0	Input, DC voltage sensing or Analog input channel 0 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN1	Input, AC Input voltage sensing or Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN2	Input, Analog input channel 2 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN3	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN4	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN5	Input, Analog input channel 5 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN6	Input, Analog input channel 6 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN7	Input, Analog input channel 7 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN8	Input, Analog input channel 8 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN9	Input, Analog input channel 9 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused

Analog Channel	Leg Shunt Mode	Single Shunt Mode	Pin number(s)
IPFC	PFC Current	PFC Current	27,28,29
IFBC1	Motor U Phase Current	Motor Shunt Current	19,20,21
IFBC2	Motor V Phase Current	-	6,7,8
AIN1	AC Voltage	AC Voltage	12

Table 1. Analog channel sensing functions in Leg and Single Shunt Modes

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4.4 Power Interface Group

VDD	Digital power (3.3V)
VDDCAP	Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally **Note:** The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	System common

4.5 Test Interface Group

P5.2/TMS	JTAG test mode input or input digital port for compressor MCE
P5.3/TDO	JTAG data output port for compressor MCE
P5.1/TDI	JTAG data input, or input digital port for compressor MCE
TCK	JTAG test clock port for compressor MCE

4.6 Factory use Group

FS1	Pin82 and Pin83 need to be connected and pulled up by 4.7K resistor for factory purpose
FS2	Pin81 and Pin84 need to be connected and pulled up by 4.7K resistor for factory purpose
FS3	Pin74 and Pin75 need to be connected and pulled up by 4.7K resistor for factory purpose
FS4	Pin73 and Pin72 need to be connected and pulled up by 4.7K resistor for factory purpose

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5 DC Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V_{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V_{ID}	Digital Input Voltage	-0.3 V	-	6.0 V	Respect to VSS
T_A	Ambient Temperature	-40 ˚C	-	85 ˚C	
T_S	Storage Temperature	-65 ˚C	-	150 ˚C	

Table 2. Absolute Maximum Ratings

Caution: Stresses beyond those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

5.2 System Clock Frequency and Power Consumption

C_{AREF} = 1nF, C_{MEXT}= 100nF. VDD=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
SYSCLK	System Clock	32	-	120	**MHz**
P_D	Power consumption		150[1]	-	**mW**

Table 3. System Clock Frequency

Note
1) The value is based on the condition of MCE clock=100MHz, 8051 clock 20MHz with an actual motor and PFC running by a typical MCE application program and 8051 code.

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5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{IL}	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		3.6 V	Recommended
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
I_L	Input leakage current		±10 nA	±1 µA	V_O = 3.3 V or 0 V
I_{OL1} (2)	Low level output current	8.9 mA	13.2 mA	15.2 mA	V_{OL} = 0.4 V (1)
I_{OH1} (2)	High level output current	12.4 mA	24.8 mA	38 mA	V_{OH} = 2.4 V (1)
I_{OL2} (3)	Low level output current	17.9 mA	26.3 mA	33.4 mA	V_{OL} = 0.4 V (1)
I_{OH2} (3)	High level output current	24.6 mA	49.5 mA	81 mA	V_{OH} = 2.4 V (1)

Table 4. Digital I/O DC Characteristics

Note:
(1) Data guaranteed by design.
(2) Applied to SCL, SDA pins.
(3) Applied to all digital I/O pins except SCL and SDA pins.

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5.4 Analog I/O DC Characteristics

- OP amps for compressor, fan and PFC current sensing

C_{AREF} = 1nF. VDD=3.3V, Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{OFFSET}	Input Offset Voltage	-	-	26 mV	V_{AVDD} = 1.8 V
V_I	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV (1)	-	1.2 V	V_{AVDD} = 1.8 V
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
R_{FDBK}	OP amp feedback resistor	5 kΩ	-	20 kΩ	Requested between IFBO and IFB-
OP_{GAINCL}	Operating Close loop Gain	80 db	-	-	(1)
CMRR	Common Mode Rejection Ratio	-	80 db	-	(1)
I_{SRC}	Op amp output source current	-	1 mA	-	V_{OUT} = 0.6 V (1)
I_{SNK}	Op amp output sink current	-	100 µA	-	V_{OUT} = 0.6 V (1)
V_{min}	Min Voltage for Ain 0 -9	60 mV	NA	NA	(1)

Table 5. Analog I/O DC Characteristics

Note:
(1) Data guaranteed by design.

5.5 A/D Accuracy

Unless specified, Ta = 25˚C.
A/D accuracy for current sensing (IFBC1+,IFBC1-,IFBC1O, IFBC2+,IFBC2-,IFBC2O, IFBF1+,IFBF1-,IFBF1O, IFBF2+,IFBF2-,IFBF2O,IPFC+,IPFC-,IPFCO), and analog input channels (AIN0-AIN9)

Symbol	Parameter	Min	Typ	Max	Condition
ADC_{error}	Error is the difference between ideal counts and compensated counts for any applied voltage in 0-1.2V range	-	±10Counts	-	(1)

Table 5. A/D Accuracy

Note:
(1) Characterized not tested at manufacturing.

5.5 Under Voltage Lockout DC characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
UV_{CC+}	UVcc positive going Threshold	2.78 V	3.04 V	3.23 V	(1)
UV_{CC-}	UVcc negative going Threshold	2.78 V	2.97 V	3.23 V	

$UV_{CC}H$	UVcc Hysteresys	-	73 mV	-	(1)

Table 6. UVcc DC Characteristics

Note:
(1) Data guaranteed by design.

5.6 Itrip comparator DC characteristics

Unless specified, VDD=3.3V, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
$Itrip_+$	Itrip positive going Threshold	-	1.22V	-	V_{DD} = 3.3 V
$Itrip_-$	Itrip negative going Threshold	-	1.10V	-	V_{DD} = 3.3 V
ItripH	Itrip Hysteresys	-	120mV	-	

Table 7. Itrip DC Characteristics

5.7 AREF Characteristics

C_{AREF} = 1nF. Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{AREF}	Buffer Output Voltage	-	600 mV	-	V_{VDD} = 3.3 V
ΔV_o	Load regulation (V_{DC}-0.6)	-	1 mV	-	(1)
PSRR	Power Supply Rejection Ratio	-	75 db	-	(1)

Table 8. CMEXT and AREF DC Characteristics

Note:
(1) Data guaranteed by design.

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6 AC Characteristics

6.1 Digital PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLKIN}	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	(1) (see figure below)
F_{PLL}	Internal clock frequency	32 MHz	50 MHz	128 MHz	(1)
F_{LWPW}	Sleep mode output frequency	$F_{CLKIN} \div 256$	-	-	(1)
J_S	Short time jitter	-	200 psec	-	(1)
D	Duty cycle	-	50 %	-	(1)
T_{LOCK}	PLL lock time	-	-	500 µsec	(1)

Table 9. PLL AC Characteristics

Note:
(1) Data guaranteed by design.

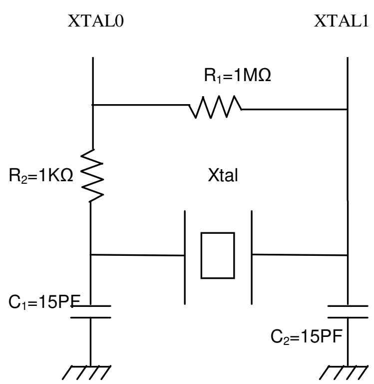

Figure 6. Crystal circuit example

6.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 µsec	(1)
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 µsec	Voltage droop ≤ 15 LSB (see figure below)

Table 10 . A/D Converter AC Characteristics

Note:
(1) Data guaranteed by design.

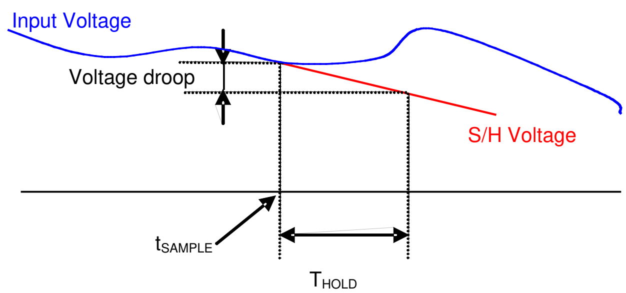

Figure 7. Voltage droop and S/H hold time

6.3 Op amp AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/µsec	-	VDD = 3.3 V, CL = 33 pF (1)
OP_{IMP}	OP input impedance	-	10^8 Ω	-	(1) (2)
T_{SET}	Settling time	-	400 ns	-	VDD = 3.3 V, CL = 33 pF (1)

Table 11 Current Sensing OP Amp AC Characteristics

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 8. Here typical OP amp connection is shown but all op amp outputs should be loaded with this capacitor value.

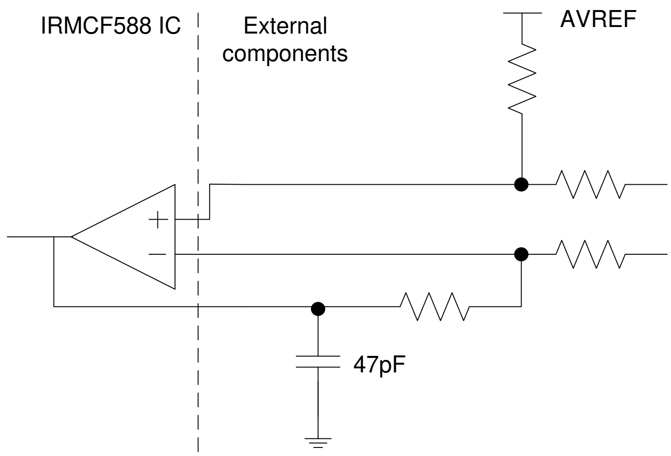

Figure 8. Op amp output capacitor

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6.4 SYNC to SVPWM and A/D Conversion AC Timing

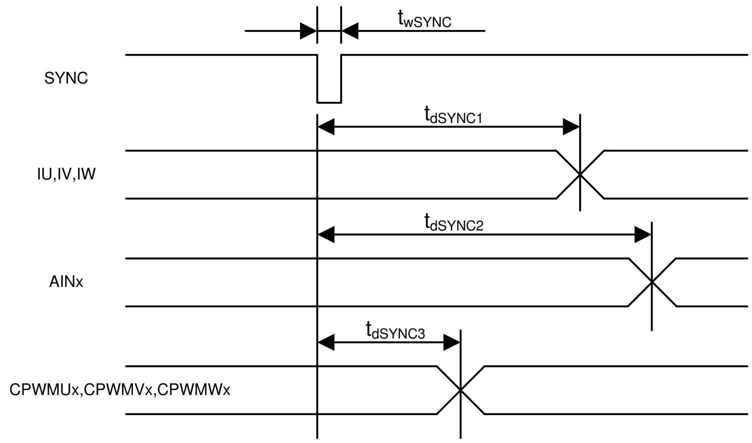

Figure 9. SYNC timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wSYNC}	SYNC pulse width	-	32	-	SYSCLK
t_{dSYNC1}	SYNC to current feedback conversion time	-	-	100	SYSCLK
t_{dSYNC2}	SYNC to AIN0-9	-	-	200	SYSCLK (1)
t_{dSYNC3}	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 12. SYNC AC Characteristics

Note:

(1) Only any 3 AINx from the compressor AIN channels (AIN0 -AIN6) and any 2 AINx (AIN7 - AIN9) from the fan AIN channels are converted once every SYNC events at the same time and the rest of the channels will be sampled once every 5 SYNC events.

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6.5 GATEKILL to SVPWM AC Timing

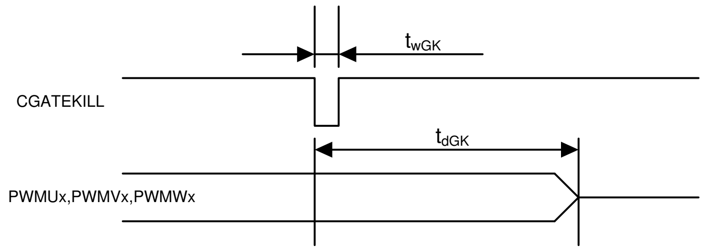

Figure 10. Gatekill timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	GATEKILL pulse width	32	-	-	SYSCLK
t_{dGK}	GATEKILL to PWM output delay	-	-	100	SYSCLK

Table 13. GATEKILL to SVPWM AC Timing

6.6 Internal Overcurrent trip AC Timing

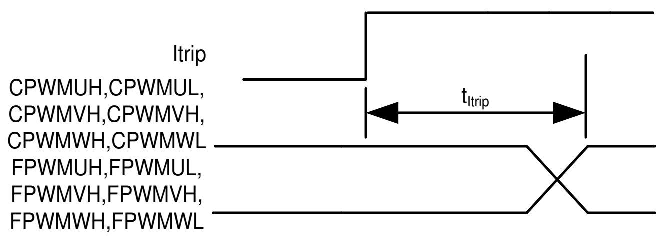

Figure 11. ITRIP timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ITRIP}	Itrip propagation delay	-	-	100(sysclk)+1.0usec	SYSCLK+usec

Table 14. Itrip AC Timing

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6.7 Interrupt AC Timing

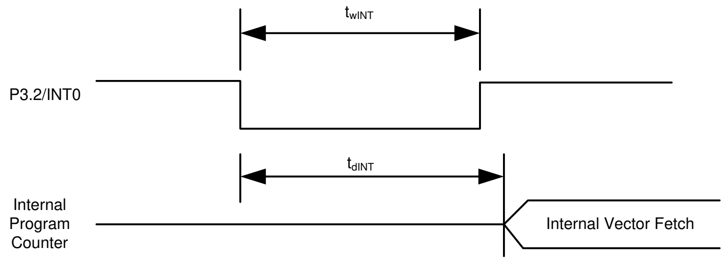

Figure 12. Interrupt timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wINT}	INT0, NMI Interrupt Assertion Time	4	-	-	SYSCLK
t_{dINT}	INT0, NMI latency	-	-	4	SYSCLK

Table 15. Interrupt AC Timing

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6.8 I²C AC Timing

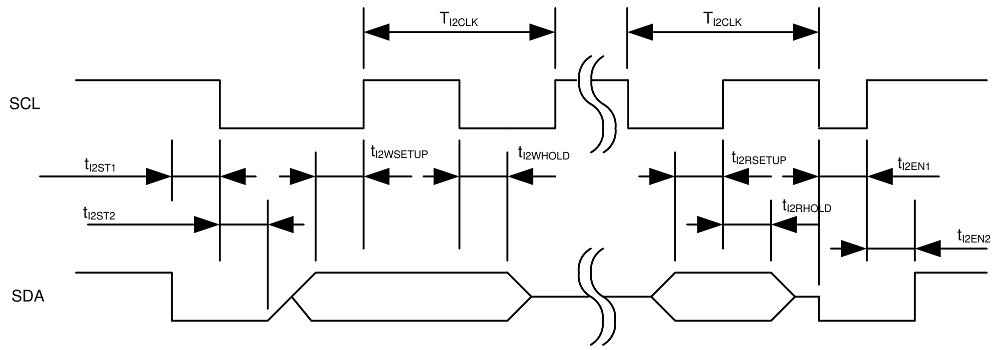

Figure 13. I²C Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{I2CLK}	I²C clock period	10	-	8192	SYSCLK
t_{I2ST1}	I²C SDA start time	0.25	-	-	T_{I2CLK}
t_{I2ST2}	I²C SCL start time	0.25	-	-	T_{I2CLK}
$t_{I2WSETUP}$	I²C write setup time	0.25	-	-	T_{I2CLK}
$t_{I2WHOLD}$	I²C write hold time	0.25	-	-	T_{I2CLK}
$t_{I2RSETUP}$	I²C read setup time	I²C filter time(1)	-	-	SYSCLK
$t_{I2RHOLD}$	I²C read hold time	1	-	-	SYSCLK

Table 16. I²C AC Timing

Note:
(1) I²C read setup time is determined by the programmable filter time applied to I²C communication.

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