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International
IOR Rectifier

International
IOR Rectifier

Data Sheet No. PD60225 Rev B

IRMCK203

High Performance Sensorless Motion Control IC

Features

- **Complete Sensorless control IC for Permanent Magnet AC motors**
- **No phase voltage feedback sensing required**
- **Sinusoidal current waveform with Synchronously Rotating Frame closed loop current control**
- **High starting torque and smooth speed ramping**
- **Direct interface to IR2175 current sensing high voltage IC**
- **Auto Retry at startup with configurable starting torque**
- **Versatile loss minimization Space Vector PWM**
- **Serial communication interface (RS232C, RS422, SPI)**
- **I^{2}C serial interface to 1k bit serial EEPROM for parameter storage for stand alone operation**
- **Phase loss/Overcurrent/Overvoltage protection**
- **7-bit discrete I/O for sequencing and status monitor**
- **Integrated brake IGBT control for dc bus voltage limitation**
- **ServoDesigner™ tool for easy operation**
- **Parallel interface for microcontroller expansion**

Product Summary

Max Clock input	33.3 MHz
Sensorless control computation time	10 µsec max
Speed operating range (typical)	5% to 100%
Speed control resolution	15 bit full range
Adjustable current limit at start-up	15 bit full range
Programmable retry on start-up	max 16 trials
Over current, speed, phase loss, dc bus fault protection	
PWM carrier frequency	16 bit/33MHz
IR2175 Current feedback data resolution	10bit
Inverter leg current sensing (optional)	12bit
RS232C speed	up to 57.6 Kbps
Optional RS422 communication	up to 1 Mbps
Max SPI Clock	8 MHz

Package: QFP80

Description

IRMCK203 is a high performance digital motion control IC for Sensorless AC permanent magnet motor application. Control is based on closed loop vector control for sinusoidal Back EMF motors. With IRMCK203, the users can readily build a high performance Sensorless drive system without any programming effort and minimum start-up time. Built-in unique start-up and ramping algorithm enables wide application. This IC is versatile enough that the users can configure and optimize system performance according to the needs of each application. With International Rectifier iMOTION products including high voltage ICs such as IR2175 current sensing IC and IRAM series of Intelligent IGBT module in combination with IRMCK203, the end result is a fully optimized system with reduced electronics component counts. This simplifies the design for low cost Sensorless drive modules. IRMCK203 can be easily adapted to various permanent magnet motors through ServoDesigner™ tool, which is the fully configurable graphic user interface tool.

Overview

IRMCK203 is a new International Rectifier integrated circuit device designed for one-chip solution for complete closed loop current and velocity control of a high performance Sensorless drive for PM motors. Unlike a traditional microcontroller or DSP, IRMCK203 does not require any programming to complete complex Sensorless algorithm development. Combined with International Rectifier's high voltage gate drive and current sensing IC, the user can implement complete speed control of PM motors with minimum component count and virtually no design effort. In addition to Sensorless closed loop speed control operation, features such as Start-up retry, Phase Loss detection, Low Loss PWM, Regeneration Braking control and various drive protections are all implemented inside IRMCK203. Analog and digital I/Os can also be configured. Host communication logic contains Asynchronous Communication Interface for RS232C or RS422 communication interface, a fast slave SPI interface and an 8 bit wide Host Parallel Interface. All communication ports have the same access capability to the host register set. The users can write to, and read from the predefined registers to configure and monitor the drive through these communication ports.

IRMCK203 Main functions

- Complete closed loop current control based on Synchronously Rotating Frame Field Orientation (using Rotor Angle Observer)
- Closed loop velocity control based on estimated speed
- Configurable parameters (PI controller gains, PI output limit range, current feedback scaling, PWM carrier frequency) provide adaptation to various PM motors
- Built-in Sensorless control logic for start-up, ramping, and running conditions
- Auto Retry (programmable) on start-up with configurable torque current limit
- Analog reference input (can be used for speed reference)
- RS232C/RS422 reference input
- Full dynamic braking control for DC bus voltage limitation
- Cycle-by-cycle on/off Control for Brake IGBT
- Loss minimization Space Vector PWM with deadtime insertion
- Build-in two IR2175 current sensing IC interfaces
- Phase Loss, Overcurrent (GATEKILL input), Overvoltage, Undervoltage, Overspeed protection
- Low cost serial 12bit A/D interface with multiplexer and sample/hold circuit
- Optional Inverter Leg (low side) current sensing in lieu of IR2175 IC
- 4 channel analog output (PWM)
- Local EEPROM for startup initialization of internal data/parameters through host register interface
  AT24C01A, 128X8
- Versatile host communication interface
  RS232C or RS422 host interface
  Fast SPI slave host interface with multi-drop capability
  Parallel Host interface (total 12 pins)
- Multiplexed data/address bus
  Address Enable
  RD/WR
- Discrete I/Os for Standalone mode operation
  STARTSTOP (Input)
  ESTOP (Input)

DIR (Input)
FLTCLR (Input)
FAULT (Output)
SYNC (Output)
REDLED (Output)
GREENLED (Output)

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IRMCK203 Block Diagrams

Basic Block Diagram

Figure 1 shows the basic block diagram of the IRMCK203 surrounded by International Rectifiers' ICs. Host communications are provided over SPI, RS-232C or Host parallel ports. Two current sensing ICs (IR2175) and a three phase high voltage gate drive typically implement the high voltage / current interface between the IRMCK203 IC and motor.

The IRMCK203 can operate in a "stand-alone" mode without the host controller. A serial EEPROM would be utilized to load motor-specific parameters into the IC.

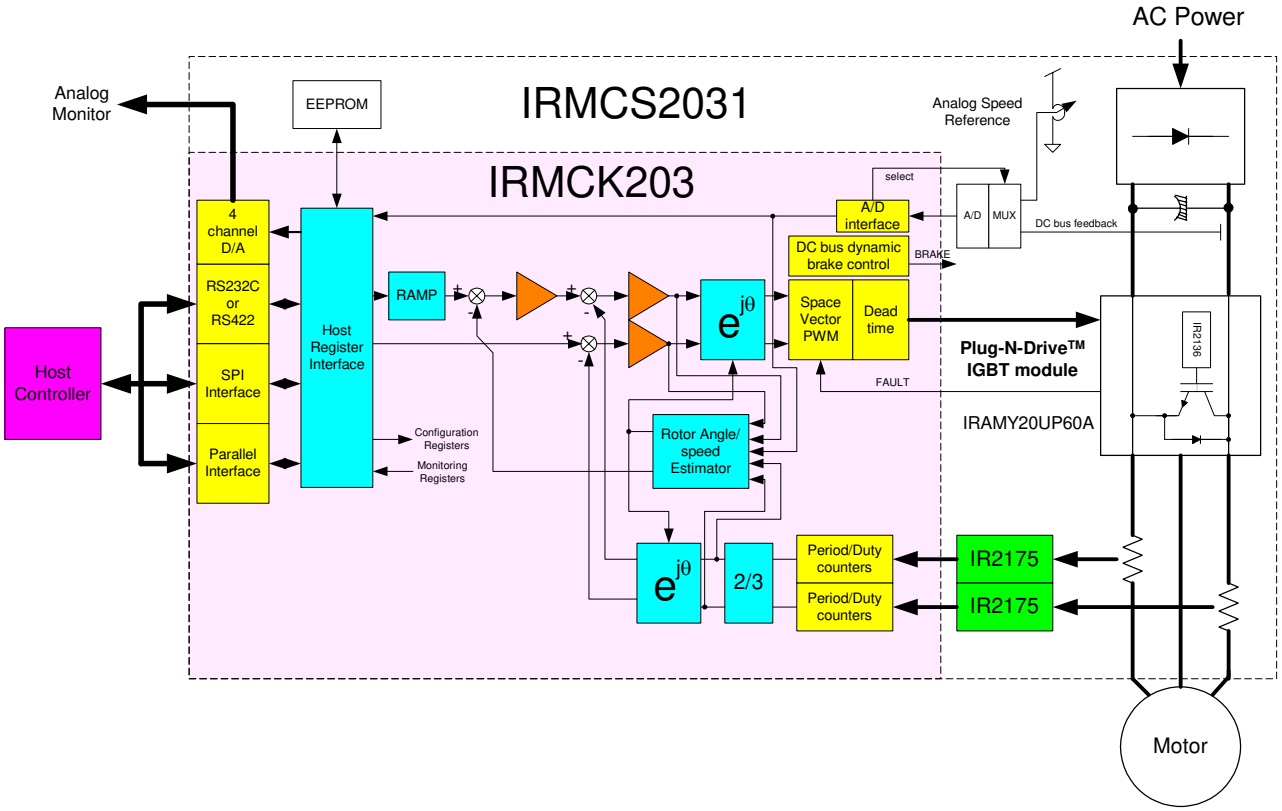

Figure 1: IRMCS2031 Simplified Blocks

Configurable parameters are provided to tailor design to various applications (motor and load). These configurable parameters can be modified via the host register interface through the communication interface. In the IRMCK203 product, a design spread sheet is provided to aid the user for ease of drive start-up, the spread sheet will input high level application data such as motor name plate information, max speed, current limit, speed and current regulator bandwidth, base on this information the program will generate the required configurable parameters. Detail on Drive commissioning is described in the IRMCK203 Application Developer's Guide.

All logic and algorithms are pre-programmed, and the user does not need to make any effort to develop code, alleviating the tedious design process. If needed, the user can configure the drive to tailor the control per specific

needs to meet the required specification. This configuration can be easily done by accessing the host register interface through the communication interface.

Input/Output of IRMCK203

The I/O signals are shown in Figure 2. The interface signals are divided into sub-groups. For detailed pin assignment, please refer to appendix (Pin definition).

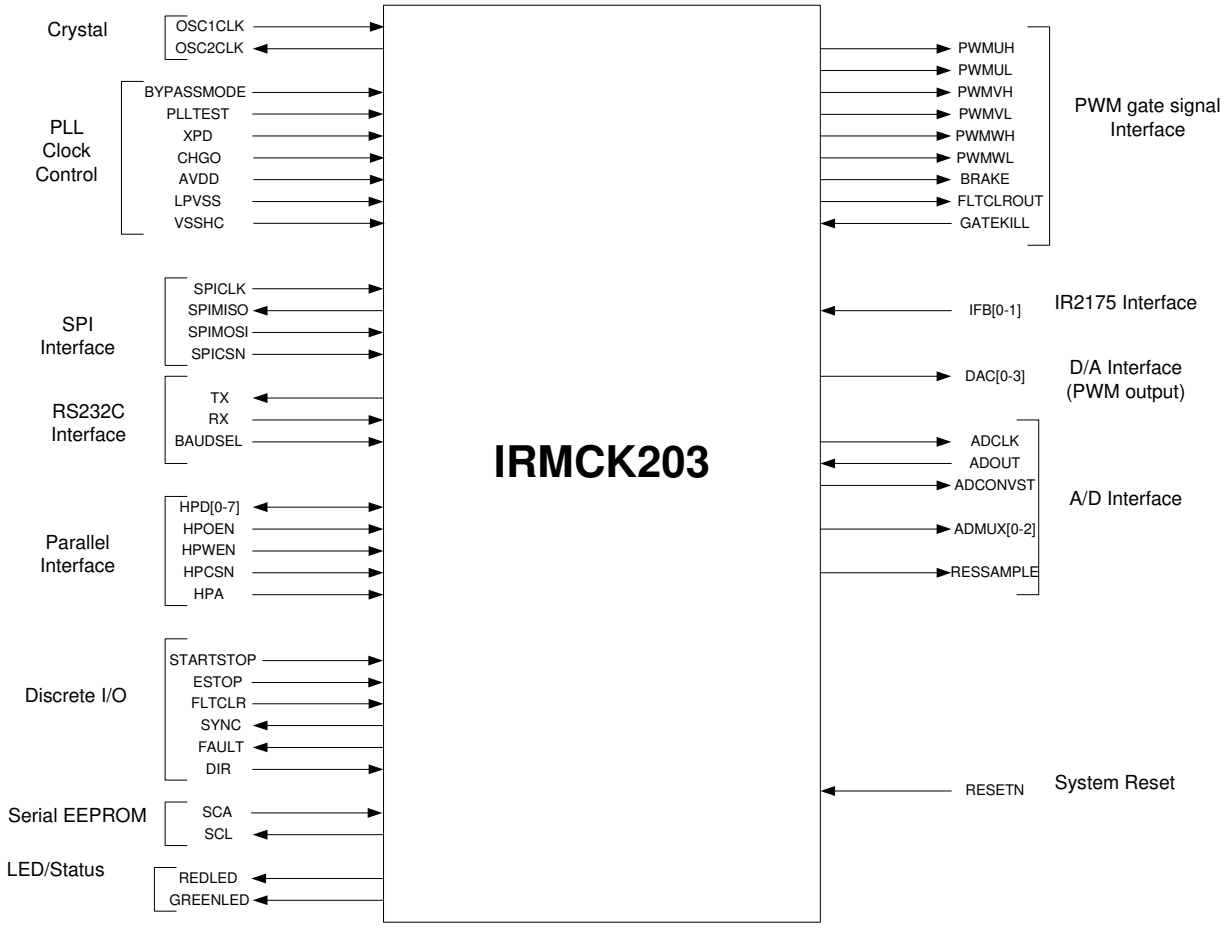

Figure 2: Input/Output of IRMCK203

Host Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
SPICLK	I	Positive edge sensitive	SPI clock
SPIMISO	O	-	Master input and slave output
SPIMOSI	I	-	Master output and slave input
SPICSN	I	L	SPI chip select
HP_nOE	I	L	Parallel data output enable
HP_nWE	I	L	Parallel data write cycle identification
HP_D [7:0]	I/O	-	Parallel data
HP_A	I	H	Parallel data address cycle identification
HP_nCS	I	L	Chip select
TX	O	-	RS-232 data out
RX	I	-	RS-232 data in
BAUDSEL[1:0]	I	H	RS-232 baud rate: 00 = 19.3K bps; 01 = 38.4K bps 10 = 57.6K bps; 11 = 1.031250M bps
SYNC	O	L	Start of PWM cycle
CLK1XOUT	O	-	33.333 MHz output of PLL. This signal has no phase relationship with the OSC1CLK or OSC2CLK inputs.

Discrete I/O Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
STARTSTOP	I	H	Start / Stop command edge sensitive
DIR	I	H	Forward/Reverse Direction command, level sensitive
FAULTCLR	I	H	Fault Clear
ESTOP	I	H	Emergency Stop, state sensitive
PWEN	O	H	PWM enable/disable state
SYNC	O	H	SYNC pulse
FAULT	O	H	Fault state

Motion Peripheral Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
PWMUH	O	-	PWM phase U high side
PWMUL	O		PWM phase U low side
PWMVH	O		PWM phase V high side
PWHVL	O		PWM phase V low side
PWMWH	O		PWM phase W high side
PWMWL	O		PWM phase W low side
BRAKE	O	L	IGBT gate
GATEKILL	I	Varies, Based on Write Register 0x0C Bit 7	When asserted, negates all six PWM signals, host writeable
IFB0	I	-	Channel 0 (phase V)
IFB1	I	-	Channel 1 (phase W)

Analog Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
ADCLK	O	Negative Edge Sensitive	Clock to ADS7818
ADOUT	I	-	Serial data from ADS7818
DAC [3:0]	O	-	Diagnostic DAC
ADCONVST	O	L	Conversion start to ADS7818
RESSAMPLE	O		Sample/hold control signal channel 0 A/D converter
ADMUX0	O	H	Analog input MUX select
ADMUX1	O	H	Analog input MUX select

PLL Interface Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
XPD	I	L	PLL reset
RESETN	I	L	Digital logic reset
BYPASSCLK	I	H	Internal test pin – force to logic low
BYPASSMODE	I	H	Internal test pin – force to logic low
OSC1CLK	I	-	33.33 MHz crystal input
OSC2CLK	I	-	33.33 MHz crystal input
PLLTEST	I	H	Internal test pin – force to logic low
CHGO	I/O	-	Low pass filter
LPVSS	I/O	-	Low pass filter ground

Miscellaneous Group			
Signal	**Input (I) / Output (O)**	**Low (L) / High (H) True Asserted**	**Function**
SCA	I/O	-	EEPROM data
SCL	O	Positive Edge Sensitive	EEPROM clock
GREENLED	O	H	LED signal
REDLED	O	H	LED signal

Power Supply Group	
Signal	**Function**
LVDD	IC Logic +3.3V power supply
AVDD	IC Phase Lock Loop +3.3V analog power supply
MVDD	IC Phase Lock Loop +3.3V digital power supply
VSS	IC Logic power supply return
VSSHC	IC Phase Lock Loop power supply return

Application Connections

Typical application connection is shown in Figure 3. In order to complete a Sensorless drive control, all necessary components are shown in connection to IRMCK203.

Although this is a typical hardware configuration, users can customize the design without the effort of modifying code.

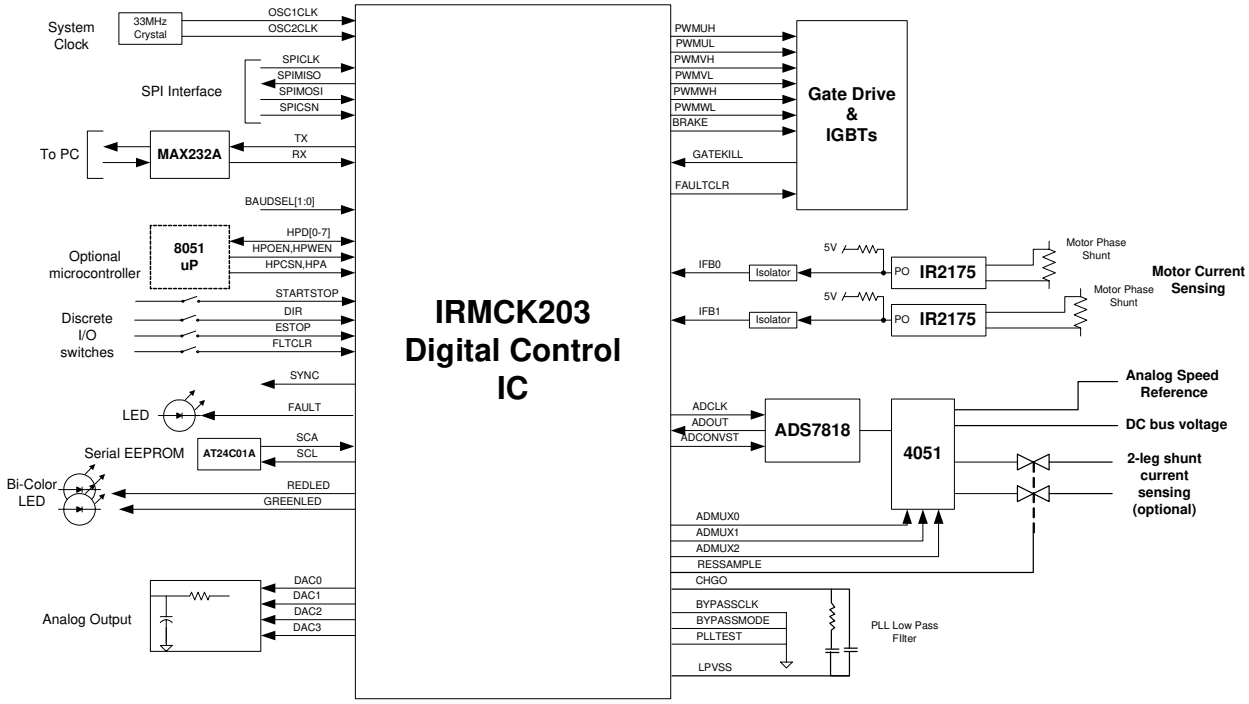

Figure 3: Application Connection of IRMCK203

IC Crystal Clock Circuitry

The clock input to the IC is a 33.33 MHz crystal oscillator. Two shunt capacitors and a possibly a series resistor is required to terminate the crystal to the IC.

The values of the R/C will vary based on actual PCB attributes, and some empirical analysis may be required to get the PLL to start oscillating. Once oscillating, verify that the signal waveform at the OSC1CLK and OSC2CLK pins are sinusoidal rather than trapezoidal. Refer to Table 1 for suggested R/C values. Most low-cost crystals can be used in this application. An example is a Citizen Part number CM309B33.333MABJT available from Digi-Key under part number 300-4160-1-ND.

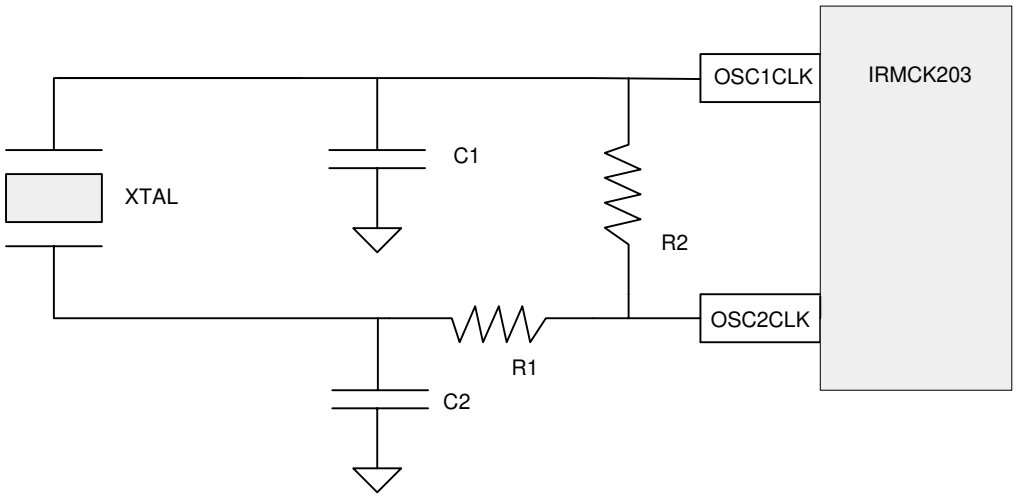

Figure 4: Oscillator Circuit

Component	Value	Units
XTAL	33.33	MHz
C1	5	pF
C2	5	pF
R1	0	Ω
R2	3.9K	Ω

Table 1: Typical Values for the Clock Circuit

PLL Clock Circuitry

The IRMCK203 contains a PLL that creates a 2X and 4X clock from the input 33.33 MHz input clock pin. There are a number of pins on the IC allocated for factory testing purposes that need to be **connected to VSS.** Table 2 shows required PCB signal connections for these pins.

Pin Number	PCB Connection
1	VSS
7	VSS

Table 2: PLL Test Pin Assignments

Low Pass Filter

The low pass filter for this PLL resides between the CHGO and LPVSS pins. Three passive components are required to implement this filter: Cp, Rp and Cs.

Figure 5 shows how to place these components around the IC.

A shield should be placed below Rp, Cp and Cs made out of copper etch.

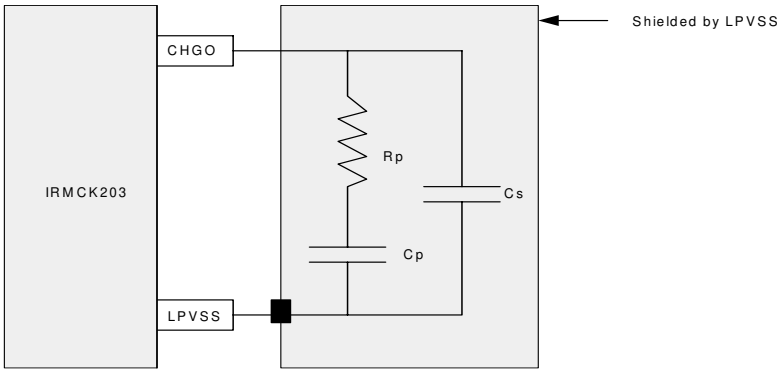

Figure 5: PLL Low Pass Filter Shielding

Implementing the Low Pass Filter Shield

Make all connections between CHGO, Rp, Cp, Cs and LPVSS as short as possible. Create the underlining shield by "copper filling" a larger area in the signal plane of the PCB. Connect this shield to the LPVSS pin of the IC. Do not connect this shield to signal ground (VSS).

Cp Rp and Cs Component Values

For a typical FR4 PCB, the values of the passive components are shown in Table 3.

Component	Value	Units
Rp	3.9K	Ω
Cp	1000	pF
Cs	Not Installed	-

Table 3: PLL Low Pass Filter Values

PLL Reset

There are two reset pins on the IC, XPD and RESETN both low true. XPD holds the PLL circuitry in reset when low. Upon XPD going high, the PLL circuitry begins to lock onto the 33.33 MHz clock input. The PLL circuit may take up to 1 msec to become stable. RESETN asserted low holds the internal DSP logic in reset. Upon RESETN going high, the IC digital logic becomes active.

RESET should be held low during and at least 1 ms after XPD goes high false to hold the internal logic in reset while the PLL becomes stable.

DC Electrical Characteristics and Operating Conditions

Absolute Maximum Ratings

Note: VSS = 0 Volt

PARAMETER	SYMBOL	LIMITS	UNITS	NOTE
Power Supply Voltage	VDD	VSS-0.3 to 4.0	V	
Input Voltage	VI	VSS-0.3 to VDD+0.5	V	Non 5 Volt Tolerant Pins (Table 11)
Input Voltage	VI	VSS-0.3 to 7	V	Only on 5 Volt Tolerant Pins (Table 11)
Output Voltage	VO	VSS-0.3 to VDD+0.5	V	
Output Current per Pin	IOUT	+/- 30	mA	
Storage Temperature	Tstg	-65 to 150	°C	

Table 4: Absolute Maximum Ratings

Recommended Operating Conditions

Note: VSS = 0 Volt

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTE
Power Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Voltage	VI	VSS	-	VDD	V	Non 5 Volt Tolerant Pins (Table 11)
Input Voltage	VI	VSS	-	5.5	V	Only on 5 Volt Tolerant Pins (Table 11)
Ambient Temperature	Ta	-40	-	85	°C	Note 2

Table 5: Recommended Operating Conditions

Notes:
2. The ambient temperature range is recommended for Tj= -40 to 125 °C

DC Characteristics

Common Quiescent and Leakage Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	IDDS	VI=VDD or VSS VDD=MAX IOH=IOL=0 Ta=Tj=85°C	-	-	.35	uA
Input Leakage Current	ILI	VDD=MAX VIH=VDD VIL=VSS	-1	-	1	uA

Table 6: DC Characteristics

Input Characteristics – Non Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VIH1	VDD=MAX	2.0	-	-	V
Low Level Input Voltage	VIL1	VDD=MIN	-	-	0.8	V

Table 7: Non Schmitt Input Characteristics

Input Characteristics – Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VT1+	VDD=MAX	1.1	-	2.4	V
Low Level Input Voltage	VT1-	VDD=MIN	0.6	-	1.8	V
Hysteresis Voltage	VH1	VDD=MIN	0.1	-	-	V

Table 8: Schmitt Input Characteristics

Output Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Voltage	VOH3	VDD=MIN IOH=-12mA	VDD - 0.4	-	-	V
Low Level Output Voltage	VOL3	VDD=MIN IOH = 12mA	-	-	VSS + 0.4	V

Table 9: Output Characteristics

Output Characteristics OSC2CLK

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Voltage	LVOH	VDD=MIN IOH=-530uA	VDD - 0.4	-	-	V
Low Level Output Voltage	LVOL	VDD=MIN IOH = 730uA	-	-	VSS + 0.4	V

Table 10: Output Characteristics OSC2CLK

Pin and I/O Characteristic Table

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
1	BYPASSMODE	40K-240K Pull Down	I	-	Table 8	-
2	FLTCLROUT		O	-	-	Table 9
3	OSC1CLK		I	-	Table 7	
4	LVDD		P	-	-	-
5	OSC2CLK		O	-		Table 10
6	VSS		P	-	-	-
7	PLLTEST	20K-120K Pull Down	I	-	Table 7	-
8	XPD		I	-	Table 7	-
9	VSSHC		P	-	-	-
10	MVDD		P	-	-	-
11	VSSHC		P	-	-	-
12	AVDD		P	-	-	-
13	CHGO		O	-	-	-
14	LPVSS		P	-	-	-
15	DIR	20K – 120K Pull Down	I	YES	Table 8	-
16	RESETN	20K -120K Pull Up	I	-	Table 8	-
17	SPICSN		I	-	Table 8	-
18	REDLED		O	-	-	Table 9
19	GREENLED		O	-	-	Table 9
20	VSS		P	-	-	-
21	PWMWL		O	-	-	Table 9
22	PWMWH		O	-	-	Table 9
23	PWMVL		O	-	-	Table 9
24	LVDD		P	-	-	-
25	PWMVH		O	-	-	Table 9
26	PWMUL		O	-	-	Table 9
27	VSS		P	-	-	-
28	PWMUH		O	-		Table 9
29	BRAKE		O	-	-	Table 9
30	BAUDSEL0	20K – 120K Pull Down	I	YES	Table 8	
31	GATEKILL	20K -120K Pull Up	I	-	Table 8	-
32	IFB1		I	YES	Table 8	-
33	IFB2		I	YES	Table 8	-
34	LVDD		P	-	-	-
35	CLK1XOUT		O	-	-	Table 9
36	VSS		P	-		
37	SPIMOSI		I	YES	Table 8	
38	SPIMISO		O	-	-	Table 9
39	SPICLK		I	YES	Table 8	-
40	TX		O	-	-	Table 9

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
41	RX		I	YES	Table 8	-
42	BAUDSEL1	20K -120K Pull Up	I	YES	Table 8	-
43	LVDD		P	-	-	-
44	ADMUX0		O	-	-	Table 9
45	VSS		P	-	-	-
46	ADMUX1		O	-	-	Table 9
47	ADMUX2		O	-	-	Table 9
48	RESSAMPLE		O	-	-	Table 9
49	ADCONVST		O	-	-	Table 9
50	ADCLK		O	-	-	Table 9
51	ADOUT		I	YES	Table 8	-
52	SYNC		O	-	-	Table 9
53	FAULT		O	-	-	Table 9
54	STARTSTOP	20K -120K Pull Down	I	YES	Table 8	-
55	ESTOP	20K -120K Pull Down	I	YES	Table 8	-
56	FLTCLR	20K -120K Pull Down	I	YES	Table 8	-
57	LVDD		P	-	-	-
58	PWMEN		O	-	-	Table 9
59	DAC3		O	-	-	Table 9
60	VSS		P	-	-	-
61	DAC2		O	-	-	Table 9
62	DAC1		O	-	-	Table 9
63	DAC0		O	-	-	Table 9
64	HP_D0	20K -120K Pull Down	B	-	Table 7	Table 9
65	HP_D1	20K -120K Pull Down	B	-	Table 7	Table 9
66	HP_D2	20K -120K Pull Down	B	-	Table 7	Table 9
67	LVDD		P	-	-	-
68	HP_D3	20K -120K Pull Down	B	-	Table 7	Table 9
69	HP_D4	20K -120K Pull Down	B	-	Table 7	Table 9
70	VSS		P	-	-	-
71	HP_D5	20K -120K Pull Down	B	-	Table 7	Table 9
72	HP_D6	20K -120K Pull Down	B	-	Table 7	Table 9
73	HP_D7	20K -120K Pull Down	B	-	Table 7	Table 9
74	HP_nOE		I	YES	Table 8	-
75	HP_nWE		I	YES	Table 8	
76	HP_A		I	YES	Table 8	-
77	HP_nCS		I	YES	Table 8	-

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
78	VSS		P	-	-	
79	SCL		O	-	-	Table 9
80	SDA	20K -120K Pull Up	B	-	Table 7	Table 9

Table 11: Pin and I/O Characteristics

Power Consumption

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
P_{Total}	PTOTAL	VDD=3.3V	-	1.2	-	WATT

Table 12: IRMCK203 Power Consumption

AC Electrical Characteristics and Operating Conditions

System Level AC Characteristics

Sync Pulse to Sync Pulse Timing

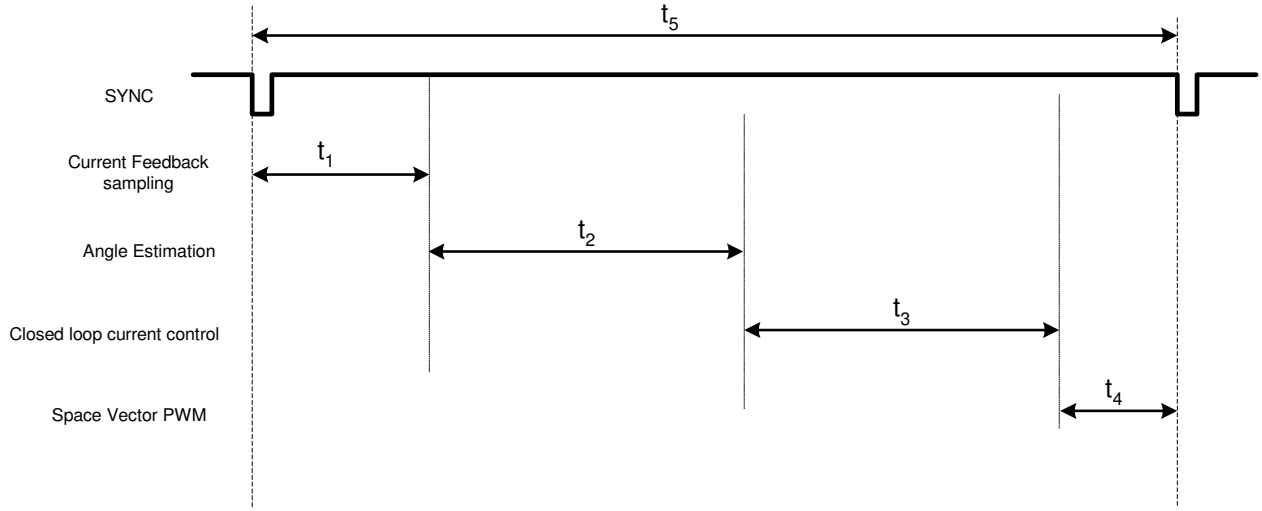

Figure 6: System Level SYNC To SYNC Timing

SYMBOL	DESCRIPTION	TIME (µsec)
t_1	Current Feedback Sample Delay Using IR2175 for current feedback Using Leg Shunts for current feedback (optional)	 4.3 2.0
t_2	Rotor Angle Estimation Time	4.9
t_3	Current and velocity control	3.1
t_4	Space Vector PWM calculation time	2.3
t_5	Total SYNC to SYNC minimum time	14.6 (max)

Table 13: System Level SYNC to SYNC Timing

FAULT and REDLED Response to GATEKILL

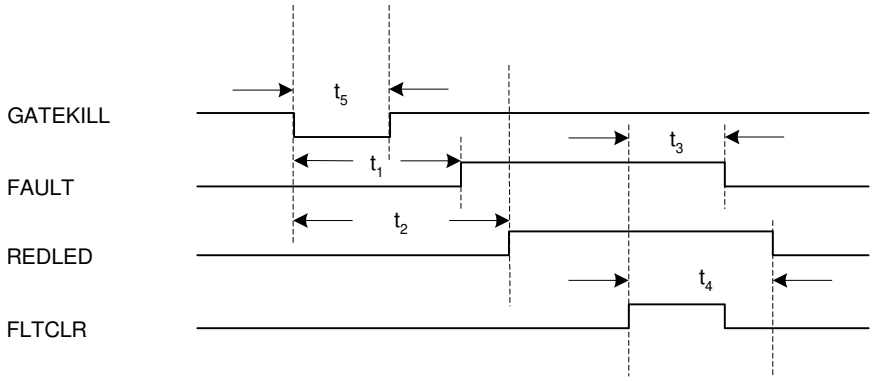

Figure 7: FAULT and REDLED Response to GATEKILL

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t_1	FAULT Response to GATEKILL		640	ns
t_2	REDLED Response to GATEKILL		640	ns
t_3	FAULT Response to FLTCLR		190	ns
t_4	REDLED Response to FLTCLR		190	ns
t_5	GATEKILL Pulse Width	485		ns

Table 14: FAULT and REDLED Response to GATEKILL

Host Interface AC Characteristics

SPI Timing

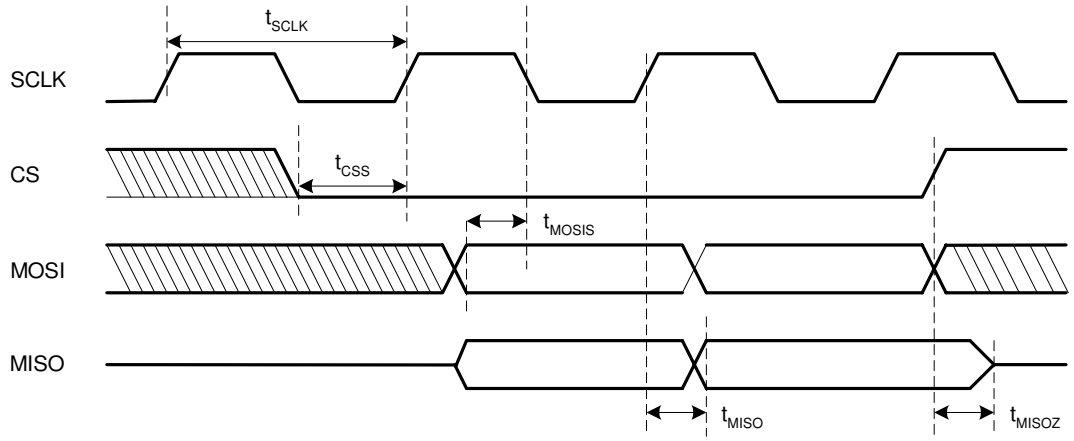

Figure 8: SPI Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
f_{SCLK}	SPI Clock Frequency		8	MHz
t_{SCLK}	SPI Clock Period	125		ns
t_{CSS}	CS to SCLK high Setup	20		ns
t_{MOSIS}	MOSI to SCLK low Setup	20		ns
t_{MISO}	SCLK to MISO Valid	73		ns
t_{MIOZ}	CS to MISO High Impedance	15	35	ns

Table 15: SPI Timing

Host Parallel Timing

Host Parallel Read Cycle

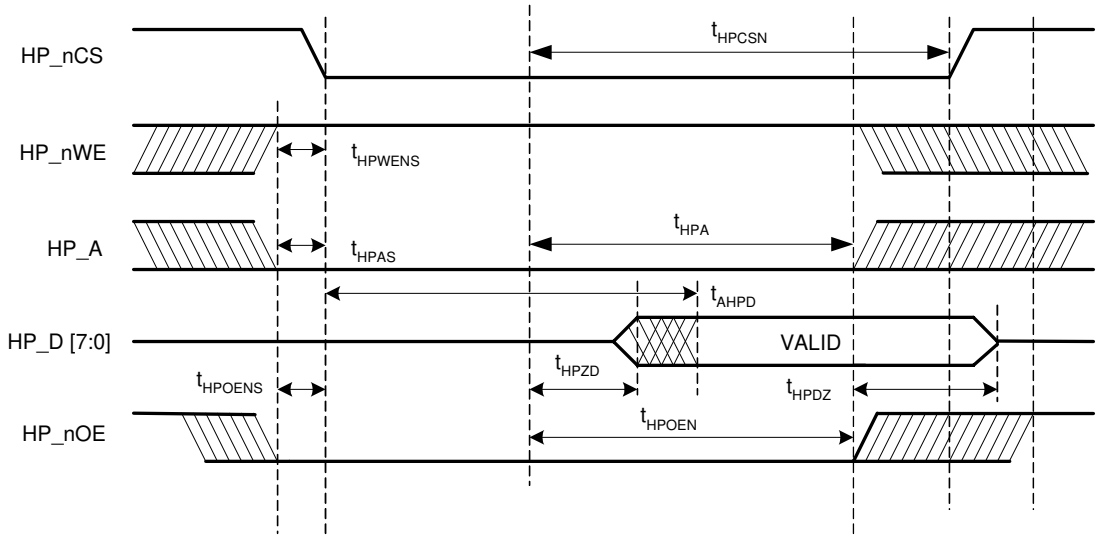

Figure 9: Host Parallel Read Cycle

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HP_nCS Period	70		ns	
t_{HPWENS}	HP_nWE Setup	40		ns	Note 3
t_{HPAS}	HP_A Setup	40		ns	
t_{AHPD}	HP_D [7:0] Access	60	105	ns	
t_{HPZD}	HP_D [7:0] Active	0	9	ns	
t_{HPDZ}	HP_D [7:0] High Impedance	0	6	ns	
t_{HPOENS}	HP_nOE Setup	40		ns	Note 3
t_{HPOEN}	HP_nOE Period	70		ns	

Table 16: Host Parallel Read Cycle Timing

Note:
3. HP_nOE, HP_nWE must be stable before the high to low transition of HP_nCS.