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International IOR Rectifier

# IRMCK312

# Dual Channel Sensorless Motor Control IC for Appliances

## Features

- MCE[TM] (Motion Control Engine) - Hardware based computation engine for high efficiency sinusoidal sensorless control of permanent magnet AC motor
- Integrated Power Factor Correction control
- Supports both interior and surface permanent magnet motors
- Built-in hardware peripheral for single shunt current feedback reconstruction
- No external current or voltage sensing operational amplifier required
- Dual channel three/two-phase Space Vector PWM
- Three-channel analog output (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Two serial communication interface (UART)
- $I^2C$/SPI serial interface
- Watchdog timer with independent analog clock
- Three general purpose timers/counters
- Two special timers: periodic timer, capture timer
- Internal 'One-Time Programmable' (OTP) memory and internal RAM for final production usage
- Pin compatible with IRMCF312 RAM version
- 1.8V/3.3V CMOS

## Product Summary

| | |
|---|---|
| Maximum crystal frequency | 60 MHz |
| Maximum internal clock (SYSCLK) frequency | 128 MHz |
| Maximum 8051 clock frequency | 33 MHz |
| Sensorless control computation time | 11 μsec typ |
| MCE[TM] computation data range | 16 bit signed |
| 8051 OTP Program memory | 56K bytes |
| MCE program and Data RAM | 8K bytes |
| GateKill latency (digital filtered) | 2 μsec |
| PWM carrier frequency counter | 16 bits/ SYSCLK |
| A/D input channels | 11 |
| A/D converter resolution | 12 bits |
| A/D converter conversion speed | 2 μsec |
| 8051 instruction execution speed | 2 SYSCLK |
| Analog output (PWM) resolution | 8 bits |
| UART baud rate (typ) | 57.6K bps |
| Number of I/O (max) | 36 |
| Package (lead-free) | QFP100 |
| Operating temperature | -40°C ~ 85°C |

## Description

IRMCK312 is a high performance OTP based motion control IC designed primarily for appliance applications. IRMCK312 is designed to achieve low cost and high performance control solutions for advanced inverterized appliance motor control. IRMCK312 contains two computation engines. One is Motion Control Engine (MCE[TM]) for sensorless control of permanent magnet motors; the other is an 8-bit high-speed microcontroller (8051). Both computation engines are integrated into one monolithic chip. The MCE[TM] contains a collection of control elements such as Proportional plus Integral, Vector rotator, Angle estimator, Multiply/Divide, Low loss SVPWM, Single Shunt IFB. The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks implemented in hardware. A unique analog/digital circuit and algorithm to fully support single shunt current reconstruction is also provided. The 8051 microcontroller performs 2-cycle instruction execution (16MIPS at 33MHz). The MCE and 8051 microcontroller are connected via dual port RAM to process signal monitoring and command input. An advanced graphic compiler for the MCE[TM] is seamlessly integrated into the MATLAB/Simulink environment, while third party JTAG based emulator tools are supported for 8051 developments. IRMCK312 comes with a small QFP100 pin lead-free package.

# TABLE OF CONTENTS

# TABLE OF FIGURES

# TABLE OF TABLES

# 1 Overview

IRMCK312 is a new International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled appliance dual motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK312 provides a built-in closed loop sensorless control algorithm using the unique Motion Control Engine (MCE™) for permanent magnet motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCK312 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. The sensorless control is the same for both motors with a single shunt current sensing capability. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using IRMCK312.

IRMCK312 is intended for volume production purpose and contains 64K bytes of OTP (One Time Programming) ROM, which can be programmed through a JTAG port. For a development purpose use, IRMCF312 contains a 48k byte of RAM in place of program OTP to facilitate an application development work. Both IRMCF312 and IRMCK312 come in the same 100-pin QFP package with identical pin configuration to facilitate PC board layout and transition to mass production

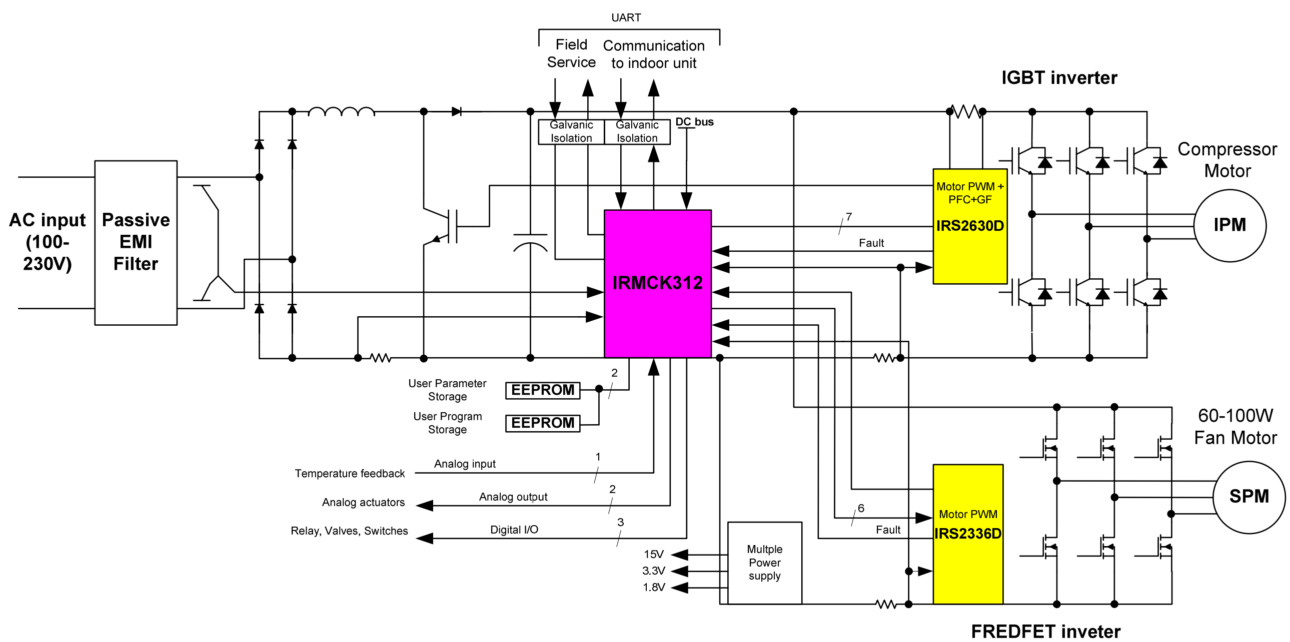


**Figure 1. Typical Application Block Diagram Using IRMCK312**

# 2 IRMCK312 Block Diagram and Main Functions

IRMCK312 block diagram is shown in Figure 2.

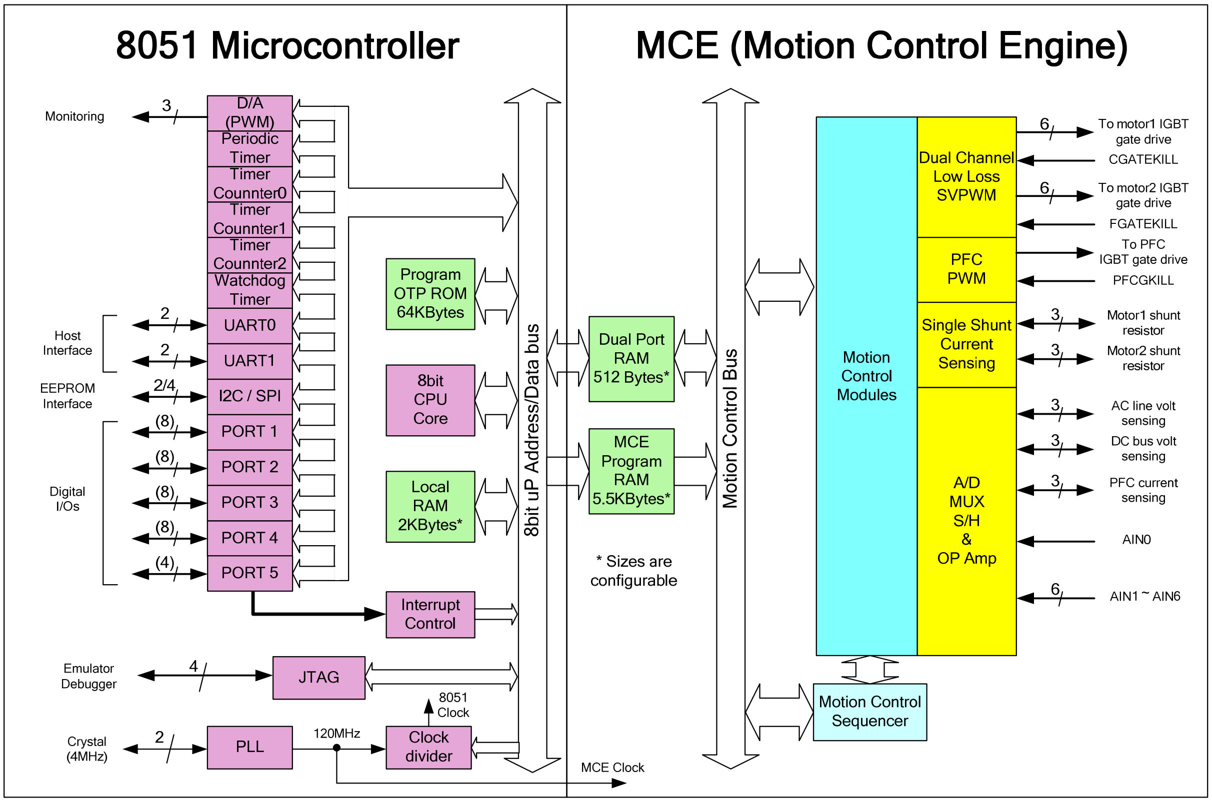


**Figure 2. IRMCK312 Internal Block Diagram**

IRMCK312 contains the following functions for sensorless AC motor control applications:

- Motion Control Engine (MCE™)
    - Proportional plus Integral block
    - Low pass filter
    - Differentiator and lag (high pass filter)
    - Ramp
    - Limit
    - Angle estimate (sensorless control)
    - Inverse Clark transformation
    - Vector rotator
    - Bit latch
    - Peak detect
    - Transition
    - Multiply-divide (signed and unsigned)
    - Divide (signed and unsigned)

- Adder
- Subtractor
- Comparator
- Counter
- Accumulator
- Switch
- Shift
- ATAN (arc tangent)
- Function block (any curve fitting, nonlinear function)
- 16-bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- MCE$^{TM}$ program and data memory (6K byte). [Note 1]
- MCE$^{TM}$ control sequencer

- 8051 microcontroller
  - Three 16-bit timer/counters
  - 16-bit periodic timer
  - 16-bit analog watchdog timer
  - 16-bit capture timer
  - Up to 36 discrete I/Os
  - Eleven-channel 12-bit A/D
    - Five buffered channels (0 – 1.2V input)
    - Six unbuffered channels (0 – 1.2V input)
  - JTAG port (4 pins)
  - Up to three channels of analog output (8-bit PWM)
  - Two UART
  - $I^2C$/SPI port
  - 64K byte [Note 1] program One-Time Programmable memory
  - 2K byte data RAM. [Note 2]

Note 1: Total size of OTP memory is 64K byte, however MCE program occupies maximum 8K byte which will be loaded into internal RAM at a powerup/boot process. Therefore only 56K byte OTP memory area is usable for 8051 microcontroller.
Note 2: Total size of RAM is 8K byte including MCE program, MCE data, and 8051 data. Different sizes can be allocated depending on applications.

# 3 Pinout

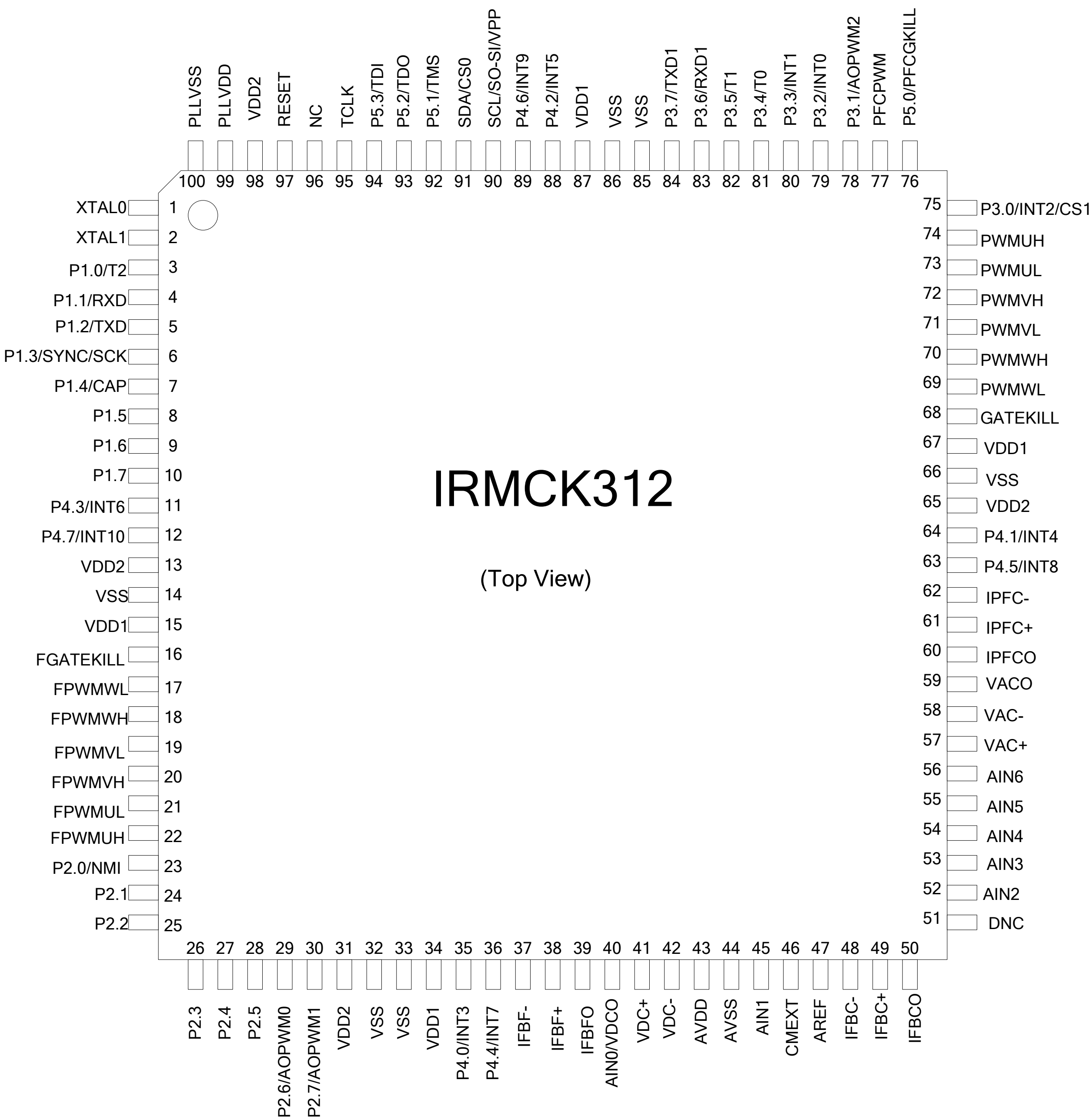


**Figure 3. IRMCK312 Pin Configuration**

**Attention**: Pin 51 must be left floating. Do not connect.

# 4 Input/Output of IRMCK312

All I/O signals of IRMCK312 are shown in Figure 4. All I/O pins are 3.3V logic interface except A/D interface pins.

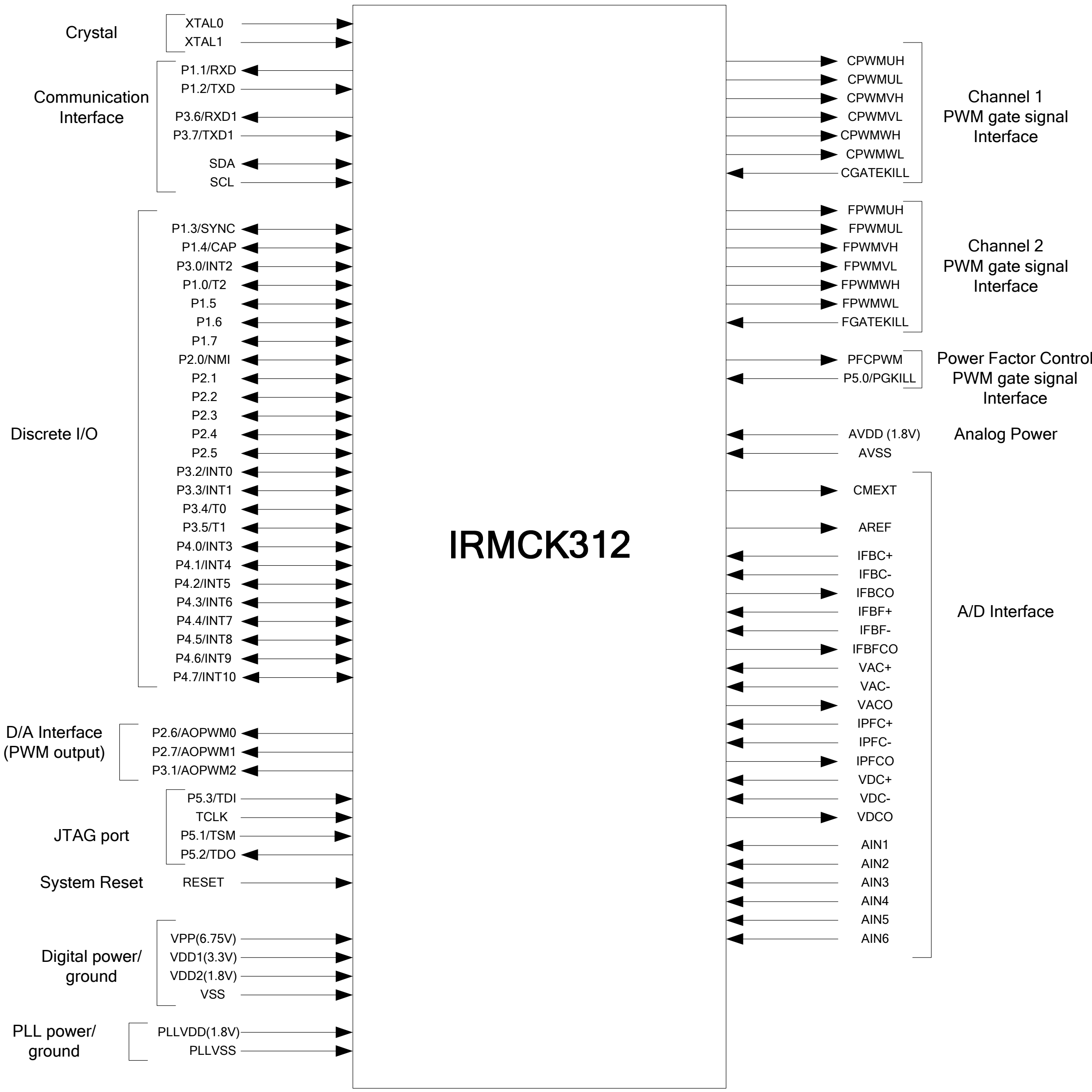


**Figure 4. Input/Output of IRMCK312**

## 4.1 8051 Peripheral Interface Group

**UART Interface**

| | |
|---|---|
| P1.1/RXD | Input, Receive data to IRMCK312, can be configured as P1.1 |
| P1.2/TXD | Output, Transmit data from IRMCK312, can be configured as P1.2 |
| P3.6/RXD1 | Input, 2nd channel Receive data to IRMCK312, can be configured as P3.6 |
| P3.7/TXD1 | Output, 2nd channel Transmit data from IRMCK312, can be configured as P3.7 |

**Discrete I/O Interface**

| | |
|---|---|
| P1.0/T2 | Input/output port 1.0, can be configured as Timer/Counter 2 input |
| P1.3/SYNC/SCK | Input/output port 1.3, can be configured as SYNC output or SPI clock |
| P1.4/CAP | Input/output port 1.4, can be configured as Capture Timer input |
| P1.5 | Input/output port 1.5 |
| P1.6 | Input/output port 1.6 |
| P1.7 | Input/output port 1.7 |
| P2.0/NMI | Input/output port 2.0, can be configured as non-maskable interrupt |
| P2.1 | Input/output port 2.1 |
| P2.2 | Input/output port 2.2 |
| P2.3 | Input/output port 2.3 |
| P2.4 | Input/output port 2.4 |
| P2.5 | Input/output port 2.5 |
| P3.0/INT2/CS1 | Input/output port 3.0, can be configured as external interrupt 2 or SPI chip select 1 |
| P3.2/INT0 | Input/output port 3.2, can be configured as external interrupt 0 |
| P3.3/INT1 | Input/output port 3.3, can be configured as external interrupt 1 |
| P3.4/T0 | Input/output port 3.4, can be configured as Timer/Counter 0 input |
| P3.5/T1 | Input/output port 3.5, can be configured as Timer/Counter 1 input |
| P4.0/INT3 | Input/output port 4.0, can be configured as external interrupt 3 |
| P4.1/INT4 | Input/output port 4.1, can be configured as external interrupt 4 |
| P4.2/INT5 | Input/output port 4.2, can be configured as external interrupt 5 |
| P4.3/INT6 | Input/output port 4.3, can be configured as external interrupt 6 |
| P4.4/INT7 | Input/output port 4.4, can be configured as external interrupt 7 |
| P4.5/INT8 | Input/output port 4.5, can be configured as external interrupt 8 |
| P4.6/INT9 | Input/output port 4.6, can be configured as external interrupt 9 |
| P4.7/INT10 | Input/output port 4.7, can be configured as external interrupt 10 |
| P5.0/PFCGKILL | Input/output port 5.0, can be configured as PFCGKILL |
| P5.1/TMS | Input/output port 5.1, can be configured as JTAG TMS pin |
| P5.2/TDO | Input/output port 5.2, can be configured as JTAG TDO pin |
| P5.3/TDI | Input/output port 5.3, can be configured as JTAG TDI pin |

**Analog Output Interface**

| | |
|---|---|
| P2.6/AOPWM0 | Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency |
| P2.7/AOPWM1 | Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency |
| P3.1/AOPWM2 | Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency |

**Crystal Interface**

| | |
|---|---|
| XTAL0 | Input, connected to crystal |
| XTAL1 | Output, connected to crystal |

**Reset Interface**

| | |
|---|---|
| RESET | Inout, system reset, needs to be pulled up to VDD1 but doesn't require external RC time constant |

**I²C/SPI Interface**

| | |
|---|---|
| SCL/SO-SI/VPP | Output, I²C clock output, SPI SO-SI |
| SDA/CS0 | Input/output, I²C Data line, Chip Select 0 of SPI |
| P3.0/INT2/CS1 | Input/output port 3.0, can be configured as external interrupt 2 or SPI chip select 1 |
| P1.3/SYNC/SCK | Input/output port 1.3, can be configured as SYNC output or SPI clock |

## 4.2 Motion Peripheral Interface Group

**PWM**

| | |
|---|---|
| CPWMUH | Output, motor 1 PWM phase U high side gate signal |
| CPWMUL | Output, motor 1 PWM phase U low side gate signal |
| CPWMVH | Output, motor 1 PWM phase V high side gate signal |
| CPWMVL | Output, motor 1 PWM phase V low side gate signal |
| CPWMWH | Output, motor 1 PWM phase W high side gate signal |
| CPWMWL | Output, motor 1 PWM phase W low side gate signal |
| FPWMUH | Output, motor 2 PWM phase U high side gate signal |
| FPWMUL | Output, motor 2 PWM phase U low side gate signal |
| FPWMVH | Output, motor 2 PWM phase V high side gate signal |
| FPWMVL | Output, motor 2 PWM phase V low side gate signal |
| FPWMWH | Output, motor 2 PWM phase W high side gate signal |
| FPWMWL | Output, motor 2 PWM phase W low side gate signal |
| PFCPWM | Output, PFC PWM |

**Fault**

| | |
|---|---|
| CGATEKILL | Input, upon assertion, this negates all six PWM signals for motor 1, programmable logic sense |
| P5.0/PFCGKILL | Input, upon assertion, this negates PFCPWM signal, programmable logic sense, can be configured as discrete I/O in which case CGATEKILL negates PFCPWM |
| FGATEKILL | Input, upon assertion, this negates all six PWM signals for motor 2, programmable logic sense |

## 4.3 Analog Interface Group

| | |
|---|---|
| AVDD | Analog power (1.8V) |
| AVSS | Analog power return |
| AREF | Buffered 0.6V output |
| CMEXT | Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected. |

| | |
|---|---|
| IFBC+ | Input, Operational amplifier positive input for shunt resistor current sensing of motor 1 |
| IFBC- | Input, Operational amplifier negative input for shunt resistor current sensing of motor 1 |
| IFBCO | Output, Operational amplifier output for shunt resistor current sensing of motor 1 |
| IFBF+ | Input, Operational amplifier positive input for shunt resistor current sensing of motor 2 |
| IFBF- | Input, Operational amplifier negative input for shunt resistor current sensing of motor 2 |
| IFBFO | Output, Operational amplifier output for shunt resistor current sensing of motor 2 |
| IPFC+ | Input, Operational amplifier positive input for PFC current sensing |
| IPFC- | Input, Operational amplifier negative input for PFC current sensing |
| IPFO | Output, Operational amplifier output for PFC current sensing |
| VAC+ | Input, Operational amplifier positive input for PFC AC voltage sensing |
| VAC- | Input, Operational amplifier negative input for PFC AC voltage sensing |
| VACO | Output, Operational amplifier output for PFC AC voltage sensing |
| VDC+ | Input, Operational amplifier positive input for DC bus voltage sensing |
| VDC- | Input, Operational amplifier negative input for DC bus voltage sensing |
| AIN0/VDCO | Input/Output, Analog input channel 0 or Operational amplifier output for DC bus voltage sensing |
| AIN1 | Input, Analog input channel 1 (0-1.2V), needs to be pulled down to AVSS if unused |
| AIN2 | Input, Analog input channel 2 (0-1.2V), needs to be pulled down to AVSS if unused |
| AIN3 | Input, Analog input channel 3 (0-1.2V), needs to be pulled down to AVSS if unused |
| AIN4 | Input, Analog input channel 4 (0-1.2V), needs to be pulled down to AVSS if unused |
| AIN5 | Input, Analog input channel 5 (0-1.2V), needs to be pulled down to AVSS if unused |
| AIN6 | Input, Analog input channel 6 (0-1.2V), needs to be pulled down to AVSS if unused |

## 4.4 Power Interface Group

| | |
|---|---|
| VDD1 | Digital power for I/O (3.3V) |
| VDD2 | Digital power for core logic (1.8V) |
| VSS | Digital common |
| PLLVDD | PLL power (1.8V) |
| PLLVSS | PLL ground return |
| SCL/SO-SI/VPP | OTP programming supply. Can be left open in OTP read mode (normal) |

## 4.5 Test Interface

| | |
|---|---|
| P5.3/TDI | Input, JTAG test data input |
| P5.1/TMS | Input, JTAG test mode select |
| TCK | Input, JTAG test clock |
| P5.2/TDO | Output, JTAG test data output |

# 5 Application Connections

Typical application connection is shown in Figure 5. All components necessary to implement a complete sensorless drive control algorithm are shown connected to IRMCK312.

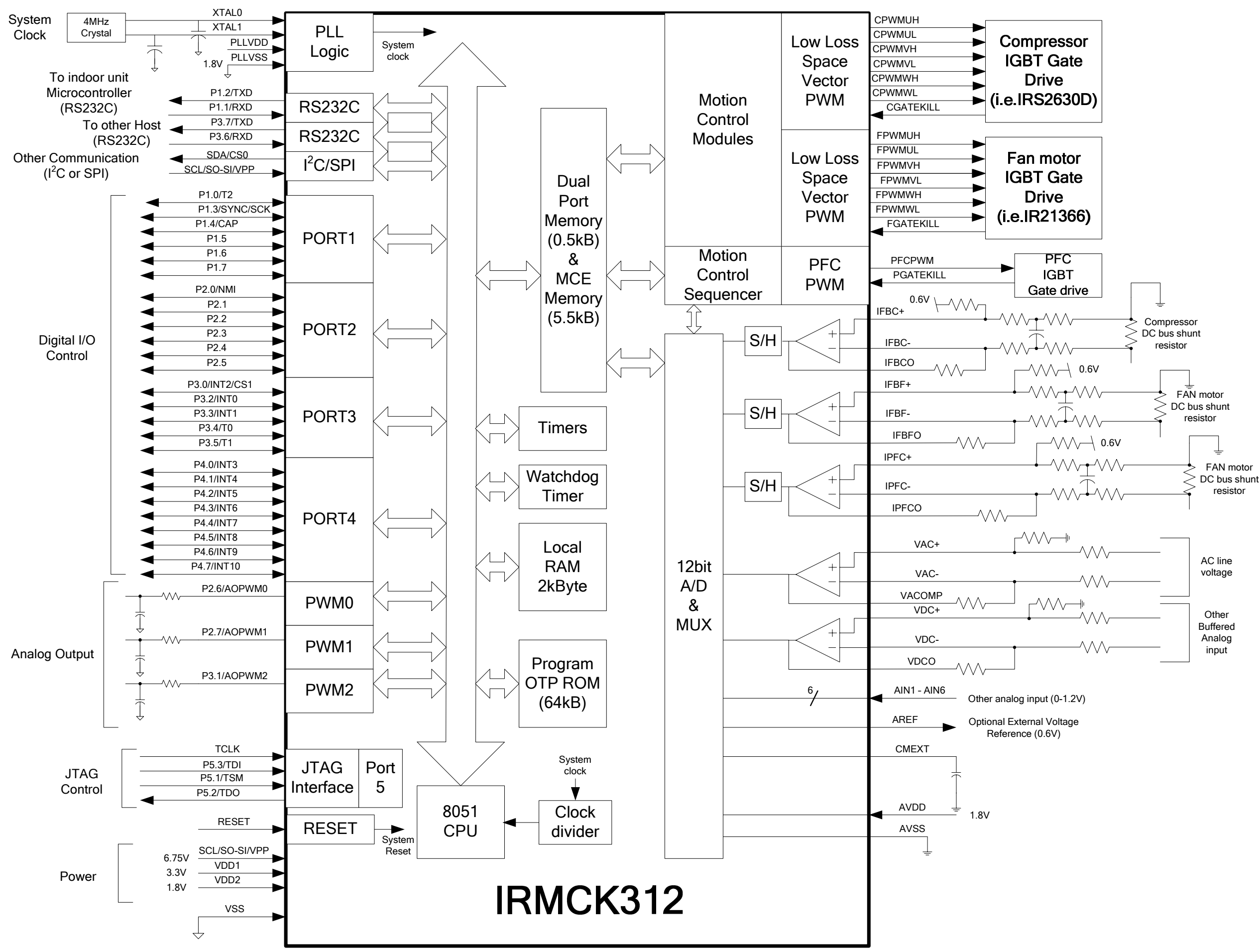


**Figure 5. Application Connection of IRMCK312**

# 6 DC Characteristics

## 6.1 Absolute Maximum Ratings

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $V_{DD1}$ | Supply Voltage | -0.3 V | - | 3.6 V | Respect to VSS |
| $V_{DD2}$ | Supply Voltage | -0.3 V | - | 1.98 V | Respect to VSS |
| $V_{PP}$ | OTP Programming Voltage | -0.3V | - | 7.0V | Respect to VSS |
| $V_{IA}$ | Analog Input Voltage | -0.3 V | - | 1.98 V | Respect to AVSS |
| $V_{ID}$ | Digital Input Voltage | -0.3 V | - | 3.65 V | Respect to VSS |
| $T_A$ | Ambient Temperature | -40 ˚C | - | 85 ˚C | |
| $T_S$ | Storage Temperature | -65 ˚C | - | 150 ˚C | |

**Table 1. Absolute Maximum Ratings**

**Caution:** Stresses beyond those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

## 6.2 System Clock Frequency and Power Consumption

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SYSCLK | System Clock | 32 | - | 128 | **MHz** |
| 8051CLK | 8051 Clock | - | - | 32 | **MHz** |

**Table 2. System Clock Frequency**

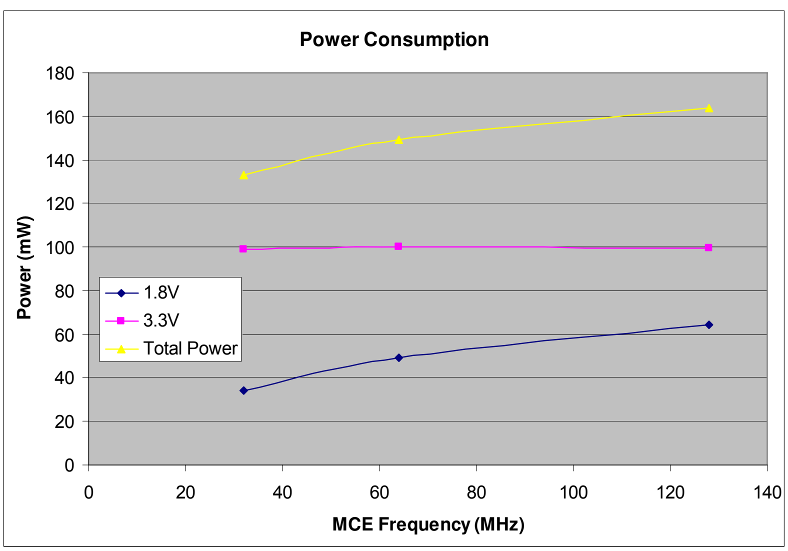


**Figure 6. Clock Frequency vs. Power Consumption**

## 6.3 Digital I/O DC Characteristics

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $V_{DD1}$ | Supply Voltage | 3.0 V | 3.3 V | 3.6 V | Recommended |
| $V_{DD2}$ | Supply Voltage | 1.62 V | 1.8 V | 1.98 V | Recommended |
| $V_{PP}$ | OTP Programming voltage | 6.50V | 6.75V | 7.0V | Recommended |
| $V_{IL}$ | Input Low Voltage | -0.3 V | - | 0.8 V | Recommended |
| $V_{IH}$ | Input High Voltage | 2.0 V | | 3.6 V | Recommended |
| $C_{IN}$ | Input capacitance | - | 3.6 pF | - | (1) |
| $I_L$ | Input leakage current | | ±10 nA | ±1 µA | $V_O$ = 3.3 V or 0 V |
| $I_{OL1}$ (2) | Low level output current | 8.9 mA | 13.2 mA | 15.2 mA | $V_{OL}$ = 0.4 V (1) |
| $I_{OH1}$ (2) | High level output current | 12.4 mA | 24.8 mA | 38 mA | $V_{OH}$ = 2.4 V (1) |
| $I_{OL2}$ (3) | Low level output current | 17.9 mA | 26.3 mA | 33.4 mA | $V_{OL}$ = 0.4 V (1) |
| $I_{OH2}$ (3) | High level output current | 24.6 mA | 49.5 mA | 81 mA | $V_{OH}$ = 2.4 V (1) |

**Table 3. Digital I/O DC Characteristics**

Note:

(1) Data guaranteed by design.
(2) Applied to SCL/SO-SI, SDA/CS0 pins.
(3) Applied to P1.0/T2, P1.1/RXD, P1.2/TXD, P1.3/SYNC/SCK, P1.4/CAP, P1.5, P1.6, P1.7, P2.0/NMI, P2.1, P2.2, P2.3, P2.4, P2.5, P2.6/AOPWM0, P2.7/AOPWM1, P3.0/INT2/CS1, P3.1/AOPWM2, P3.2/INT0, P3.3/INT1, P3.4/T0, P3.5/T1, P3.6/RXD1, P3.7/TXD1, P4.0/INT3, P4.1/INT4, P4.2/INT5, P4.3/INT6, P4.4/INT7, P4.5/INT8, P4.6/INT9, P4.7/INT10, P5.0/PFCGKILL, P5.1/TMS, P5.2/TDO, P5.3/TDI, CGATEKILL, FGATEKILL, CPWMUL, CPWMUH, CPWMVL, CPWMVH, CPWMWL, CPWMWH, FPWMUL, FPWMUH, FPWMVL, FPWMVH, FPWMWL, FPWMWH, and PFCPWM pins.

## 6.4 PLL and Oscillator DC Characteristics

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $V_{PLLVDD}$ | Supply Voltage | 1.62 V | 1.8 V | 1.92 V | Recommended |
| $V_{IL\ OSC}$ | Oscillator Input Low Voltage | $V_{PLLVSS}$ | - | 0.2* $V_{PLLVDD}$ | $V_{PLLVDD}$ = 1.8 V (1) |
| $V_{IH\ OSC}$ | Oscillator Input High Voltage | 0.8* $V_{PLLVDD}$ | | $V_{PLLVDD}$ | $V_{PLLVDD}$ = 1.8 V (1) |

**Table 4. PLL DC Characteristics**

Note:
(1) Data guaranteed by design.

## 6.5 Analog I/O DC Characteristics

- OP amps for current sensing (IFBC+, IFBC-, IFBCO, IFBF+, IFBF-, IFBFO, IPFC+, IPFC-, IPFCO)

$C_{AREF}$ = 1nF, $C_{MEXT}$= 100nF. Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $V_{AVDD}$ | Supply Voltage | 1.71 V | 1.8 V | 1.89 V | Recommended |
| $V_{OFFSET}$ | Input Offset Voltage | - | - | 26 mV | $V_{AVDD}$ = 1.8 V |
| $V_I$ | Input Voltage Range | 0 V | | 1.2 V | Recommended |
| $V_{OUTSW}$ | OP amp output operating range | 50 mV (1) | - | 1.2 V | $V_{AVDD}$ = 1.8 V |
| $C_{IN}$ | Input capacitance | - | 3.6 pF | - | (1) |
| $R_{FDBK}$ | OP amp feedback resistor | 5 kΩ | - | 20 kΩ | Requested between op amp output and negative input |
| $OP_{GAINCL}$ | Operating Close loop Gain | 80 db | - | - | (1) |
| CMRR | Common Mode Rejection Ratio | - | 80 db | - | (1) |
| $I_{SRC}$ | Op amp output source current | - | 1 mA | - | $V_{OUT}$ = 0.6 V (1) |
| $I_{SNK}$ | Op amp output sink current | - | 100 µA | - | $V_{OUT}$ = 0.6 V (1) |

**Table 5. Analog I/O DC Characteristics**

Note: (1) Data guaranteed by design.

## 6.6 Under Voltage Lockout DC Characteristics

- Based on AVDD (1.8V)

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $UV_{CC+}$ | UVcc positive going Threshold[1)] | 1.53 V | 1.66 V | 1.71 V | $V_{DD1}$ = 3.3 V |
| $UV_{CC-}$ | UVcc negative going Threshold | 1.52 V | 1.62 V | 1.71 V | $V_{DD1}$ = 3.3 V |
| $UV_{CC}H$ | UVcc Hysteresys | - | 40 mV | - | |

**Table 6. UVcc DC Characteristics**

Note:

1) Data guaranteed by design.

## 6.7 AREF Characteristics

$C_{AREF}$ = 1nF, $C_{MEXT}$= 100nF. Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $V_{AREF}$ | AREF Output Voltage | 495 mV | 600 mV | 700 mV | $V_{AVDD}$ = 1.8 V |
| $\Delta V_o$ | Load regulation ($V_{DC}$-0.6) | - | 1 mV | - | [(1)] |
| PSRR | Power Supply Rejection Ratio | - | 75 db | - | [(1)] |

**Table 7. AREF DC Characteristics**

Note:

(1) Data guaranteed by design.

# 7 AC Characteristics

## 7.1 PLL AC Characteristics

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $F_{CLKIN}$ | Crystal input frequency | 3.2 MHz | 4 MHz | 60 MHz | (1) (see figure below) |
| $F_{PLL}$ | Internal clock frequency | 32 MHz | 50 MHz | 128 MHz | (1) |
| $F_{LWPW}$ | Sleep mode output frequency | $F_{CLKIN}$ ÷ 256 | - | - | (1) |
| $J_S$ | Short time jitter | - | 200 psec | - | (1) |
| D | Duty cycle | - | 50 % | - | (1) |
| $T_{LOCK}$ | PLL lock time | - | - | 500 µsec | (1) |

**Table 8. PLL AC Characteristics**

Note:
(1) Data guaranteed by design.

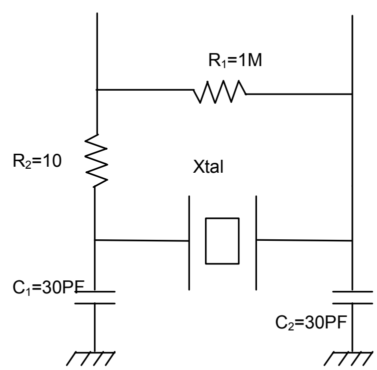


**Figure 7 Crystal oscillator circuit**

## 7.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $T_{CONV}$ | Conversion time | - | - | 2.05 µsec | (1) |
| $T_{HOLD}$ | Sample/Hold maximum hold time | - | - | 10 µsec | Voltage droop ≤ 15 LSB (see figure below) |

**Table 9. A/D Converter AC Characteristics**

Note:
(1) Data guaranteed by design.

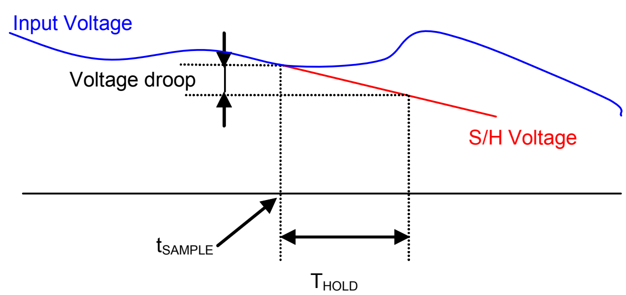


**Figure 8 Voltage droop of sample and hold**

## 7.3 Op Amp AC Characteristics

- OP amps for current sensing (IFBC+, IFBC-, IFBCO, IFBF+, IFBF-, IFBFO, IPFC+, IPFC-, IPFCO)

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Condition |
|---|---|---|---|---|---|
| $OP_{SR}$ | OP amp slew rate | - | 10 V/µsec | - | $V_{AVDD}$ = 1.8 V, CL = 33 pF (1) |
| $OP_{IMP}$ | OP input impedance | - | $10^8$ Ω | - | (1) |
| $T_{SET}$ | Settling time | - | 400 ns | - | $V_{AVDD}$ = 1.8 V, CL = 33 pF (1) |

**Table 10. Current Sensing OP Amp AC Characteristics**

Note:
(1) Data guaranteed by design.

## 7.4 SYNC to SVPWM and A/D Conversion AC Timing

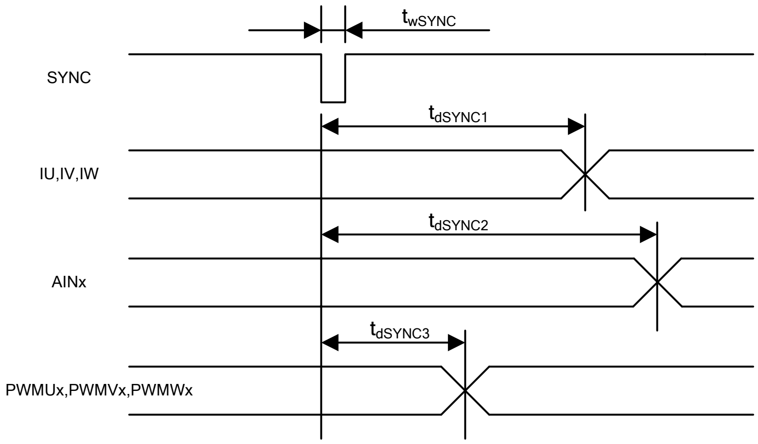


**Figure 9 SYNC to SVPWM and A/D conversion AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{wSYNC}$ | SYNC pulse width | - | 32 | - | SYSCLK |
| $t_{dSYNC1}$ | SYNC to current feedback conversion time | - | - | 100 | SYSCLK |
| $t_{dSYNC2}$ | SYNC to AIN0-6 analog input conversion time | - | - | 200 | SYSCLK (1) |
| $t_{dSYNC3}$ | SYNC to PWM output delay time | - | - | 2 | SYSCLK |

**Table 11. SYNC AC Characteristics**

Note:

(1) AIN1 through AIN6 channels are converted once every 6 SYNC events

## 7.5 GATEKILL to SVPWM AC Timing

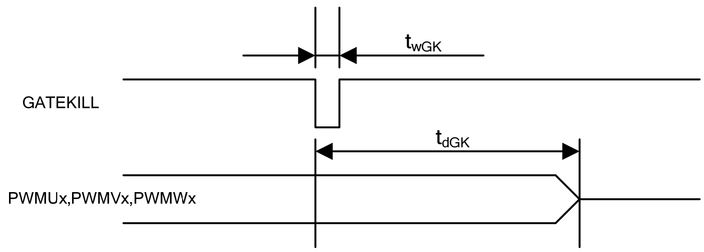


**Figure 10 GATEKILL to SVPWM AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{wGK}$ | GATEKILL pulse width | 32 | - | - | SYSCLK |
| $t_{dGK}$ | GATEKILL to PWM output delay | - | - | 100 | SYSCLK |

**Table 12. GATEKILL to SVPWM AC Timing**

## 7.6 Interrupt AC Timing

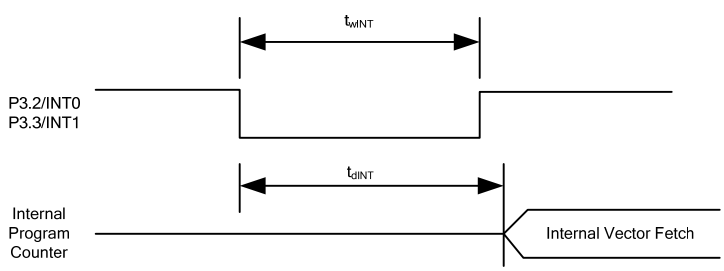


**Figure 11 Interrupt AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{wINT}$ | INT0, INT1 Interrupt Assertion Time | 4 | - | - | SYSCLK |
| $t_{dINT}$ | INT0, INT1 latency | - | - | 4 | SYSCLK |

**Table 13. Interrupt AC Timing**

## 7.7 I²C AC Timing

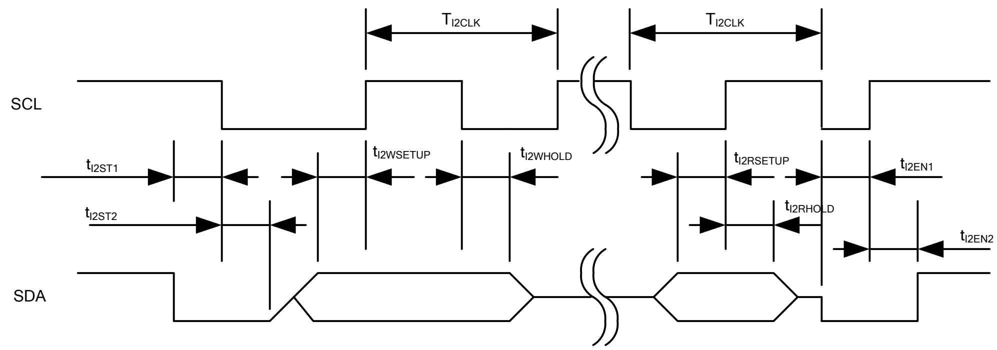


**Figure 12 I²C AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{I2CLK}$ | I²C clock period | 10 | - | 8192 | SYSCLK |
| $t_{I2ST1}$ | I²C SDA start time | 0.25 | - | - | $T_{I2CLK}$ |
| $t_{I2ST2}$ | I²C SCL start time | 0.25 | - | - | $T_{I2CLK}$ |
| $t_{I2WSETUP}$ | I²C write setup time | 0.25 | - | - | $T_{I2CLK}$ |
| $t_{I2WHOLD}$ | I²C write hold time | 0.25 | - | - | $T_{I2CLK}$ |
| $t_{I2RSETUP}$ | I²C read setup time | I²C filter time(1) | - | - | SYSCLK |
| $t_{I2RHOLD}$ | I²C read hold time | 1 | - | - | SYSCLK |

**Table 14. I²C AC Timing**

Note:

(1) I²C read setup time is determined by the programmable filter time applied to I²C communication.

# 7.8 SPI AC Timing

## *7.8.1 SPI Write AC timing*

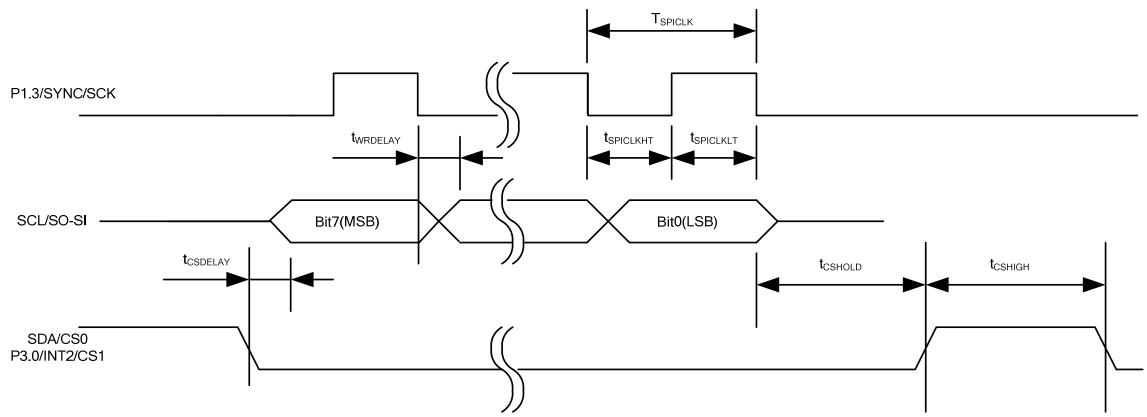


**Figure 13 SPI AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SPICLK}$ | SPI clock period | 4 | - | - | SYSCLK |
| $t_{SPICLKHT}$ | SPI clock high time | - | 1/2 | - | $T_{SPICLK}$ |
| $t_{SPICLKLT}$ | SPI clock low time | - | 1/2 | - | $T_{SPICLK}$ |
| $t_{CSDELAY}$ | CS to data delay time | - | - | 10 | nsec |
| $t_{WRDELAY}$ | CLK falling edge to data delay time | - | - | 10 | nsec |
| $t_{CSHIGH}$ | CS high time between two consecutive byte transfer | 1 | - | - | $T_{SPICLK}$ |
| $t_{CSHOLD}$ | CS hold time | - | 1 | - | $T_{SPICLK}$ |

**Table 15. SPI Write AC Timing**

### 7.8.2 SPI Read AC Timing

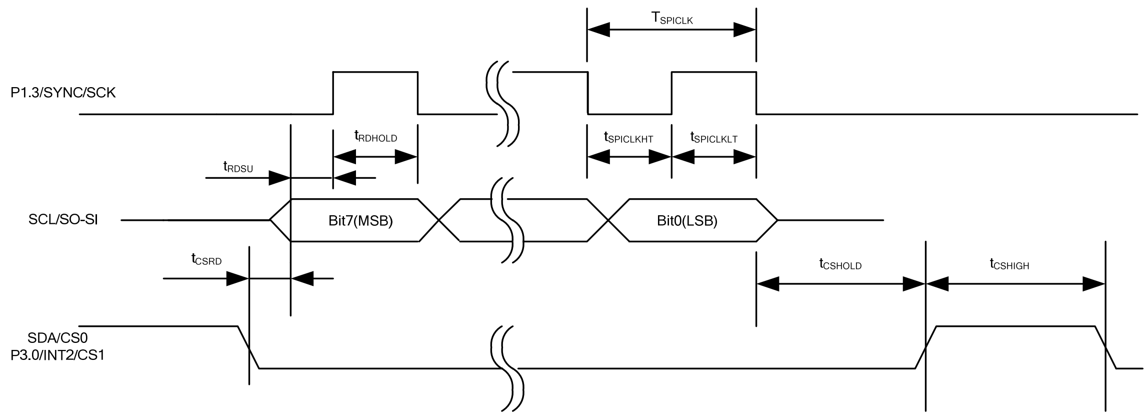


**Figure 14 SPI Read AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SPICLK}$ | SPI clock period | 4 | - | - | SYSCLK |
| $t_{SPICLKHT}$ | SPI clock high time | - | 1/2 | - | $T_{SPICLK}$ |
| $t_{SPICLKLT}$ | SPI clock low time | - | 1/2 | - | $T_{SPICLK}$ |
| $t_{CSRD}$ | CS to data delay time | - | - | 10 | nsec |
| $t_{RDSU}$ | SPI read data setup time | 10 | - | - | nsec |
| $t_{RDHOLD}$ | SPI read data hold time | 10 | - | - | nsec |
| $t_{CSHIGH}$ | CS high time between two consecutive byte transfer | 1 | - | - | $T_{SPICLK}$ |
| $t_{CSHOLD}$ | CS hold time | - | 1 | - | $T_{SPICLK}$ |

**Table 16. SPI Read AC Timing**

## 7.9 UART AC Timing

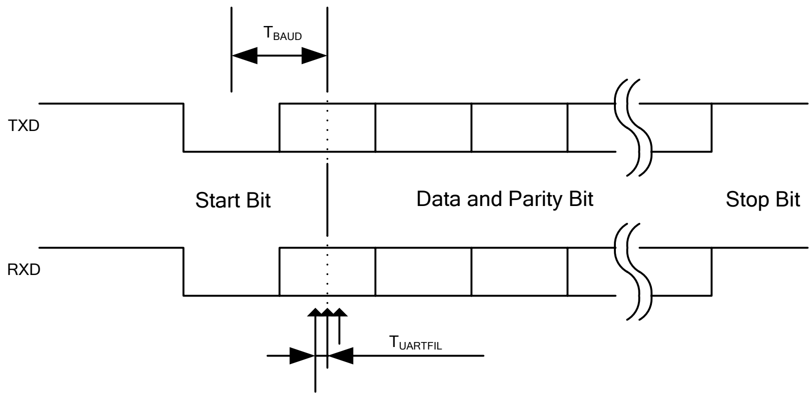


**Figure 15 UART AC Timing**

Unless specified, Ta = 25˚C.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{BAUD}$ | Baud Rate Period | - | 57600 | - | bit/sec |
| $T_{UARTFIL}$ | UART sampling filter period (1) | - | 1/16 | - | $T_{BAUD}$ |

**Table 17. UART AC Timing**

Note:

(1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 $T_{BAUD}$. If three sampled values do not agree, then UART noise error is generated.