Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

IRPLLED1

IRPLLED1 (Rev D Version)
350mA to 1.5A High Voltage LED Driver using
IRS2540,1 or IRS25401,11

Table of Contents

EVALUATION BOARD - IRPLLED1

1. Introduction

Development of LED technology over the last few years has produced high power devices with luminous efficacies surpassing Fluorescent and HID light sources. These solid state light sources also posses the added advantages of longer operating life span, up to 50000 hours as well greater robustness that other less efficient light sources.
For these reasons high power LEDs have now become a viable alternative for many general lighting applications.
High power LEDs are driven with constant regulated DC current, requiring a "ballast" or "converter" to provide the required current from an AC or DC power source. The IRS2540/1/01/11 series Buck LED driver provides an accurately controlled current and protects the LEDs against damage from overload, while providing the ability to dim the light level. The IRS2540/1/01/11 will be replaced by the fully compatible revised IRS25401/11.

The IRPLLED1evaluation board is a high voltage LED driver designed to operate from a DC input voltage of 50V to 170V and produce an output voltage of 16V-24V to supply a programmable load current of 350mA, 700mA, 1A, or 1.5A. It uses the IRS2540/1/01/11 or revised version IRS25401/11, a high voltage, high frequency Buck control IC for constant LED current regulation. The IRS2540/1/01/11 controls the average load current by a continuous mode time-delayed hysteretic method using an accurate on chip band gap voltage reference. The 8-pin, 200V/600V rated IRS2540/1/01/11 inherently provides short-circuit protection with open-circuit protection incorporated by a simple external circuit and has dimming capability.
The evaluation board documentation will briefly describe the functionality of IRS2540/1/01/11, discuss the selection of the output stage, switching components and surrounding circuitry. This board was tested with a single HBLED panel for the 350mA and 700mA settings, using two similar flood boards in parallel to provide test loads for the 1A and 1.5A settings.

Important Safety Information
The IRPLLED1 does not provide galvanic isolation of the LED drive output from the line input. Therefore if the system is supplied directly from a non-isolated input, an electrical shock hazard exists at the LED outputs and these should not be touched during operation. Although the output voltage is low this electrical shock hazard still exists.
It is recommended that for laboratory evaluation that the IRPLLED1 board be used with an isolated DC input supply. The IRS2540/1/01/11 series Buck topology is suitable only for final applications where isolation is either not necessary or provided elsewhere in the system.

2. Constant current control

The IRS2540/1/01/11 is a time-delayed hysteretic Buck controller. During normal operating conditions the output current is regulated via the IFB pin voltage to a nominal value of 500mV. This feedback signal is compared to an internal high precision band gap voltage reference. An on-board dV/dt filter has also been used to prevent erroneous transitioning. This is necessary since the IFB pin is sensitive to noise.

The Buck topology may use a fast recovery diode for the lower switch or a synchronous MOSFET shown as M2 in Fig 1. On power up as the VCC supply to the IR2540/1/01/11 reaches V_{CCUV+} the LO output is held high and the HO output low for a predetermined period of time. This initiates charging of the bootstrap capacitor establishing the VBS floating supply for the high side output. The chip then begins toggling HO and LO outputs as needed to regulate the load current monitored and fed back through the current sense resistor RCS. The dead times of approximately 140ns between the LO and HO gate drive signals prevents shoot through and reduce switching losses, particularly at higher frequencies.

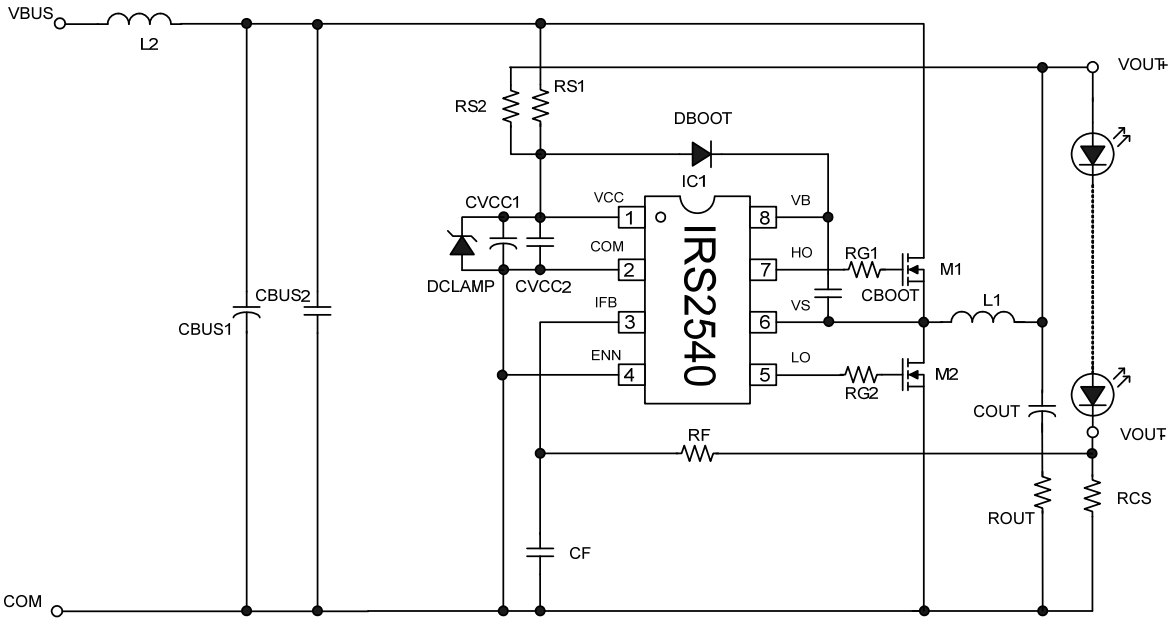
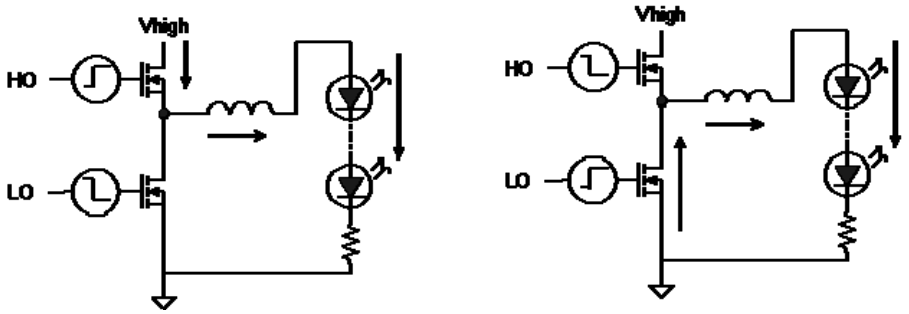


Fig. 1 IRS2540/1/01/11 Constant Current LED Driver Typical Schematic
(see Fig. 16 for evaluation board full schematic)

Note: Cout and Rout are optional and may be required in some applications

Under normal operating conditions, if VIFB is below VIFBTH, HO will be high and the load receives current from VBUS through the Buck inductor L1. This simultaneously stores energy in the output stage comprised of L1 and COUT as VIFB begins to increase. When VIFB crosses VIFBTH, HO transitions low after the delay t_HO_off. Once HO is low, LO will transition high after the deadtime. The inductor and output capacitor release the stored energy into the load and VIFB starts decreasing. When VIFB crosses VIFBTH again, LO switches low after the delay t_LO_off and HO switches high after the delay t_HO_on. The cycle then repeats continuously at a frequency depending on the load current and the values of the output inductor and capacitor.



(A) **(B)**

Fig. 2 (A) Storing Energy in Inductor
(B) Releasing Stored Inductor Energy

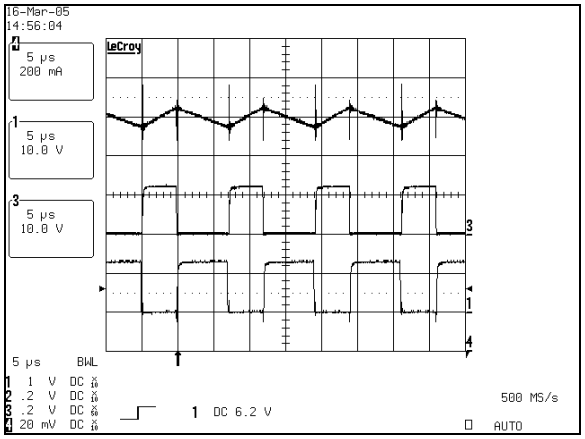


Fig. 3 IRS2540/1/01/11 Control Signals, Iavg=1.2A

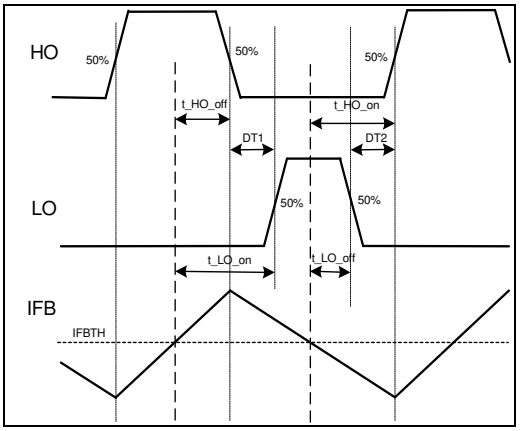


Fig. 4 IRS2540/1/01/11 Time Delayed Hysteresis

The switching continues to regulate the current at an average value determined as follows: when the output combination of L1 and COUT is large enough to maintain a low ripple on IFB (less than 100mV), Iout(avg) can be calculated:

$$Iout(avg) = {VIFBTH}/{RCS}$$

Having load current programmable from 350mA to 1.5A, series and parallel combinations of resistors must be used to correctly set the current as well as distribute power accordingly. Equivalent resistances for each current setting are calculated as follows:

$$R_{350mA} = \frac{0.5V}{350mA} = 1.43\Omega$$

$$R_{700mA} = \frac{0.5V}{700mA} = 0.71\Omega$$

$$R_{1A} = \frac{0.5V}{1A} = 0.5\Omega$$

$$R_{1.5A} = \frac{0.5V}{1.5A} = 0.33\Omega$$

Since some of these equivalent values of resistance are not available, series and parallel combinations are used and are specified as follows (all combinations use standard value resistors: 1.43Ω, 0.56Ω, and 0.47Ω):

$$R_{350mA} = 1.43\Omega$$

$$R_{700mA} = 0.71\Omega \approx (1.43\Omega \,||\, 1.43\Omega) = 0.715\Omega$$

$$R_{1A} = 0.5\Omega \approx (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) = 0.515\Omega$$

$$R_{1.5A} = 0.33\Omega \approx (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) = 0.343\Omega$$

Although some of the series and parallel combinations do not yield the exact resistance needed for tolerance purposes, they are accurate enough. For this evaluation board an extremely tight current regulation is achieved with a worst case result of ±1.2% for the 350mA setting over the bus voltage range from 50V to 170V. Likewise a precise regulation of ±0.25% can be maintained for a range of load voltage from 16V to 24V at the 350mA current setting. The jumper positions on the evaluation boards (JSET) for setting the different load currents are shown below:

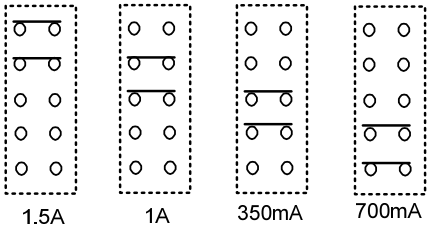


Fig. 4a: JSET LED Current Programming Settings

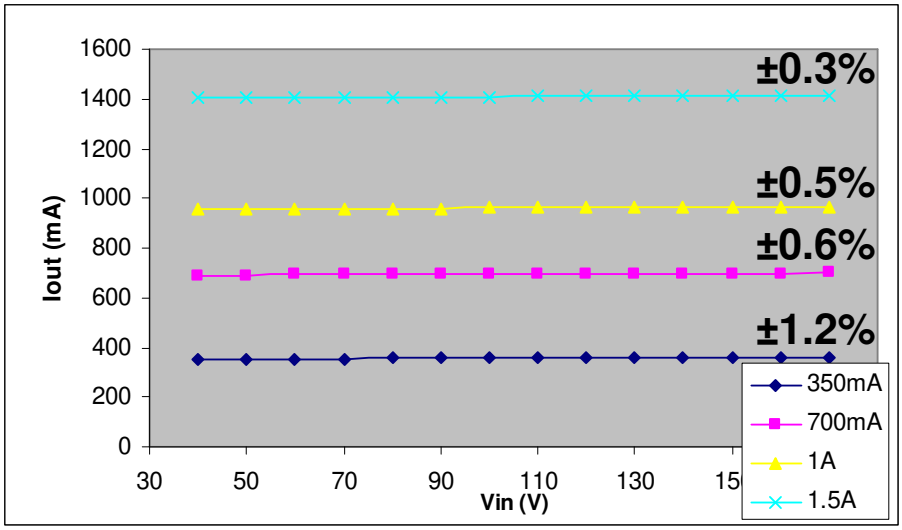


Fig. 5 Vout = 16V, L1 = 470uH, COUT = 33uF

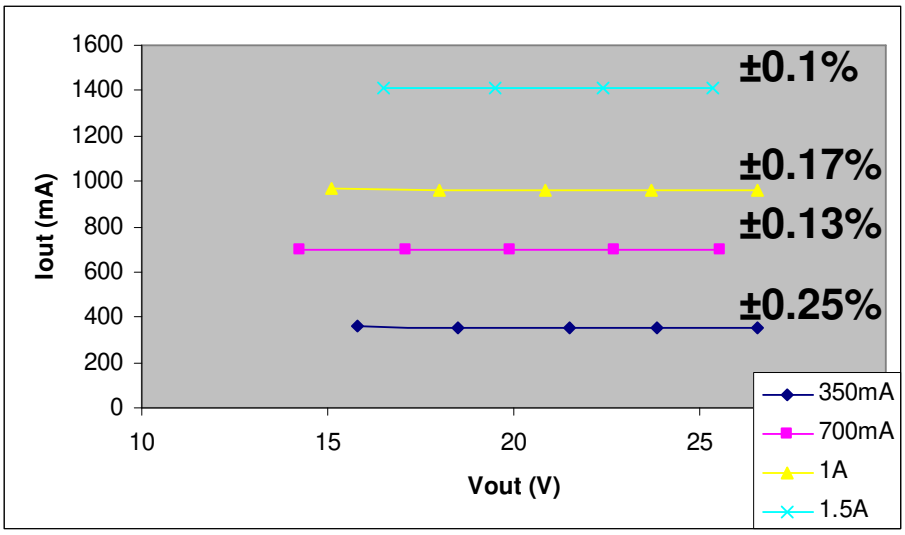


Fig. 6 Vbus = 100V, L1 = 470uH, COUT = 33uF

3. Frequency selection

The frequency in the IRS2540/1/01/11 application is free running and maintains current regulation by quickly adapting to changes in input and output voltages. There is no need for additional external components to set the frequency as seen in other controllers. The frequency is determined by L1 and COUT, as well as the input/output voltages and load current. The selection of the frequency is a trade-off between system efficiency, current control regulation, size, and cost.

The higher the frequency, the smaller and lower the cost of L1 and COUT, the higher the ripple, the higher the FET switching losses, which becomes the driving factor as VBUS increases to higher voltages, the higher the component stresses and the harder it is to control the output current.

4. Output L1 and COUT selection

In order to maintain good output current regulation with minimum ripple, the value of L1 needs to be adequately sized. COUT is optional and can also be used for energy storage, which allows the converter to run at a lower frequency. Excess ripple at the output results in high peak currents that are undesirable for driving high power LEDs and also negates the ability of the system to accurately regulate the average current.

First, the effect of the inductor in a configuration with no output capacitor will be considered to clearly demonstrate the impact of the inductor. In this case, the load current is identical to the inductor current. Fig. 7 shows how the inductor value influences the frequency over a range of input voltages. As can be seen, the input voltage also has a great effect on the frequency. The inductor value reduces the frequency for lower input voltages.

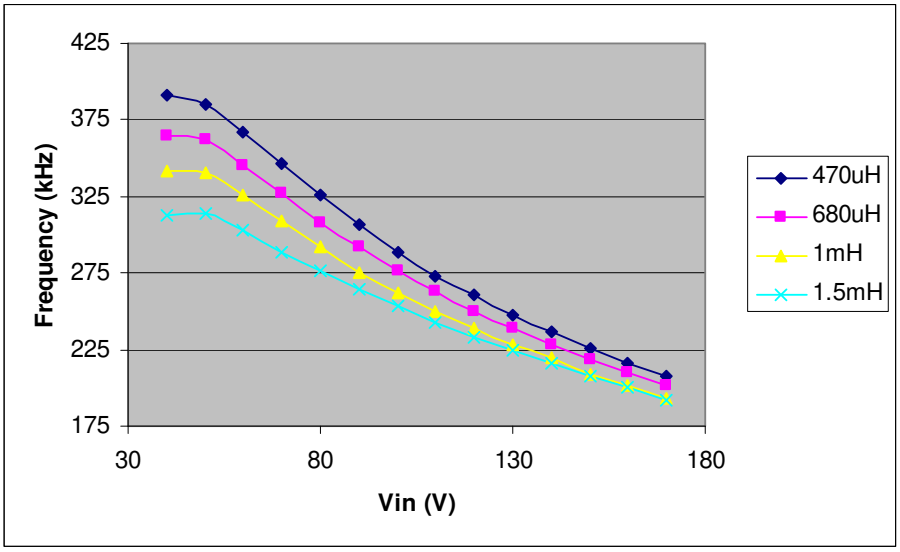


Fig. 7 Iout = 350mA, Vout = 16.8V, COUT = 0uF

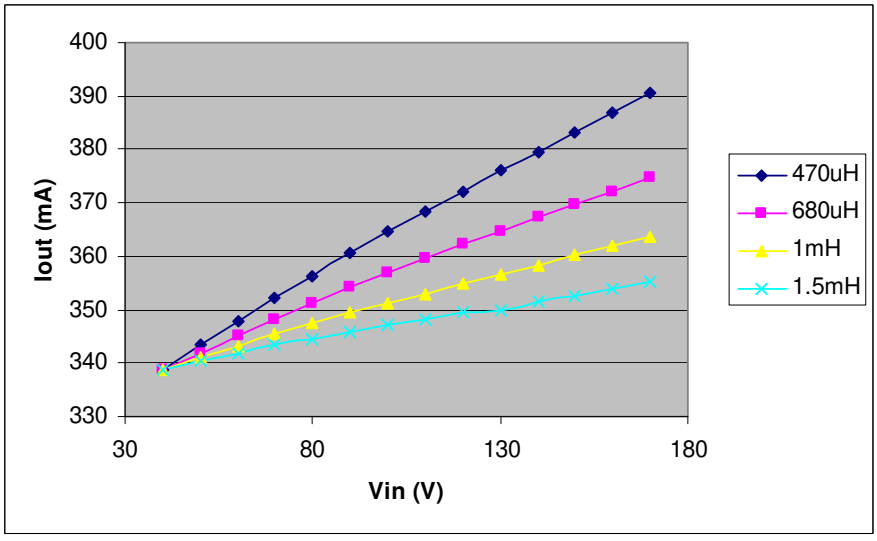


Fig. 8 Iout = 350mA, Vout = 16.8V, COUT = 0uF

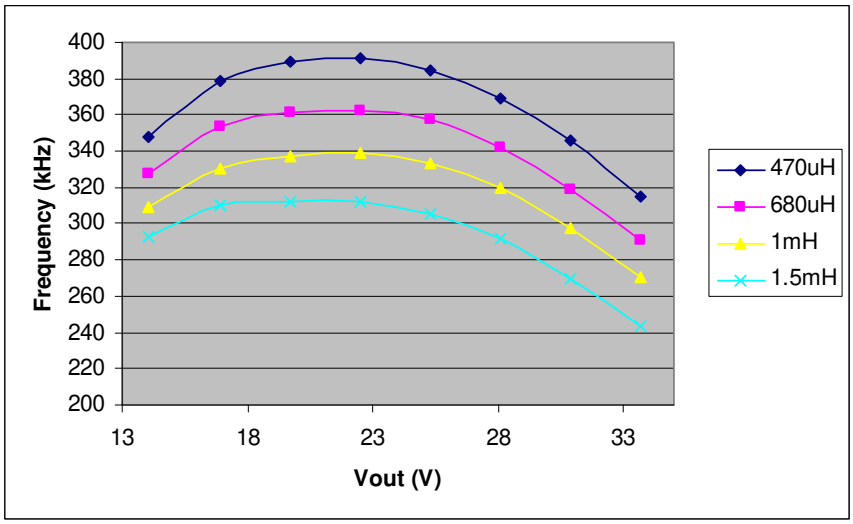


Fig. 9 Iout = 350mA, Vin = 50V, COUT = 0uF

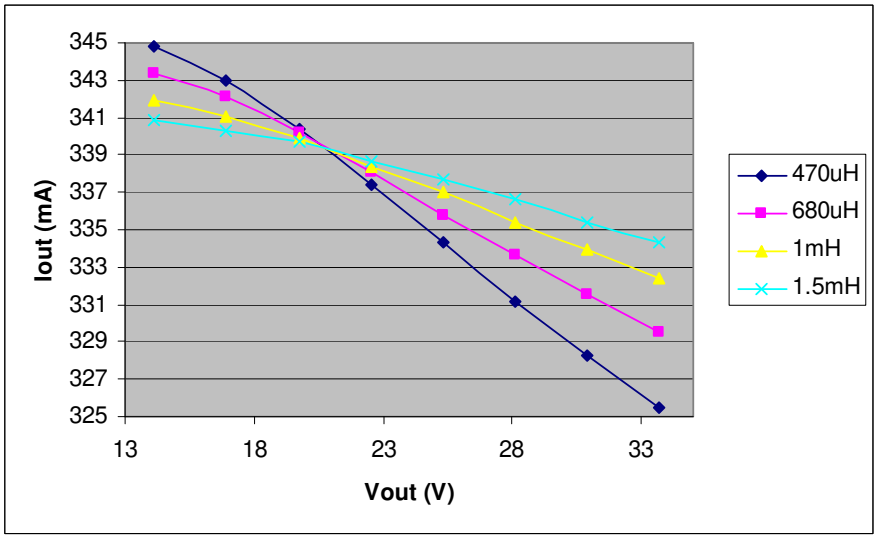


Fig. 10 Iout = 350mA, Vin = 50V, COUT = 0uF

The output capacitor can be used simultaneously to reduce the frequency and improve current control accuracy. Fig. 11 shows how the capacitance reduces the frequency over a range of input voltage. A capacitance of 4.7uF has a large effect on reducing the frequency. Fig. 12 shows how the current regulation is also improved with the output capacitance. There is a point at which continuing to add capacitance no longer has a significant effect on the operating frequency or current regulation, as can be seen in Fig. 12 and Fig. 13.

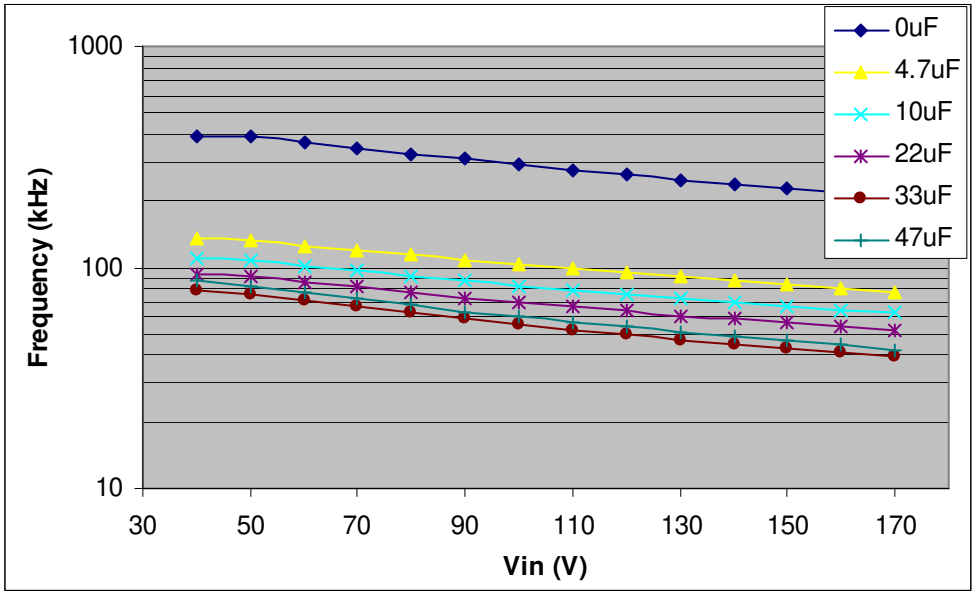


Fig. 11 Iout = 350mA, Vout = 16.8V, L = 470uH

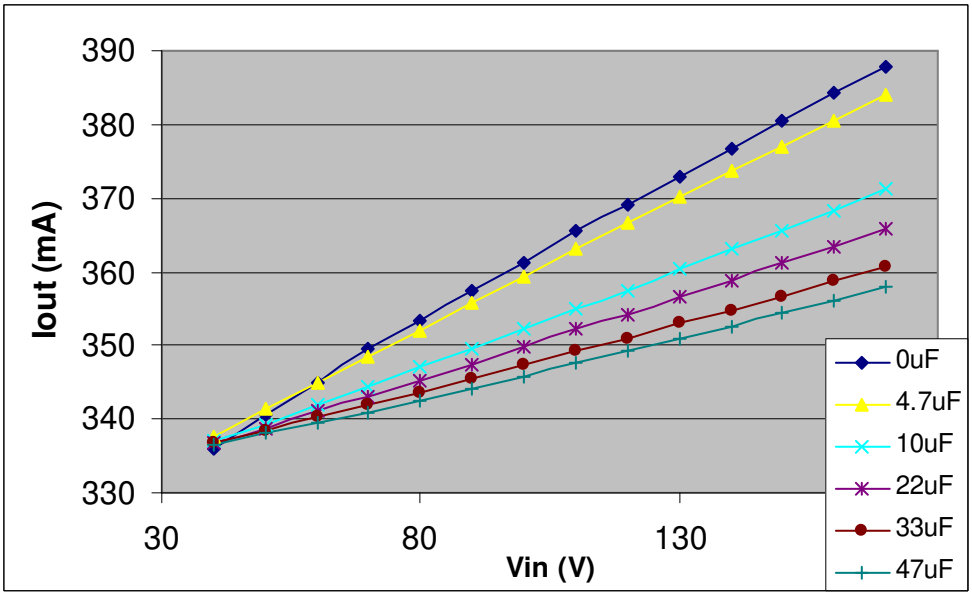


Fig. 12 Iout = 350mA, Vout = 16.8V, L = 470uH

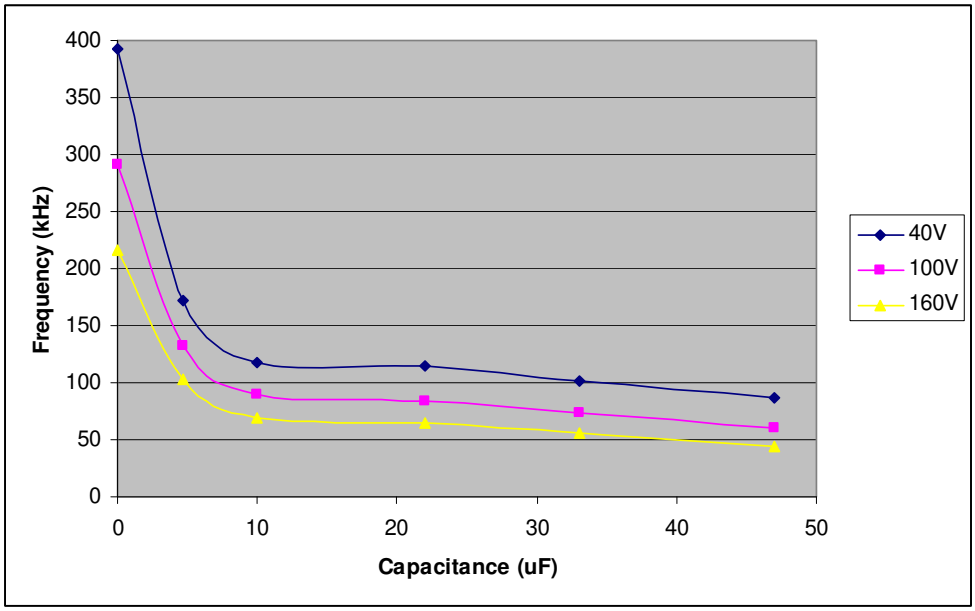


Fig. 13 Iout = 350mA, Vout = 16.8V, L = 470uH

The addition of the COUT is essentially increasing the amount of energy that can be stored in the output stage, which also means it can supply current for an increased period of time. Therefore by slowing down the di/dt transients in the load, the frequency is effectively decreased.

With the COUT capacitor added to the circuit the inductor current is no longer identical to that seen in the load. The inductor current has a triangular shape, where as the load will see the same basic trend in the current, but all sharp corners become rounded with peaks significantly reduced, as can be seen in Fig. 14 and 13.

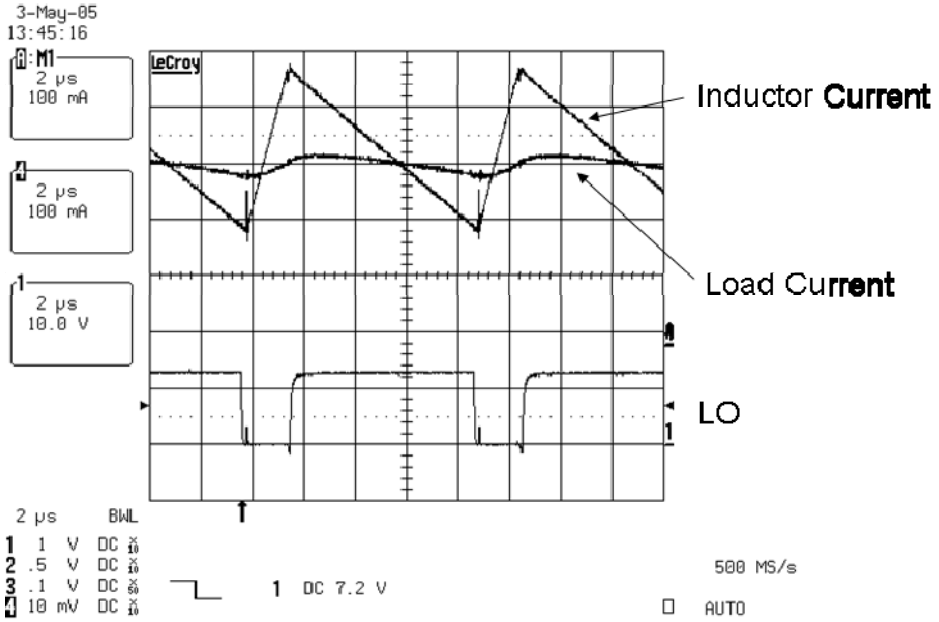


Fig. 14 Iout = 350mA, Vin = 100V, Vout = 16.85V, L = 470uH, COUT = 33uF

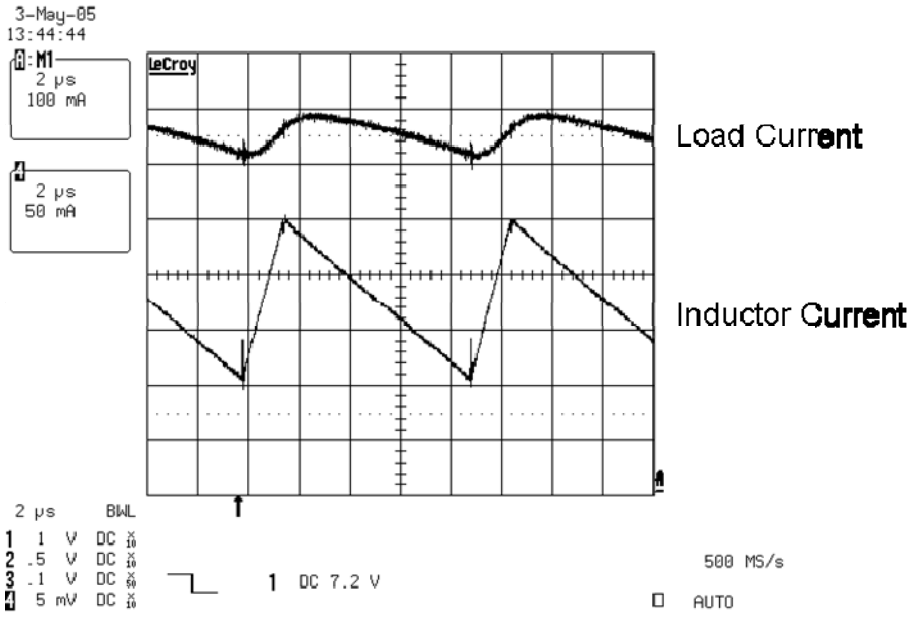


Fig. 15 Iout = 350mA, Vin = 100V, Vout = 16.85V, L = 470uH, COUT = 33uF

Since the system is operating in a free running hysteretic mode, the frequency will adjust to whatever point maintains the regulation of the load current. Since there are fixed delays and a fixed dead time within the IRS2540/1/01/11 controller, the current monitored at the IFB input always overshoots the threshold before the system switches from the energy store phase to the energy release phase. The current must also undershoot the threshold before the system switches back to the energy storage phase. These inherent delays in the system mean that the inductor L1 and capacitor COUT (if used) must be selected to maintain a low enough frequency to minimize this overshoot and undershoot. Output ripple is determined by overshoot and undershoot, which become greater as frequency increases.

The inductor for the IRPLLED1 evaluation board was selected to supply the maximum output current of 1.5A. Due to constraints of size a value of 470uH was chosen, which provides good performance. The IRPLLED1 may be used with or without the output capacitor COUT connected. If COUT is not connected the system runs at higher frequency and consequently with reduced efficiency due to switching losses.

Because of these considerations an inductor of 470uH and an output capacitance of 33uF were chosen to accommodate the 1.5A load current. The current ripple associated with 470uH is relatively small so the board can be operated with or without output capacitance at the lower current ratings.

5. MOSFET vs Diode for the low side switch

The IRS2540/1/01/11 has been designed so that it can drive a low side MOSFET and a high side MOSFET. Alternatively the low side FET can be replaced by a freewheeling diode as shown in Fig. 16. This may yield a lower cost system, but there are some efficiency tradeoffs to be considered, particularly for higher load currents. The system efficiency is directly influenced by several system parameters including operating frequency, load current, and input voltage.
In this evaluation board a fast recovery power diode is used for the lower switch.
A major parameter to consider is the reverse recovery time of the diode in comparison to the body diode of the FET it replaces. The diode intrinsically has a much shorter reverse recovery time since the device is specifically designed for this, where as the body diode is a parasitic element that originates from basic processing technology and typically has inferior characteristics, in terms of forward drop, reverse recovery, and power handling capabilities.

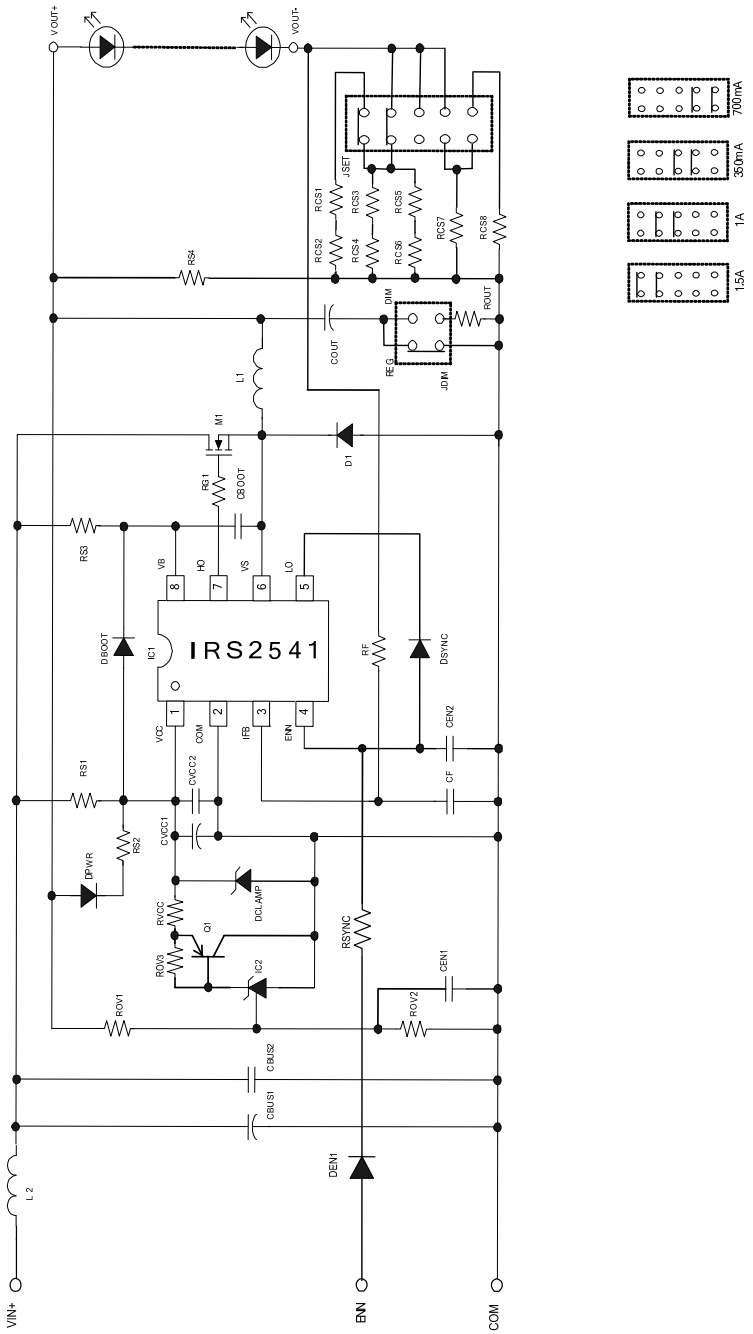


Fig. 16 IRPLLED1 Rev D Evaluation Board Schematic

Note: Rout is needed only in few applications

If a MOSFET is used for the lower switch, reverse recovery losses are incurred during the dead time after the low side MOSFET has been on and conducting current. During this dead time the low side MOSFET is off, but the body diode is freewheeling and providing current to the load. Since the body diode is conducting current, carriers are present and will eventually need to be recombined leading to reverse recovery delay. When the high side MOSFET turns on the VS node is very rapidly pulled from COM to VBUS and the low side MOSFET or the freewheeling diode conducts current from VS to ground due to the reverse recovery effect resulting in power losses. This can result in overheating of the low side switching component and component stress, as can be seen in Fig. 17 to 18. Since the power diode has a much shorter reverse recovery time the diode will conduct current for a significantly shorter period and exhibit lower power losses. At lower frequency and reduced load current, the long recovery time associated with the MOSFET body diode may not be an issue. For higher frequency higher current applications a diode could provide lower power losses with respect to a MOSFET.

With a low side MOSFET fitted to the IRPLLED1 evaluation board reverse recovery current peaks 8A were measured. This resulted in a temperature rise which could be reduced by replacing the low side MOSFET with an appropriate freewheeling diode. The reverse recovery current peaks were reduced to 4.5A. The frequency was also selected to keep the diode reverse recovery associated power losses low.

With the inclusion of a freewheeling diode instead of a low side MOSFET comes the need for an alternative means of pre-charging the bootstrap capacitor CBOOT at startup. RS3 and RS4 provide a current path from the DC bus to VB and from the output to COM in order to accomplish this. After the IRS2540/1/01/11 begins to switch and the high side Buck MOSFET switches off after the first cycle, the voltage at VS transitions to 0V/COM due to the freewheeling action of the lower diode. this allows CBOOT to charge through DBOOT in the normal way and this operation is repeated every cycle. RS4 represents only a small power loss if the output voltage is below 30V, however for higher output voltages a low side MOSFET is necessary.

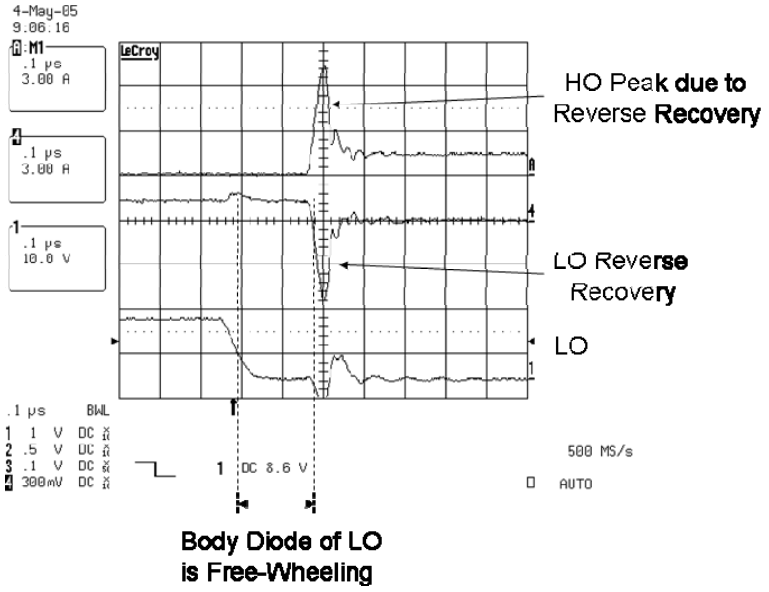


Fig. 17 Using a low side FET, Vin = 100V, Iout = 1.5A, Vout = 17V

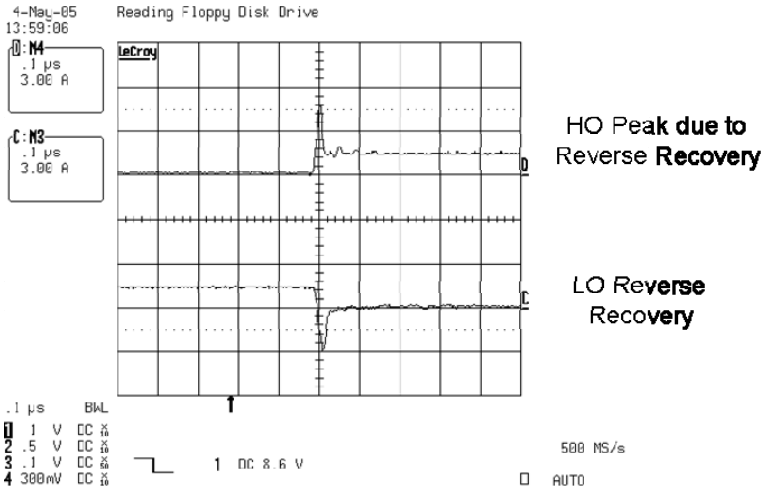


Fig. 18 Using a diode on the low side, Vin = 100V, Iout = 1.5A, Vout = 17V

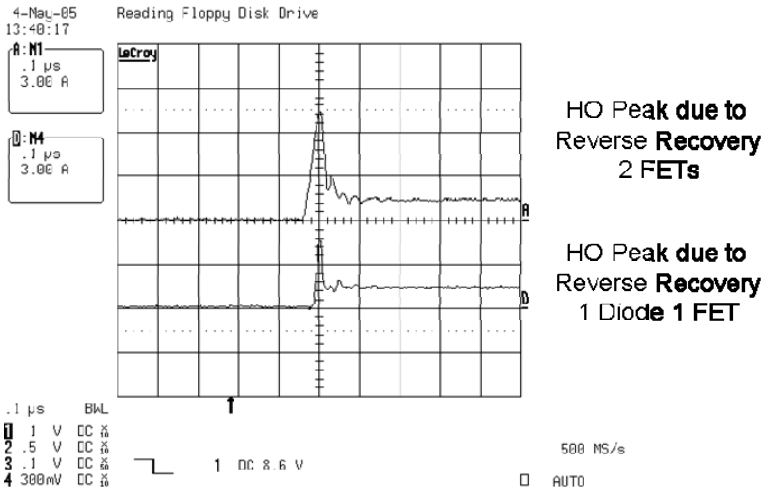


Fig. 19 Low side FET vs. low side diode comparison, Vin = 100V, Iout = 1.5A, Vout = 17V

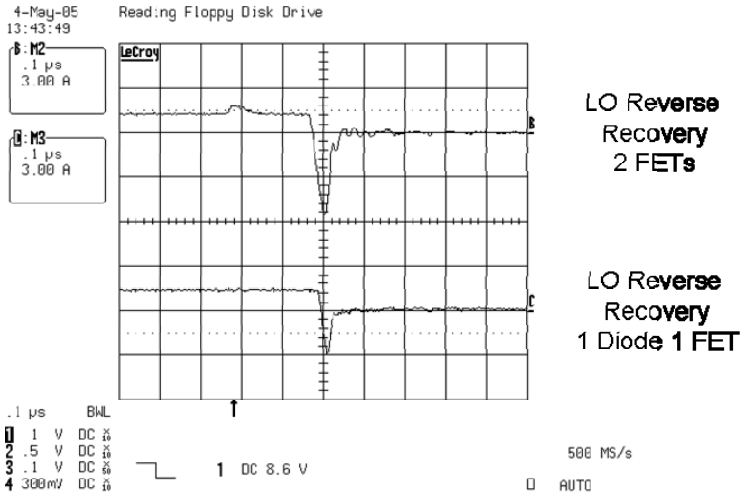


Fig. 20 Low side FET and low side diode comparison, Vin = 100V, Iout = 1.5A, Vout = 17V

Switching losses increase with higher bus voltage. Conduction losses in the lower switch also increase as the difference between input and output voltages increases, since it conducts for a greater part of the switching cycle. A MOSFET has much lower conduction losses than a diode since it has a fixed on resistance and not a fixed junction voltage drop and therefore offers an advantage at higher voltages and currents. A combination of diode and MOSFET together is also a possibility if required. The IRPLLED1 board allows for an additional MOSFET switch M2 to be added. In this case, during the dead time, instead of the body diode free-wheeling the additional diode would be conducting. This will always be the case as long as the forward drop of the external diode is less than that of the body diode.
If the load current is the low hundred milliamps range, the losses in the diode may not be a concern. For optimized system efficiency the forward conduction losses of a diode can also be compared to the reverse recovery losses with a low side MOSFET. For this evaluation board, it was found that conduction losses were less than reverse recovery losses when running at 1.5A and therefore and diode alone was used..

Selecting the correct MOSFET involves finding a part with as low an RDSon low as possible. MOSFET RDSon increases for higher VDS rated parts. Therefore, if a 600V MOSFET is used in a 200V application, extra losses may be incurred due to a component that far exceeds the requirements. If using two MOSFETs the next parameter to be considered is the reverse recovery time. Obviously MOSFETs will not have a reverse recovery time comparable to diodes but a reverse recovery time in the order of 150 to 200ns is possible. The two remaining parameters to consider are direct trade-offs of each other, on resistance and gate charge. If the MOSFET has a relatively low gate capacitance the die size will be small, which will result in a larger on resistance that could potentially be a problem for high current applications. On the other hand, if the MOSFET has a larger gate capacitance the die will be relatively large and the part will have a lower on resistance. In this case more current is needed to turn on the MOSFET therefore requiring more VCC current in the IRS2540/1/01/11 and resulting in higher losses. There has to be a direct compromise between the two. Typically the best solution is a MOSFET with a relatively low RDSon and a medium sized gate capacitance much like the device chosen for this application.

6. VCC Supply

Since the IRS2450/1/01/11 is rated for 200V/600V VBUS can vary considerably in different applications. If a simple supply resistor from VBUS is used for VCC it will experience high power losses at higher bus voltages. For higher voltage applications therefore an alternate V_{CC} supply scheme utilizing a resistor feed-back (RS2) from the output needs to be implemented, as seen in Fig. 1 and Fig. 16. This solution is limited to applications where the LED string voltage exceeds the voltage required to drive VCC, which is about 13V to guarantee good operation.

The resistance between VBUS and V_{CC} (RS1) should be large enough to minimize the current sourced directly from the input voltage line. Through this supply resistor a current will flow to charge the V_{CC} capacitor. Once the capacitor is charged up to the V_{CCUV+} threshold, the IRS2540/1/01/11 begins to operate activating the LO and HO outputs. After the first few cycles of switching the resistor RS2 connected between the output and V_{CC} will take over and source current for VCC from the output. The RS2 resistor provided in the evaluation board has been designed for an output of 16 to 24V. If a higher output voltage is desired, RS2 will need to be increased accordingly. Conversely, if the output voltage is below 20V the value of RS2 may need to be reduced in order to supply sufficient voltage to VCC.

A 10uF capacitor has been used at VCC of the IRS2540/1/01/11, which removes most low frequency ripple that could originate from VBUS due to a rectified voltage waveform.

If the input and output voltages are defined for the evaluation board, enough information is provided to calculate values for RS1, RS2, and RS3 (see Fig. 23 for component definition). All three supply resistors were chosen to be 1W devices since they source all current to the chip. Efficiency can be improved by optimizing these values for specific applications.
By making each component 1W, the work in supplying VCC can be split up equally making it a more robust solution instead of relying entirely on one component. This also allows the chip to turn on at a lower bus voltage.

Assuming that a 14V external zener diode will be used on Vcc, exact values of RS1, RS2, and RS3 are calculated as follows (values calculated to operate the components just below half their rated power):

$$P = V^2 / R$$

RS1

$$\tfrac{1}{2}W = \frac{\left(V_{Bus_{\max}} - 14V\right)^2}{RS1}$$

$$RS1 = \frac{\left(V_{Bus_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{(170V - 14V)^2}{\tfrac{1}{2}W}$$

$$RS1 = 48.6k\Omega \approx 56k\Omega$$

RS3

min duty ratio ≈ 10%

$$\tfrac{1}{2}W = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14V\right)^2}{RS3}$$

$$RS3 = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{(1-0.1)\cdot(170V - 14V)^2}{\tfrac{1}{2}W}$$

$$RS1 = 43.8k\Omega \approx 47k\Omega$$

RS2

$$\tfrac{1}{2}W = \frac{\left(V_{Out_{\max}} - 14V\right)^2}{RS2}$$

$$RS2 = \frac{\left(V_{Out_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{\left(30V - 14V\right)^2}{\tfrac{1}{2}W}$$

$$RS1 = 512\Omega \le 1k\Omega$$

RS1 may be rounded up to 1K

7. VBS Supply

The bootstrap diode (DBOOT) and supply capacitor (CBOOT) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before operation commences, the first pulse from the output drivers comes from the LO pin. During under voltage lock-out mode, the high and low-side outputs are both held low.

During an open circuit condition, without the watchdog timer, the HO output would remain high at all times and the charge stored in the bootstrap capacitor (CBOOT) would slowly leak until reaching zero, thus eliminating the floating power supply for the high side driver. To maintain sufficient charge on CBOOT, a watchdog timer has been implemented. In the condition where VIFB remains below VIFBTH, the HO output will be forced low roughly after 20µs and the LO output forced high. This toggling of the outputs will last for 1µs to maintain and replenish sufficient charge on CBOOT.

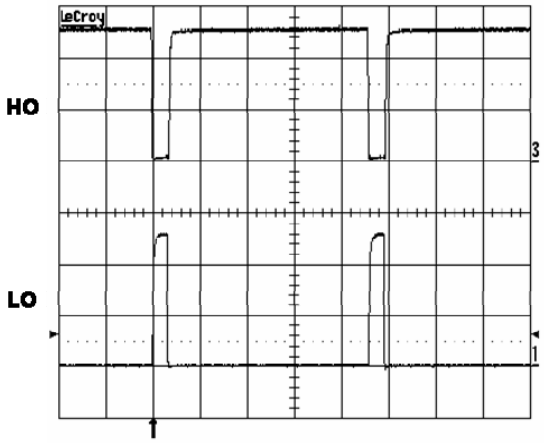


Fig. 21 Illustration of Watchdog Timer

The bootstrap capacitor value needs to be chosen so that it maintains sufficient charge for at least the 20µs interval until the watchdog timer allows the capacitor to recharge. If the capacitor value is too small, the charge will fully dissipate in less than 20µs. The bootstrap capacitor should be at least 100nF. A larger value within reason can be used if preferred.

The bootstrap diode should be a fast recovery, if not an ultrafast recovery component to maintain good efficiency. Since the cathode of the bootstrap diode will be switching between COM and VBUS + 14V, the reverse recovery time of this diode is of critical importance. For additional information concerning the bootstrap components, refer to the Design Tip (DT 98-2), *"Bootstrap Component Selection For Control ICs"* at www.irf.com under Design Support.

8. Enable Pin

The enable pin can be used for dimming or open-circuit protection. When the ENN pin is held low the IRS2540 remains in a fully functional state with no alterations to the operating environment. To disable the control feedback and regulation a voltage greater than VENTH (approximately 2.5V) needs to be applied to the ENN pin. With the chip in a disabled state the HO output will remain low and the LO output will remain high to prevent VS from floating, in addition to maintaining charge on the bootstrap capacitor if a MOSFET is used for the lower switch. The threshold for disabling the IRS2540/1/01/11 has been set to 2.5V to enhance immunity to any externally generated noise or application ground noise and also makes it possible receive a drive signal from a microcontroller.

Dimming Mode

To achieve dimming a signal with constant frequency and set duty cycle can be fed into the ENN pin. There is a direct linear relationship between the average load current and duty cycle if no output capacitor is used in the circuit. A large output capacitor tends to increase the minimum dim level because some current continues to supply the LEDs from this capacitor during the off phase of the PWM dimming. With no output capacitor, if the ratio is 50% then 50% of the maximum set light output will be emitted. Similarly if the ratio is 30% then 70% of the maximum set light output will be realized. A sufficiently high frequency of the dimming signal must be chosen to avoid visible flashing or "strobe light" effect. A signal around 1kHz from zero to 5V is recommended. For this evaluation board, a fully adjustable (0% to 100% duty cycle) PWM wave generator is suggested but this is not included as part of the evaluation board. The following circuit is a simple enable pin dimming signal generator.

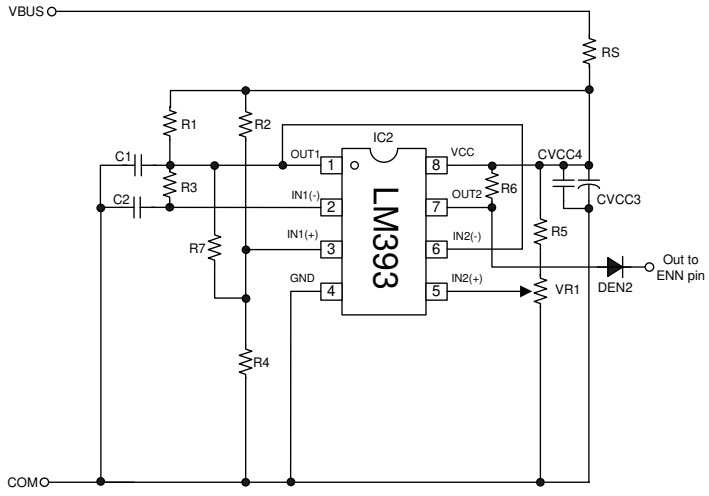


Fig. 22 Suggested PWM Driver (not included in IRPLLED1.5X2)

If an external supply for VCC is used, the minimum amount of dimming achievable (light output approaches 0%) will be determined by the "on" time of the HO output, when in a fully functional regulating state. To maintain reliable dimming, it is recommended to keep the "off" time of the enable signal at least 10 times that of the HO "on" time. For example, if the application is running at 75kHz with an input voltage of 100V and an output voltage of 20V, the HO "on" time will be 2.7µs (one-fourth of the period – see calculations below) according to standard buck topology theory. This will set the minimum "off" time of the enable signal to 27µs.

$$Duty\ Cycle = \frac{V_{out}}{V_{in}} * 100 = \frac{20V}{100V} * 100 = 20\%$$

$$HO_{on\ \text{time}} = 20\% * {}^{1}\!/_{75kHz} = 2.7\mu s$$

If the IRS2540/1/01/11 is supplied from the output, a large enough capacitor on VCC is required to maintain sufficient current while in a disabled state. For this evaluation board where the IC supply comes from the output, a 10uF capacitor is used to ensure continued operation while disabled. The output is capable of dropping to roughly 10V. A "strobe light" effect in the LEDs may be observed if VCC drops too much or if the dimming frequency is too low.

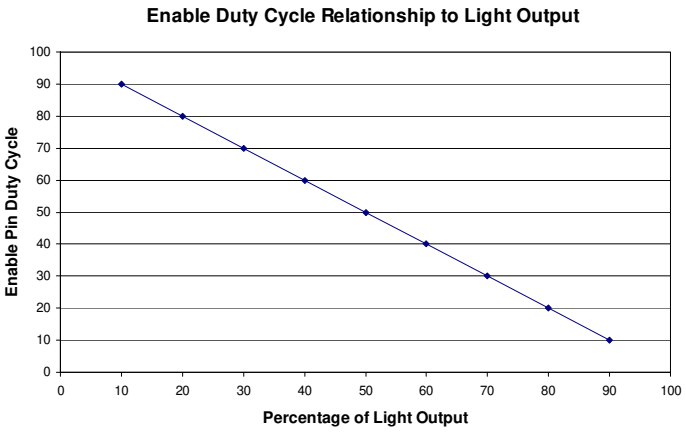


Fig. 23 Light Output vs Enable Pin Duty Cycle

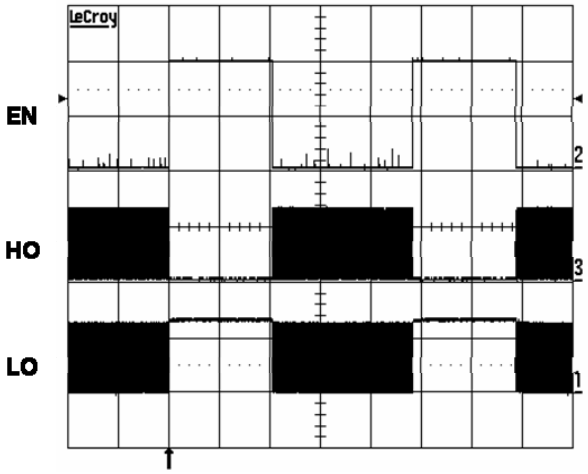


Fig. 24 IRS2540 Dimming Signals

Since the IRS2540/1/01/11 does not include an onboard oscillator, a soft start feature is not easily implemented. This is only a concern when operating in the dimming mode. Since PWM dimming is required of LEDs, the output is essentially turning on and off at a rate of the dimming frequency. In the absence of soft start a large spike of current would be observed in the load each time the output is turned on. This current spike stresses the load possibly decreasing LED operating lifetime. The IRPLLED1 includes a jumper setting to define whether or not the board is being used in the dimming mode. This two position jumper allows the designer to either include or exclude the resistor Rout, which is in series with the output capacitor. The inclusion of this resistor will sufficiently damp the

output stage, such that output current spikes are reduced or eliminated. The presence of such current spikes may cause the inductor to hum or buzz where the emitted sound will be that of the dimming frequency. The inrush of current produces mechanical movement in the inductor due to the change in magnetic field, which can be heard since the PWM signal is within the audible range of the human ear. The effects of adding in Rout can be seen in Fig. 25 – 28.

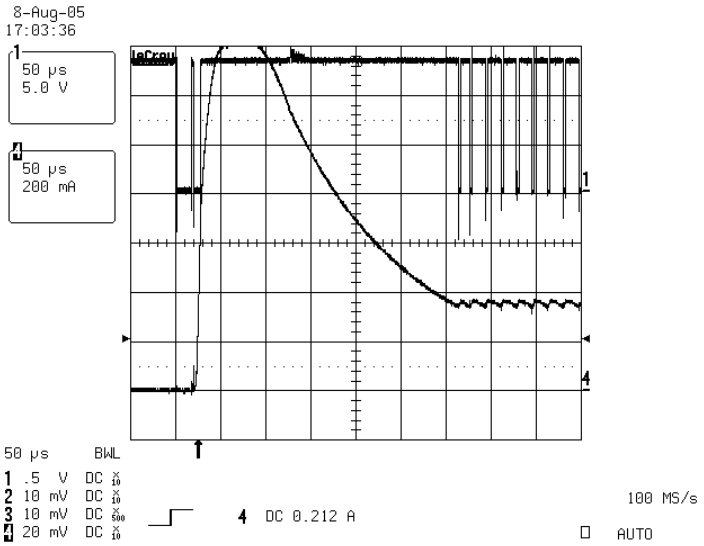


Fig. 25 Load Current Spike Excluding Rout
Iout = 350mA, Vin = 100V, Vout = 17V

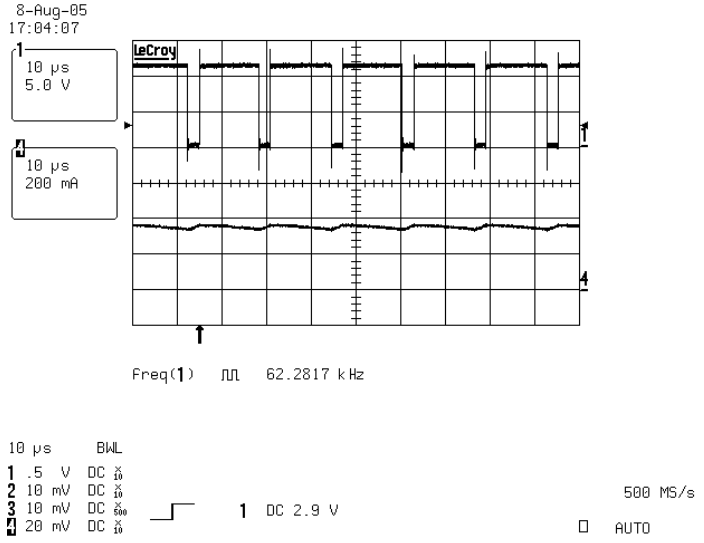


Fig. 26 Load Current Ripple Excluding Rout
Iout = 350mA, Vin = 100V, Vout = 17V

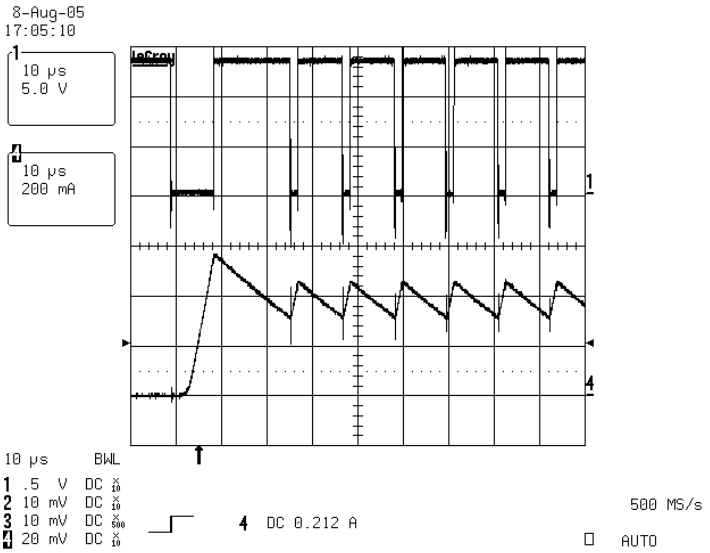


Fig. 27 Load Current Spike Including Rout (5ohm)
Iout = 350mA, Vin = 100V, Vout = 17V

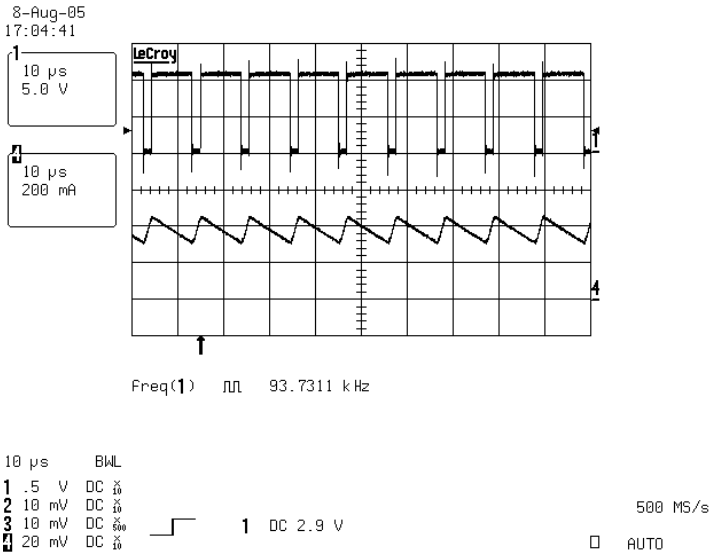


Fig. 28 Load Current Ripple Including Rout (5ohm)
Iout = 350mA, Vin = 100V, Vout = 17V

Although the inclusion of the resistor Rout minimizes or eliminates the load current spikes, the overall current regulation and operating frequency will be slightly compromised. The resistor reduces the overall effectiveness of the output capacitor, which means the switching frequency will marginally increase. The output ripple current will also increase, which ultimately leads to a larger current regulation tolerance. Although the overall current regulation capabilities may decrease with the inclusion of this resistor, the actual stability of the PWM dimming signal will still be the dominant factor of the overall output current regulation capabilities.

It should be noted that the IRPLLED1 reference design board reflects the schematic of Figure 16 where a high speed diode is used in place of the lower MOSFET switch indicated in Figure 1.

The addition of resistor RSYNC and diode DSYNC synchronizes the ENN input signal such that, when ENN transitions from low to high to disable the oscillator during a period when HO is high, the IRS2540 will not react

until the end of the current HO cycle as shown in the waveform diagram below. The reason for this is to avoid the possibility off ENN transitioning from low to high at the exact time that HO transitions from low to high, which may trigger the HO output to latch up under a low VBS supply condition. This is caused by propagation delays that exist inside the IC. RSYNC and DSYNC are not necessary in non-dimming applications. Synchronization as described will not affect the operation or dimming functionality of the circuit. It will serve only to protect the circuit against a possible fault condition, without any detrimental effect to operation. The revised IRS25401 and IRS25411 contain internal circuitry to protect against possible latch up conditions and do not require RSYNC and DSYNC.

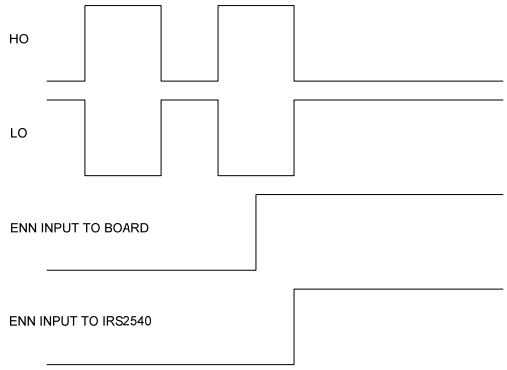


Fig. 28a: Dimming Synchronization Waveforms.

9. Open circuit protection

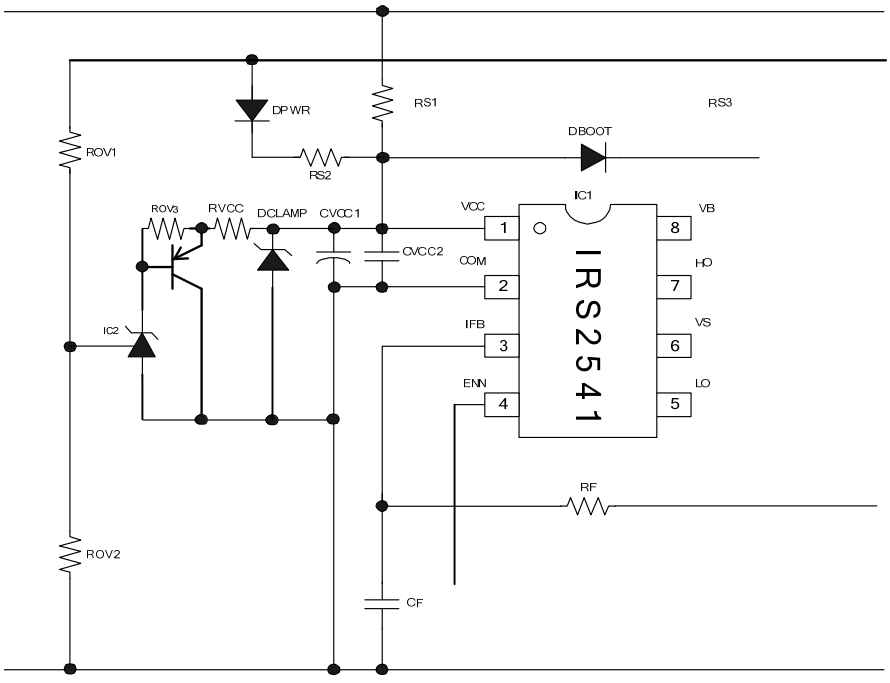


Fig. 29 IRPLLED1 Improved Open Circuit Protection Scheme

The overvoltage / open-circuit protection circuit shown in Figure 29 replaces schemes used on previous versions of the IRPLLED1 reference design. This method offers far more reliable performance over the range of operating conditions with or without an output capacitor. It also works reliably during PWM dimming.

The output over voltage / open circuit protection circuit shown in Figure 29 allows the designer to program the allowable maximum output voltage by means of ROV1 and ROV2. An industry standard programmable zener diode type LM431 (IC2) is used to pull down the base of Q1, which pulls down on VCC when the divided voltage from ROV1 and ROV2 exceeds the internal 2.5V reference. IC2 is capable of sinking no more than 100mA and in the SOT-23 package has limited power handling ability, therefore Q1 was added to pull down the VCC voltage fed from RS1 and RS2 to below the under voltage lockout threshold VCCUV- of the IRS2540/1/01/11 causing it to shutdown. This circuit reacts very rapidly when the output voltage exceeds the predetermined level. It operates whether or not an output capacitor is connected, i.e. in any of the alternative JDIM jumper positions.
The over voltage protection threshold has been set to 32V in the IRPLLED1 Rev D demo board to allow one or two standard LED panels to be connected in series to the output before reaching a voltage level high enough to trigger the protection circuit. The open circuit protection circuit operates in hiccup mode such that Q1 pulls the VCC voltage below the VCCUV- threshold causing the IRS2540/1/01/11 to switch off and enter micro power mode and the output to fall to zero. VCC then charges up again through RS1 until the voltage again exceeds VCCUV+ and the IRS2540/1/01/11 starts up again. The sequence then repeats until a load is added to clamp the output voltage.

The above circuit is able to limit the output voltage to a series of pulses instead of a DC level. However it should be noted reducing the average output voltage **does not prevent the possibility of electric shock in non-isolated systems!** Therefore an IRS2540/1/01/11 based Buck LED driver running directly off line would still be an electric shock hazard and it would **not** be safe to attempt to replace the LEDs if such a system were powered. In non-isolated systems, additional mechanical protection is required to ensure that access to the LEDs is not possible or alternative a mechanical isolation system could be used to disconnect the LEDs completely from the ballast for safe access. In an illuminated sign for example, this would be a reasonable approach.

The open circuit protection system described in this section can only be an effective safety feature in a system where the IRS2540/1/01/11 Buck stage is used as a back end stage supplied by an already isolated DC source. It does however serve to limit the output voltage to prevent damage to the output capacitor COUT in cases where the bus voltage is greater than the rating of this capacitor.

Note:
The over voltage protection scheme used in the IRPLLED1 evaluation board is different to that used in earlier revisions of the IRPLLED1 and does not conflict with the synchronization operation described in the previous section.

The open load protection circuit in Fig 29 is recommended for isolated non-dimming applications where the load may be disconnected and then reconnected without shutting down the driver. When the load is reconnected with power on this would reduce the initial surge of current to the output reducing stress on the LEDs.
In an open circuit condition, switching will continue at the HO and LO outputs, whether due to the output voltage clamp or to the watchdog timer.

Due to the operation of this circuit the output voltage under open circuit conditions where JDIM is in the DIM position is made up of pulses as shown in Fig 30. If JDIM is in the REG position then these pulses will delay slowly as the output discharges. This can leave an average voltage of approximately 50V at the output. The decay rate of these pulses depends on the value of COUT and the interval between pulses depends on the time taken for CVCC1 to charge above VCCUV- through RS1 and therefore depends on the input voltage.

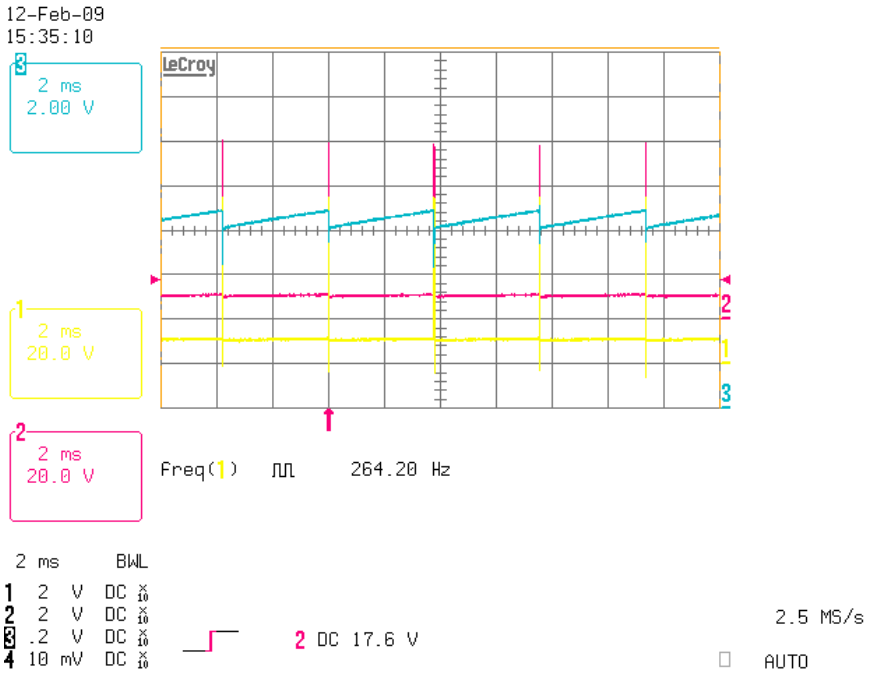


Fig. 30 Open Circuit Fault Signals, with Clamp

The yellow waveform shows the output voltage and the red waveform shows the VS switching waveform. In this example there is no output capacitor. When the output goes above the over voltage threshold the VCC voltage shown in blue is quickly pulled below VCCUV- and then gradually charges back up to VCCUV+ through RS1. If an output capacitor is connected then VCC is pulled almost to zero by IC3 and the systems takes longer to re-start.

$$V_{out} = 2.5 \cdot \frac{(R_{OV1} + R_{OV2})}{R_{OV2}}$$

The values of the divider resistor ROV1 and ROV2 are calculated as follows:
Let ROV2 = 10K

$$V_{out} = 2.5 \cdot \frac{(R_{OV1} + R_{OV2})}{R_{OV2}}$$

$$R_{OV1} = \frac{V_{out} R_{OV2}}{2.5} - R_{OV2} = \frac{32V \cdot 10k\Omega}{2.5} - 10k\Omega = 118k\Omega$$

$$R_{OV1} \approx 120k\Omega$$

10. Other Design Considerations

Filtering

The RC filter at the IFB pin is used to remove high frequency transients associated with the switching. The corner frequency of this filter was left high enough to prevent any further distortion of the feedback signal.

The input filter is a low-pass filter. Its main objective is to prevent ringing of comparable frequency on Vbus. Exact values of capacitance and inductance are not of critical importance, so long as adequate filtering is accomplished. In addition to the electrolytic capacitor that is used for filtering on the bus there is also a small ceramic for decoupling of high frequency noise. Ceramic capacitors typically have low ESR such that they are more ideal for high frequency filtering.

The IRS2540/1/01/11 was specifically designed to handle low frequency ripples on VBUS. Its capability to handle such ripple makes it ideal for an offline rectified waveform. However if high voltage (on the order of 5V-10V) high frequency oscillations (greater than or close to the operating frequency) are present on VBUS, it is recommended to implement an input filter. If these high frequency signals are present on VBUS the IRS2540/1/01/11 will still continue to regulate the current through the load, however abnormal switching of LO and HO may be observed. This poses a problem in terms of switching losses. As previously discussed, the application may need to control the operating frequency to optimize the system efficiency. Excessive high frequency ripple at the DC bus could cause the frequency to become unstable, since this system relies on a self-oscillating principle and is sensitive to noise. Careful attention to the PCB layout is also necessary for this system to operate correctly. If filters on IFB and VCC are not placed correctly, high frequency ripple will couple to the IFB input and interfere with the operation of the control loop. Also if the load current is 1A or 1.5A, when HO turns on the load immediately tries to draw this current. Since the circuit supply is not usually close by, the capacitance of the input wire is not enough to compensate for this large pull of current and this can result in oscillations or change in potential on the input line. To alleviate the circuit of such potential problems it is advisable to implement an input filter. The input filter will also greatly improve the EMC performance.

EMC performance

The IRPLLED1 evaluation board has not been EMC tested. Input and Output filters can be used to reduce the conducted emissions to below the limits of the applicable EMC standard as needed. Inductors may require a powdered Iron core rather than Ferrite, which can handle a much larger current before saturating. If EMC is of critical importance, it may be beneficial to use a MOSFET for the upper switching element and a diode for the lower switch. The reverse recovery time for a diode is inherently shorter than that of a MOSFET and this can help in reducing transients observed in the switching elements resulting in better EMC performance.

Layout Considerations

It is very important when laying out the PCB for the IRS2540/1/01/11 based ballast to consider the following points:

1. CVCC2 and CF must be as close to IC1 as possible.
2. The feedback path should be kept to a minimum without crossing any high frequency lines.
3. COUT should be as close to the main inductor as possible.
4. All traces that form the nodes VS and VB should be kept as short as possible.
5. It is essential that all signal and power grounds should be kept separated from each other to prevent noise from entering the control environment. Signal and power grounds should be connected together at one point only, which must be at the COM pin of the IRS2540/1/01/11. The IRS2540/1/01/11 is very sensitive to noise and will not operate if these guidelines are not followed!