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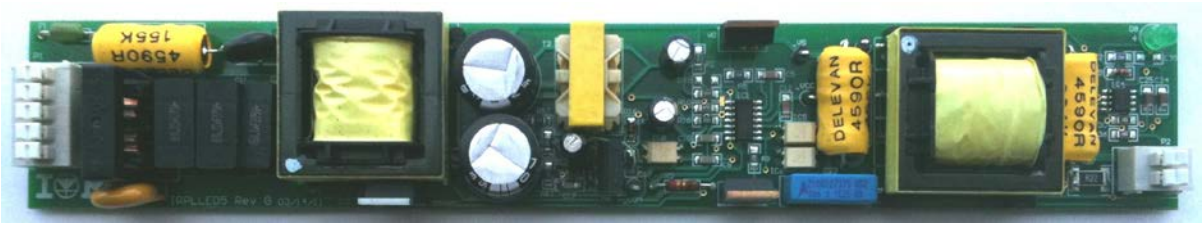
Application Note AN-1169

IRPLLED5
40V/1.4A Low Voltage LED Driver using IRS2548D

By Peter B. Green

Table of Contents

EVALUATION BOARD - IRPLLED5



1. Introduction

Solid state light sources are now available that offer viable alternatives to Fluorescent and HID lamps and far surpass incandescent lamps. Luminous efficacy expressed in Lumens per Watt has now reached levels enabling LEDs to be used for general illumination. High brightness LEDs also possess the added advantages of longer operating life span up to 50000 hours and greater robustness than other less efficient light sources making them suitable for outside applications such as street lighting.

High power LEDs are ideally driven with constant regulated DC current, requiring a "driver" or "converter" to provide the required current from an AC or DC power source. A two stage power converter based around the IRS2548D PFC plus half bridge LED driver IC provides a controlled current output over a wide AC line voltage input range with high power factor and low THD.

The IRPLLED5 evaluation board is an off line isolated low voltage / high output current LED driver designed to supply a 1.4A regulated DC output current over a voltage range of 30V to 60V operating from an AC line input voltage between 90 and 305VAC 50/60Hz. It also includes 1-10V dimming capability from 0 to 100% of light output. The outputs of this LED driver are fully protected against short circuit and limit the open circuit voltage to below 60VDC for safety compliance.

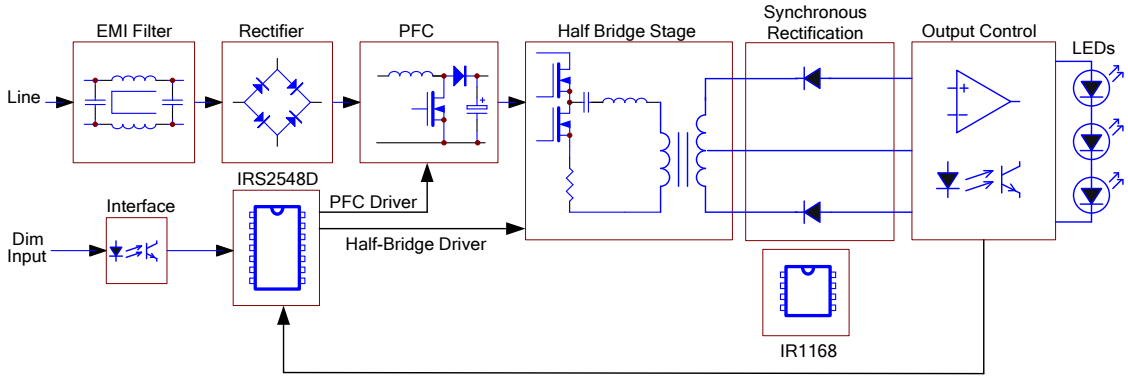


Figure 1: IRPLLED5 Block Diagram

2. PFC Section

The IRPLLED5 board includes a power factor correction Boost converter front end stage, which operates in critical conduction mode. During each switching cycle of the PFC MOSFET the IRS2548D detects the point at which the inductor current has discharged to zero thereby detecting when the stored energy has been completely transferred to the output. The PFC MOSFET is then turned on to start the next switching cycle.

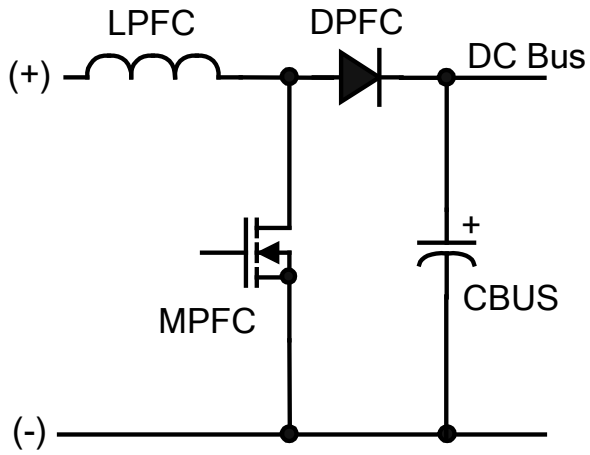


Figure 2: PFC Boost converter circuit.

When the switch MPFC is turned on the inductor LPFC is connected between the rectified line input (+) and (-) return causing the current in LPFC to rise linearly. When MPFC is turned off LPFC current is redirected from the rectified line input (+) bus to the DC bus capacitor CBUS through diode DPFC. The stored energy in LPFC is thereby transferred to CBUS. MPFC is switched on and off at a high frequency and the voltage on CBUS charges to a defined voltage. The PFC feedback loop of the IRS2548D regulates this voltage to by continuously monitoring the DC bus voltage and adjusting the on-time of MPFC accordingly. Negative feedback control is performed by a transconductance error amplifier (OTA) with a slow loop speed such that the average inductor current smoothly follows the low frequency line input voltage. This produce a sinusoidal input current yielding high power factor and low THD. The on-time of MPFC is therefore effectively constant (with an additional modulation to be discussed later) only changing over several cycles of the line voltage. With fixed on-time and off-time determined by the inductor current discharging to zero the switching frequency changes from a high frequency near the zero crossing of the AC input line voltage to a lower frequency at the peaks (Figure 3).

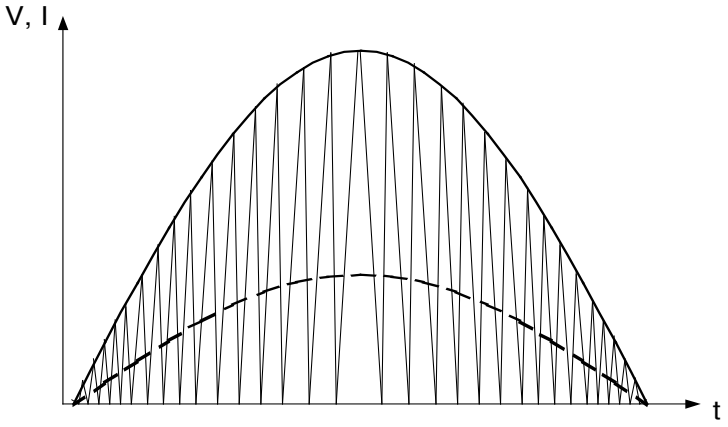


Figure 3: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line.

When the line input voltage is low close to the zero crossing, the inductor current also rises to a relatively low peak so the discharge time is also shorter resulting in a high switching frequency. When the input line voltage is high near the peak the inductor current rises to a much higher peak and the discharge time is therefore longer resulting in a lower switching frequency. The PFC control circuit of the IRS2548D (Figure 4) includes five control pins: VBUS, COMP, ZX, PFC and OC. The VBUS pin measures the DC bus voltage via an external resistor voltage divider. The COMP pin voltage at the error amplifier output sets the on-time of and the speed of the feedback loop with an external capacitor. The ZX (zero crossing) pin detects when the inductor current discharges to zero during the off time using a secondary winding from the PFC inductor. The PFC pin is the gate driver output for the external MOSFET, MPFC and the OC pin senses the current flowing through MPFC providing cycle-by-cycle over-current protection.

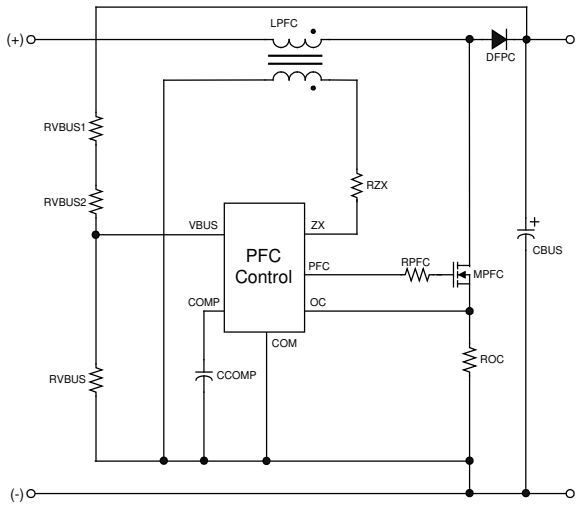


Figure 4: IRS2548D simplified PFC control circuit.

The VBUS pin is regulated against a fixed internal 4V reference voltage for regulation of the output DC bus voltage (Figure 5). The feedback loop error amplifier sinks or sources a current to the external capacitor at the COMP pin. The IRS2548D PFC section operates in voltage mode with the COMP pin voltage providing the threshold for the charging the internal timing capacitor (C1, Figure 5) to control the on-time of MPFC.

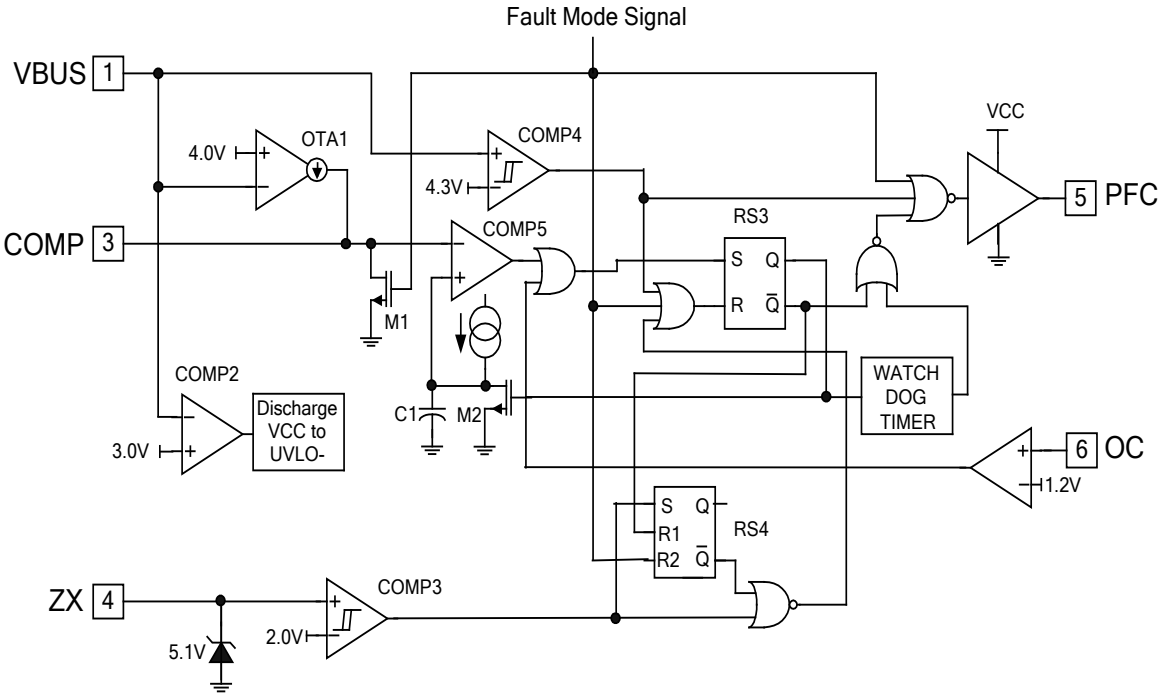


Figure 5: IRS2548D detailed PFC control circuit.

The zero current level is detected by a secondary winding on LPFC connected to the ZX pin through an external current limiting resistor RZX. A positive-going edge exceeding the internal 2V threshold (VZXTH+) signals the beginning of the off-time. A negative-going edge on the ZX pin falling below 1.7V (VZXTH+ - VZXHYS) will occur when the LPFC current discharges to zero, which signals the end of the off-time and MPFC is turned on again (Figure 6). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the half-bridge driver section (Fault Mode), an over-voltage or condition on the DC bus or the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin fail to be detected for any reason MPFC will remain off until the internal “watch-dog” timer forces a restart. Watch-dog pulses occur every 400us (tW) until a correct positive and negative-going signal is detected on the ZX pin and normal PFC operation is resumed. Should the OC pin exceed the 1.2V (VOCTH+) over-current threshold during the on-time, the PFC output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the PFC output on again.

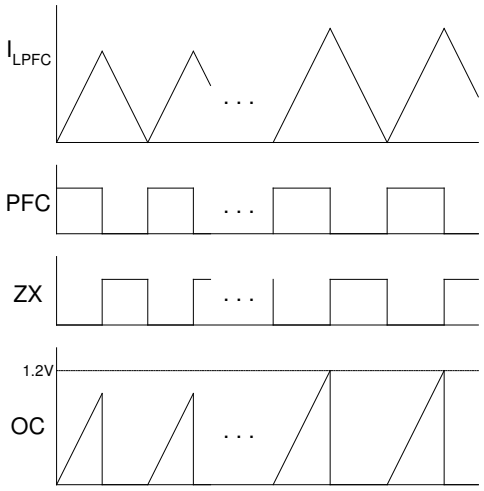


Figure 6: Inductor current, PFC pin, ZX pin and OC pin timing diagram.

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current that naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage to provide a high power factor. Some harmonic distortion of the line current still remains mostly due to cross-over distortion near the zero-crossings. To achieve low THD additional on-time modulation circuit is built into the IRS2548D PFC control. This function dynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 7). This causes the peak LPFC current, and therefore the smoothed line input current, to increase slightly higher near the zero-crossings of the line input voltage.

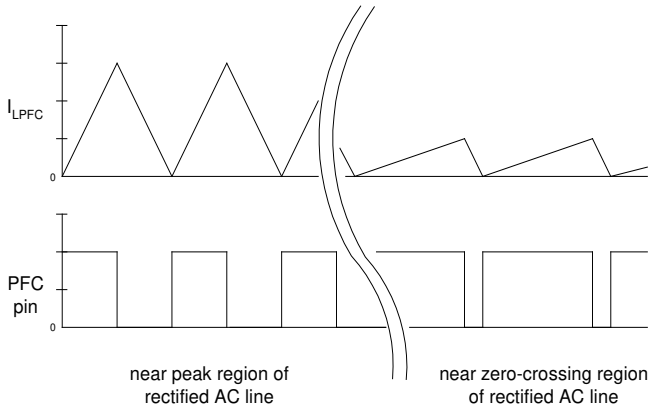


Figure 7: On-time modulation circuit timing diagram

Should over-voltage occur on the DC bus and the VBUS pin exceed the internal 4.3V threshold (VBUSOV+) the PFC output will transition to switch off MPFC.

When the DC bus decreases again and the VBUS pin voltage decreases below the internal 4.15V threshold (VBUSOV-) PFC operation is resumed.

The PFC inductor value can be calculated from the following formula:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad \text{[Henries]}$$

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum RMS AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = System output power

The peak current in the PFC inductor is given by:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad \text{[Amps Peak]}$$

The PFC inductor should be designed so that it does not saturate at i_{PK} at maximum operating temperature. This involves adequate sizing of the core and air-gap.

The value of the PFC current sense resistor (ROC) is calculated from the following formula and rounded up to the nearest preferred value.

$$R_{OC} = \frac{1.25}{i_{PK}} \quad \text{where VCSTH+ = 1.25V} \quad \text{[Ohms]}$$

3. LLC Resonant Half Bridge Section

The run frequency is programmed with the timing resistor RFMIN at the FMIN pin.
The graph in Figure 6 (RFMIN vs. Frequency) can be used to select RFMIN value for desired run frequency.

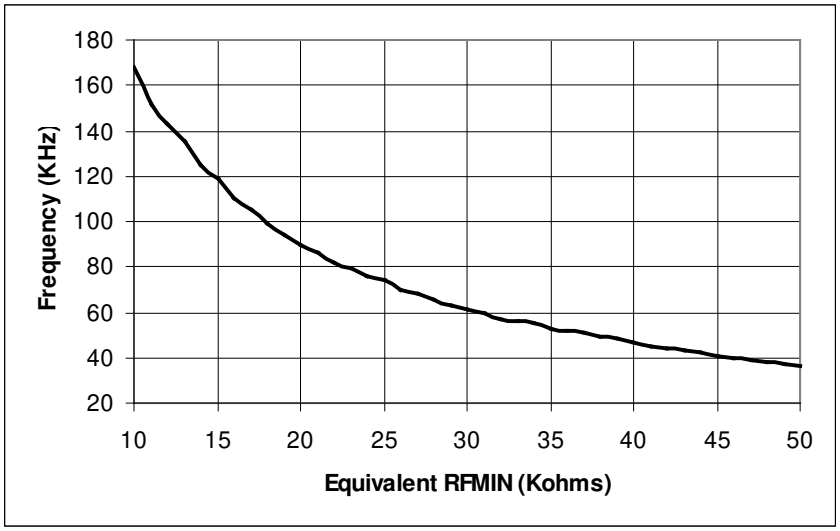


Figure 8: Graph of frequency against RFMIN

The maximum current is programmed with the external resistor RCS and an internal threshold of 1.25V (VCSTH+). This threshold determines the over-current limit of the system:

$$I_{MAX} = \frac{1.25}{R_{CS}}$$ [Amps Peak]

or

$$R_{CS} = \frac{1.25}{I_{MAX}}$$ [Ohms]

The half-bridge LLC resonant converter offers high efficiency due to zero voltage switching operation which also eliminates switching noise. Since the switching losses are negligible no heat sinking is required for the half-bridge MOSFETs. This topology can achieve high power density due to the efficient utilization of the transformer operating in two quadrants of the B-H curve. The resonant topology requires an additional series inductance to be added to the circuit in order to construct a complex resonant tank with Buck-Boost transfer characteristics in the soft switching region. Although it is possible to incorporate this additional

inductance into the transformer, for simplicity the IRPLLED5 design uses a standard transformer design with the additional inductance added externally. The typical power stage schematic for this topology is shown in figure 9.

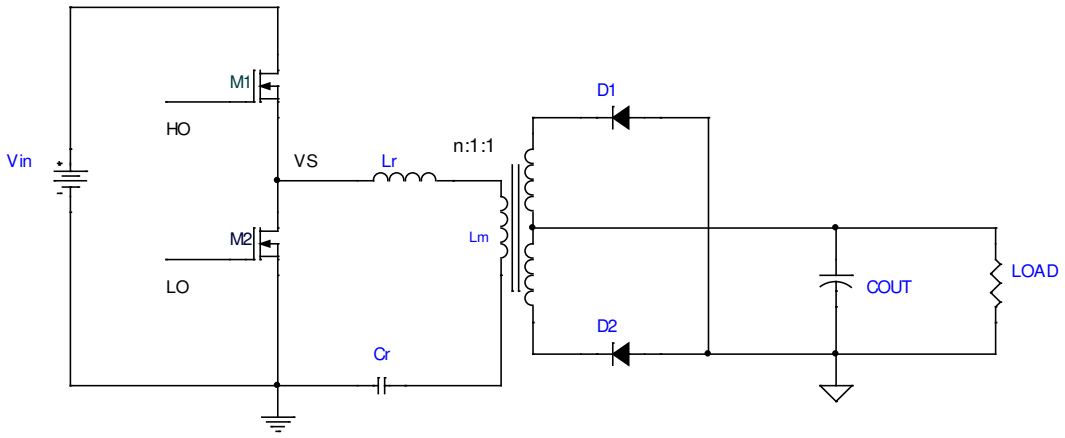


Figure 9: Typical schematic of a DC-DC half-bridge resonant converter

The half-bridge switches operate at 50% duty cycle where the output voltage is regulated by varying the switching frequency. Since the IRPLLED5 drives an LED load which can be approximately represented by a voltage source with a series resistor. The current is regulated by adjusting the half-bridge switching frequency. The frequency is adjusted to provide the required drive current for varying numbers of LEDs connected to the output up to a total series voltage of 60V. The LLC half-bridge stage has two resonant frequencies, the first determined by the series inductor (Lr) and resonant capacitor (Cr) and the second determined by the transformer magnetizing inductance (Lm) and the resonant capacitor. While the frequency remains in the inductive region soft switching will occur.

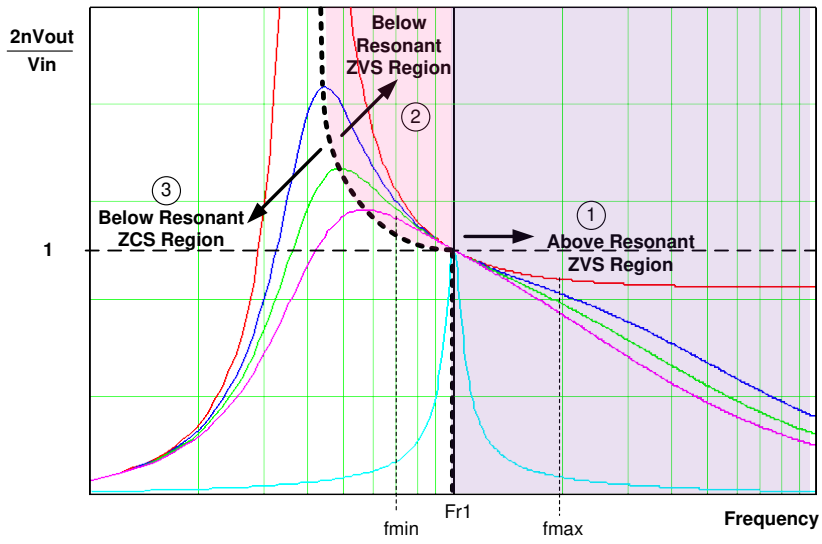


Figure 10: Typical frequency response of an LLC resonant converter

The characteristics of an LLC resonant converter can be divided into three regions based on the three different modes of operation. The first region is for switching frequency above the resonant frequency F_{r1}:

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}$$

In region 1 of figure 10 (the purple shaded area) the switching frequency is higher than resonant frequency F_{r1}. The converter operation is very similar to a series resonant converter. Here L_m never resonates with resonant capacitor (C_r) it is clamped by the output voltage and acts as the load of the series resonant tank. This is the inductive load region and the converter is always under ZVS operation regardless of the load condition.

In region 2 (the pink shaded area) the switching frequency is higher than the lower resonant frequency but lower than F_{r1}. The lower resonant frequency varies with load so the boundary of region 2 and region 3 traces the peak of the family load vs gain curves. In this complex region the LLC resonant operation can be divided into two time intervals; in the first time interval L_r resonates with C_r and L_m and is clamped by output voltage. When the current in the resonant inductor L_r resonates back to the same level as the magnetizing current L_r and C_r stop resonating. L_m now participates in the resonant operation and the second time interval begins. During this time interval the dominant resonant components become C_r and L_m in series with L_r. The ZVS operation in region 2 is guaranteed by operating the converter to the right side of the load gain curve. For a switching frequency below resonant F_{r1} it could fall in either region 2 or region 3 depending on the load condition.

In the ZCS range below f_{r1}, the LLC resonant converter operates in capacitive mode; M1 and M2 are hard switching with high switching losses. For this reason ZCS operation should always be avoided.

The waveforms in figures 11,12 and 13 show the behavior of the system in each of the operating regions. The typical voltage conversion ratio of a LLC resonant converter is shown in Figure 12.

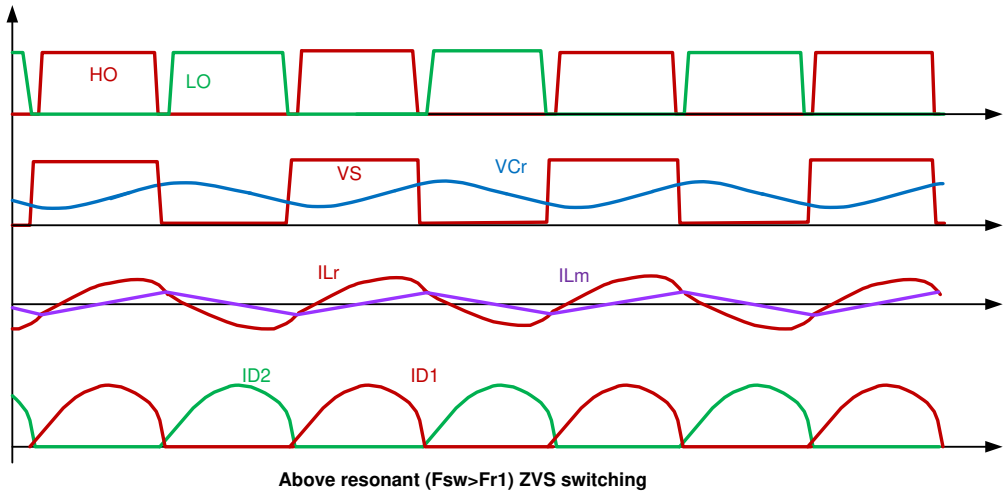


Figure 11: Typical waveform of above resonant ZVS switching

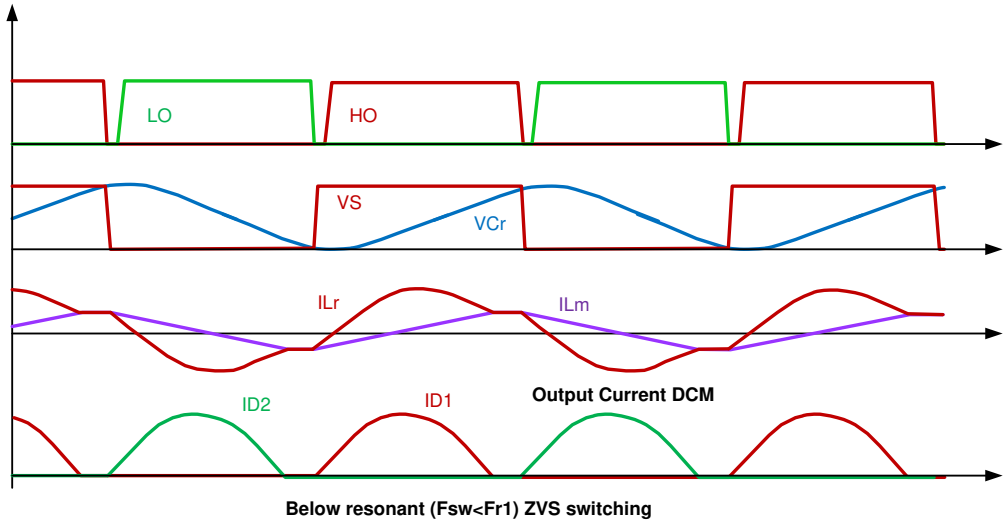


Figure 12: Typical waveform of below resonant ZVS switching

The waveforms in figure 12 indicate that the secondary rectifier diode currents move from continuous current mode (CCM) to discontinuous current mode (DCM) when the switching frequency changes from above resonant ZVS to below resonant ZVS due to load increasing. The ripple voltage on the resonant capacitor C_r also increases in the below resonant ZVS mode.

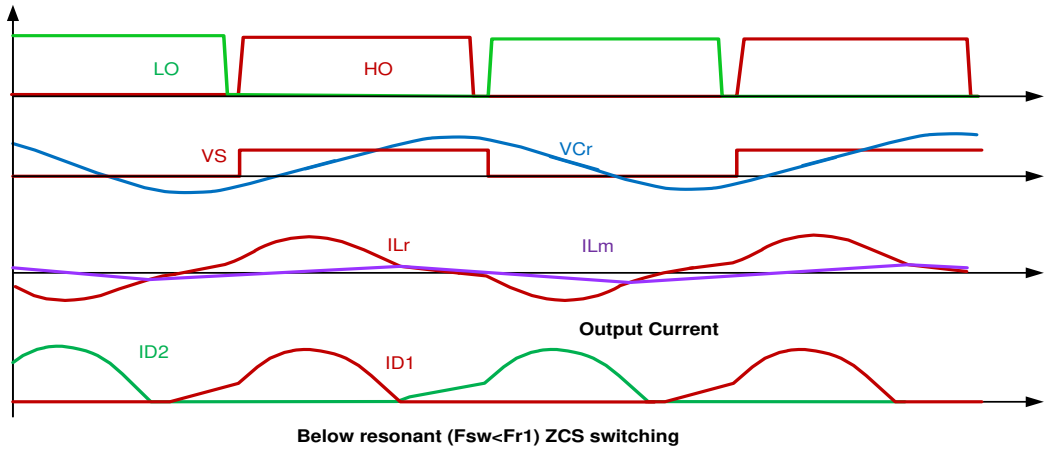


Figure 13: Typical waveform of below resonant ZCS switching

In ZCS mode, the two switching devices M1 and M2 are turned off under zero current condition. The turn-on of the two switches is hard switched (non-ZVS). The turn-on switching loss is high especially under high voltage bus voltage. The resonant capacitor C_r also has high voltage stress. ZCS operation should always be avoided.

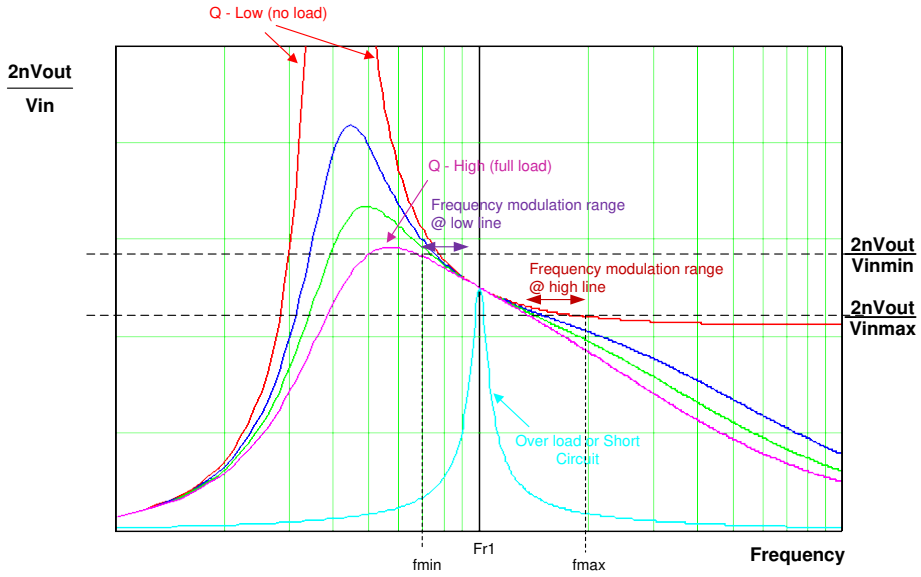


Figure 14: Typical voltage conversion ratio of a LLC resonant converter

With a regulated DC bus voltage supplied from the PFC stage the converter switching frequency can be adjusted to regulate the output voltage and current over the load range keeping the same conversion ratio over the family of curves with different Q. Given a fixed load the converter adjusts the switching frequency along the corresponding load line to regulate the output over input voltage range.

The procedure used to design the LLC resonant half-bridge converter uses the First Harmonic Approximation (FHA) to obtain an equivalent circuit model. All the components are moved to the primary side to simplify analysis. R_{ac} represents the equivalent load resistance in parallel with transformer primary inductance L_m.

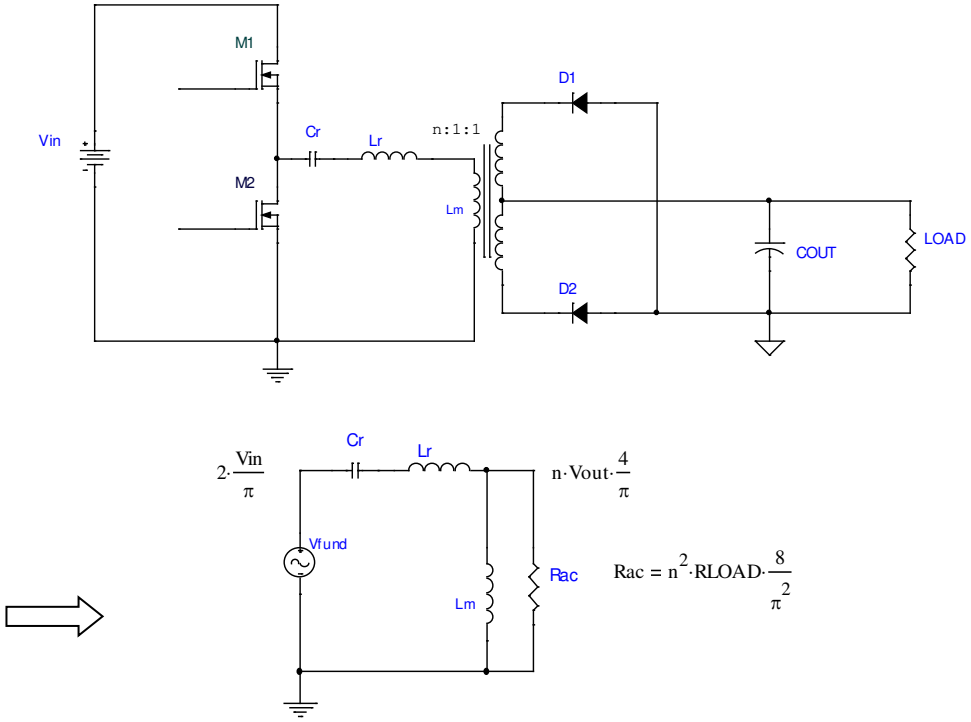


Figure 15: The FHA equivalent circuit

The input voltage of the resonant tank is a square wave with amplitude equal to the DC bus voltage Vbus. The fundamental component of the square waveform is:

$$\frac{2 \cdot Vbus}{\pi} \sin(\omega \cdot t)$$

The output voltage of the resonant tank is the voltage across L_m. It is very close to a square waveform with amplitude swinging from $-n \cdot Vout$ to $+n \cdot Vout$. So the fundamental component of the output square waveform is:

$$\frac{4 \cdot n \cdot Vout}{\pi} \sin(\omega \cdot t)$$

The power dissipation on the equivalent AC resistor is equal to the power dissipation of the load represented by a resistor R_{LOAD}, which can be derived by dividing the maximum output voltage by the output current, written as:

$$\frac{Vout^2}{R_{LOAD}} = \frac{\left(\frac{4 \cdot n \cdot Vout}{\sqrt{2}\pi}\right)^2}{Rac}$$

Re-arranging the formula gives the equivalent AC resistor:

$$Rac = \frac{8 \cdot n^2}{\pi^2} R_{LOAD}$$

The transfer ratio of the equivalent circuit can be obtained as following:

$$M = \left| \frac{\frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}}{j \cdot \omega \cdot Lr + \frac{1}{j \cdot \omega \cdot Cr} + \frac{j \cdot \omega \cdot Lm \cdot Rac}{j \cdot \omega \cdot Lm + Rac}} \right|$$

Simplifying to:

$$M = \left| \frac{1}{1 + \frac{Lr}{Lm} - \frac{1}{\omega^2 \cdot Lm \cdot Cr} + \frac{j\omega \cdot Lr}{Rac} - \frac{j}{\omega \cdot Cr \cdot Rac}} \right|$$

With the following definitions, calculation of M can be further simplified:

$$F_{r1} = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}, \qquad x = \frac{Fsw}{F_{r1}}, \qquad \varpi = 2\pi Fsw = 2\pi \cdot x \cdot F_{r1} = \frac{x}{\sqrt{L_r \cdot C_r}},$$

$$k = \frac{L_m}{L_r}, \qquad Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2}, \qquad Q = \frac{2\pi F_{r1} \cdot L_r}{Rac} = \frac{1}{2\pi F_{r1} \cdot C_r \cdot Rac}$$

$$M = \left| \frac{1}{1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right) + j \cdot Q \cdot \left(x - \frac{1}{x}\right)} \right|$$

Or,

$$M = \frac{1}{\sqrt{\left[1 + \frac{1}{k} \cdot \left(1 - \frac{1}{x^2}\right)\right]^2 + \left[Q \cdot \left(x - \frac{1}{x}\right)\right]^2}}$$

Per Figure 15, M is also equal to the output voltage to bus voltage ratio:

$$M = \frac{n \cdot Vout \cdot \frac{4}{\pi}}{2 \cdot \frac{Vbus}{\pi}} = \frac{Vout}{Vbus} \cdot 2 \cdot n$$

So the conversion ratio of output voltage Vout to bus voltage Vbus is:

$$\frac{Vout}{Vbus} = \frac{M}{2 \cdot n}$$

4. Transformer and Resonant Circuit Design

The system input data:

Parameter	Unit	Description	Value
$Vbus_{max}$	V	The maximum DC bus voltage	480
$Vbus_{min}$	V	The minimum DC bus voltage	440
$Vbus_{nom}$	V	The nominal DC bus voltage	460
Vout	V	The DC output voltage	48
Iout	A	The output load current	1.4
F_{r1}	kHz	The resonant frequency	60
Fmax	kHz	The maximum switching frequency	120
Dmax		The maximum duty-cycle	0.5
		Transformer core size	E32/16/9

Note: Typically Fmax < 2 x F_{r1} becuase the parasitic capacitance in the system introduces a third resonant frequency that could cause the output voltage to increase with switching frequency at no load if the maximum switching frequency is higher than the limit.

Step 1: Calculate the transformer turns ratio

$$n = \frac{Vbus(\max)}{2 \cdot Vout},$$

$$n = \frac{480}{2 \cdot 48} = 5$$

The transformer turns ratio is calculated with the maximum input voltage to make sure the output is always under regulation, including the worst case high-line voltage and no load condition.

Step 2: Choose k value

k is the ratio between the transformer magnetizing inductance and the resonant inductance. Smaller *k* value gives steeper gain curve, especially at the below resonant ZVS region as shown in figure 16. The output voltage is more sensitive to frequency variation with smaller *k* factor.

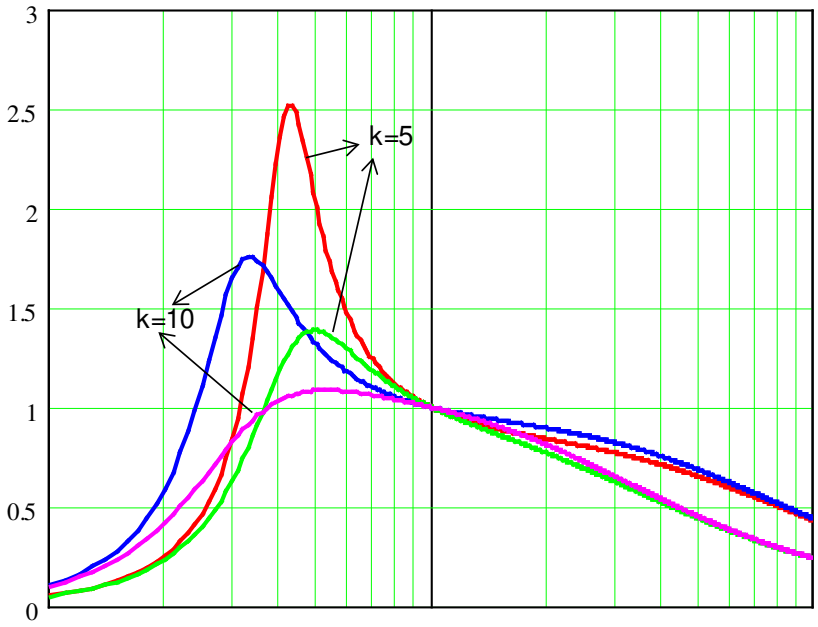


Figure16: k factor

A higher *k* value results in higher magnetizing inductance and thus lower magnetizing current in the transformer primary winding resulting in lower circulating power losses. However higher magnetic inductance could also cause non-ZVS switching at high line and zero load condition where the circulating current is too small to fully charge / discharge the VS node during dead-time.

The recommended range of k is from 3 to 10. In this case $k = 7$ is chosen.

Step 3: Calculate Qmax to maintain ZVS operation at the maximum load under the minimum input voltage

The input impedance of the equivalent resonant circuit (Figure 15) is given by:

$$Zin = j\cdot\omega\cdot Lr + \frac{1}{j\cdot\omega\cdot Cr} + \frac{j\cdot\omega\cdot Lm\cdot Rac}{j\cdot\omega\cdot Lm + Rac}$$

$$Zin = Q\cdot Rac\left|\frac{k^2\cdot x^2\cdot Q}{1 + k^2\cdot x^2\cdot Q^2} + j\left(x - \frac{1}{x} + \frac{x\cdot k}{1 + k^2\cdot x^2\cdot Q^2}\right)\right|$$

To keep the converter working in soft switching mode the operating point should remain in the ZVS region as shown in figure 10. The ZVS-ZCS boundary line is defined by the phase angle of Zin Φ(Zin)= 0 (the boundary condition between capacitive and inductive load), i.e. the imaginary part of Zin is zero. With this condition we can calculate the maximum Q which allows the converter to stay in ZVS. The maximum Q happens at the minimum input voltage and the maximum load.

$$Qmax = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}{Mmax^2-1}} = \frac{1}{k}\cdot\sqrt{\frac{1+k\cdot\left[1-\frac{1}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2}\right]}{\left(2\cdot n\cdot\frac{Vout}{Vinmin}\right)^2-1}}$$

Where *Mmax* is the maximum conversion ratio at the minimum input voltage,

$$Q\max = 0.523$$

Step 4: Calculate the minimum switching frequency

The minimum switching frequency occurs at the maximum load and minimum input voltage with the previous calculated maximum Qmax. As Qmax is defined by Im(Zin)=0,

$$\left(x-\frac{1}{x}+\frac{x\cdot k}{1+k^2\cdot x^2\cdot Qmax^2}\right)=0$$

The Fmin can be calculated with:

$$xmin = \frac{1}{\sqrt{1+k\cdot\left(1-\frac{1}{Mmax^2}\right)}} = \frac{1}{\sqrt{1+k\cdot\left[1-\frac{1}{\left(\frac{2n\cdot Vout}{Vinmin}\right)^2}\right]}}$$

$$x\min = 0.736$$

$$F\min = x\min\cdot F_{r1} = 44.2KHz$$

Step 5: Calculate L_r, C_r and L_m

As Qmax happens at the maximum load, so the resonant components L_r, C_r and L_m can be calculated per the Qmax value that had obtained in step 3:

$$R_{LOAD} = \frac{Vout}{Iout} = \frac{48V}{1.4A} = 34.3\Omega$$

$$Rac = \frac{8 \cdot n^2 \cdot R_{LOAD}}{\pi^2} = \frac{8 \times 5^2 \times 34.5}{\pi^2} = 699\Omega$$

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = \frac{0.523 \times 699}{2 \cdot \pi \cdot 44.2 \cdot 10^3} = 1.32mH$$

$$C_r = \frac{1}{2 \cdot \pi \cdot F_{r1} \cdot Q\max \cdot Rac} = \frac{1}{2 \cdot \pi \cdot 44.2 \cdot 10^3 \times 0.523 \times 699} = 9.85nF$$

Choose the nearest standard capacitor value for C_r, $C_r = 10nF$

Recalculate F_{r1} to keep the same Qmax with the selected C_r capacitor:

$$F_{r1} = \frac{1}{2 \cdot \pi \cdot C_r \cdot Q\max \cdot Rac} = 43.5kHz$$

Recalculate L_r with the selected C_r and F_{r1}:

$$L_r = \frac{Q\max \cdot Rac}{2 \cdot \pi \cdot F_{r1}} = 1.33mH$$

The actual L_r value should be lower than the calculated value to stay in ZVS region.
Now calculate L_m value based on L_r and the *k* factor that preset in step 2:

$$L_m = L_r \cdot k = 1.33 \times 7 = 9.31mH$$

Step 6: Calculate transformer primary and secondary turns

The standard half-bridge equation for the transformer turns number calculation is used here:

$$Np = \frac{Vin\min \cdot D\max}{2 \cdot \Delta B \cdot Ae \cdot F\min}$$

With $\Delta B = 0.2T$, $Ae = 0.83cm^2$ (ETD49), $F\min = 28kHz$, $Vin\min = 440V$, $D\max = 0.5$

$$Np = \frac{440 \times 0.5}{2 \times 0.2 \times 0.83 \times 28} \times 10 = 235$$

$$Ns = \frac{Np}{n} = \frac{235}{5} = 47$$

The transformer was designed to be capable of operating down to 28kHz to provide a safety margin although the minimum frequency is 43.5kHz in this design. Np was rounded to the nearest number divisible by n so that Ns would come out as a whole number.

Step 7: Calculate transformer primary and secondary current

In most LLC converter designs the minimum switching frequency is set below the resonant frequency Fr1 in order to maintain output voltage regulation at low line and full load. When the switching frequency is lower than the resonant frequency Fr1, the current waveform is shown as in figure 17.

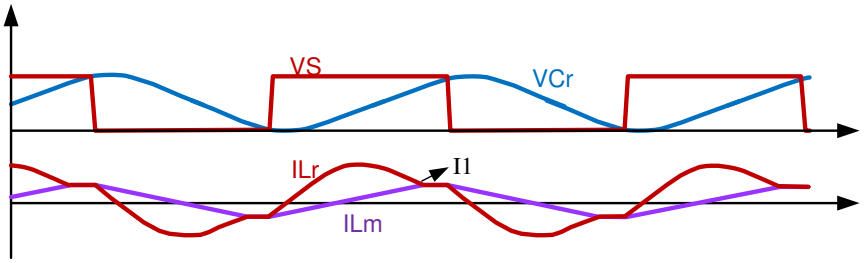


Figure17: Transformer primary current at full load and minimum input voltage

I1 is the current where the resonant current in L_r equals the magnetizing current in L_m. This is also the point where C_r and L_r cease to resonanate for the first half-period of F_{r1}. At this point, no more energy is delivered to the load and the output diodes are not conducting. C_r starts to resonate with L_r + L_m until the switching MOSFETs changes state. I1 can be calculated as:

$$I1 = \frac{n \cdot Vout}{2 \cdot Lm \cdot 2 \cdot Fr1} = 0.15A$$

The peak and RMS value of primary current can be estimated as:

$$Ipri(pk) = \sqrt{\left(\frac{Iout \cdot \pi}{2 \cdot n}\right)^2 + I1^2} = 0.47A$$

$$IpriRMS = \frac{Ipri(pk)}{\sqrt{2}} = 0.33A$$

The RMS current is calculated by assuming a purely sinusoidal current waveform. The actual primary RMS current is therefore higher than the calculated value.

The current in each secondary winding is very close to a half-sinusoid, thus the peak and RMS current can be estimated by:

$$Ispk = \frac{Iout \cdot \pi}{2} = 2.2A$$

$$Isrms = \frac{Iout \cdot \pi}{4} = 1.1A$$

The wire gauge of primary and secondary windings should be selected according to the calculated RMS current.

Step 8: Calculate resonant capacitor voltage

The C_r waveform is shown as in Figure 18:

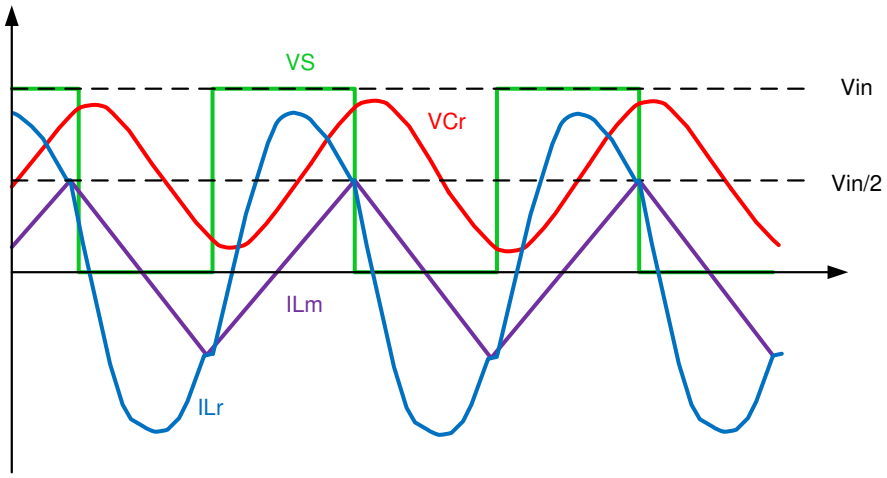


Figure 18: Typical resonant tank voltage and current waveforms

IL_m is the transformer primary magnetizing current, not including the current delivered to the secondary load through an ideal transformer in parallel with L_m. The difference between IL_r and IL_m is the output current.

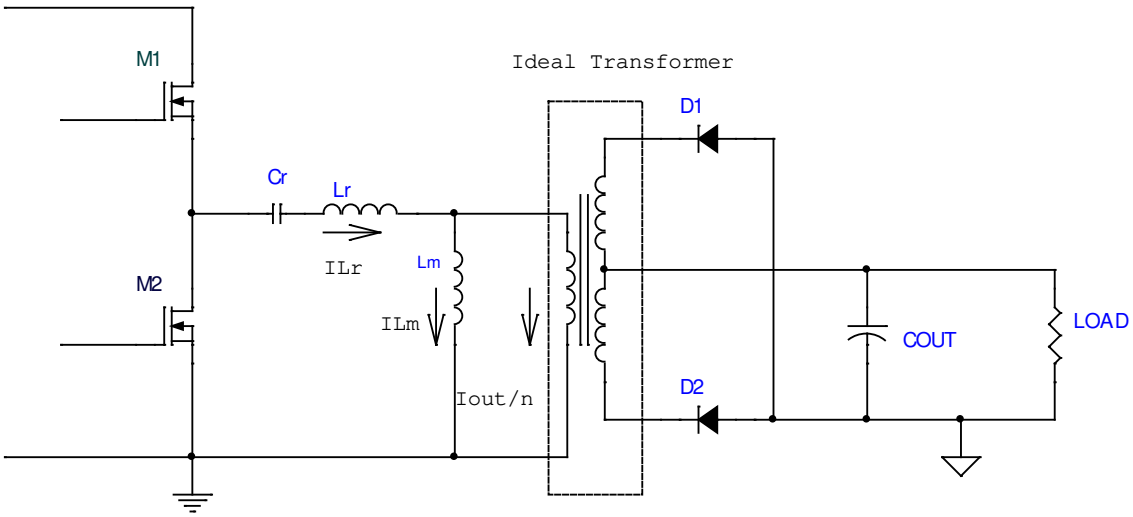


Figure 19: L_m and ideal transformer

The VC_r voltage reaches its peak when L_r current is crossing zero and it is at the mid-point of the input voltage when L_r current reaches its peak. The C_r voltage is at the maximum value when the VS node is at zero and is at the minimum value when the VS node is equal to Vin. VC_{rmin} and VC_{rmax} can be calculated as:

$$VC_{r\max} = n \cdot Vout + Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

$$VC_{r\min} = Vin - n \cdot Vout - Ipri(pk) \times \sqrt{\frac{L_r}{C_r}}$$

The peak to peak voltage ripple of VC_r is VC_{rmax}-VC_{rmin}:

$$VC_{rpk\_pk} = 2n \cdot Vout + 2 \cdot Ipri(pk) \times \sqrt{\frac{L_r}{C_r}} - Vin$$

It can be seen that the maximum peak-to-peak voltage occurs at the maximum load and the minimum DC input Vinmin, the switching frequency is at the minimum Fmin.

In this example:

$$Vcrpk\_pk = 2 \times 5 \times 48V + 2 \times 0.47A \times \sqrt{\frac{1.33mH}{10nF}} - 460V = 363V$$

The resonant capacitor C_r should be selected according to the capacitance value together with its voltage and current rating. A Polypropylene film capacitor should be used for minimum lower power loss. Polypropylene film capacitors are rated at DC voltage or 50Hz AC voltage with voltage de-rating at high frequency. The ability to withstand high frequency voltages is limited by thermal losses (power dissipation) and peak current capability. Even though the calculation result shows the maximum AC RMS voltage is 363V, a capacitor with higher voltage rating should be selected according to its frequency curve. Below is an example of EPCOS MKP capacitor B32612 (1000Vdc/250Vac).

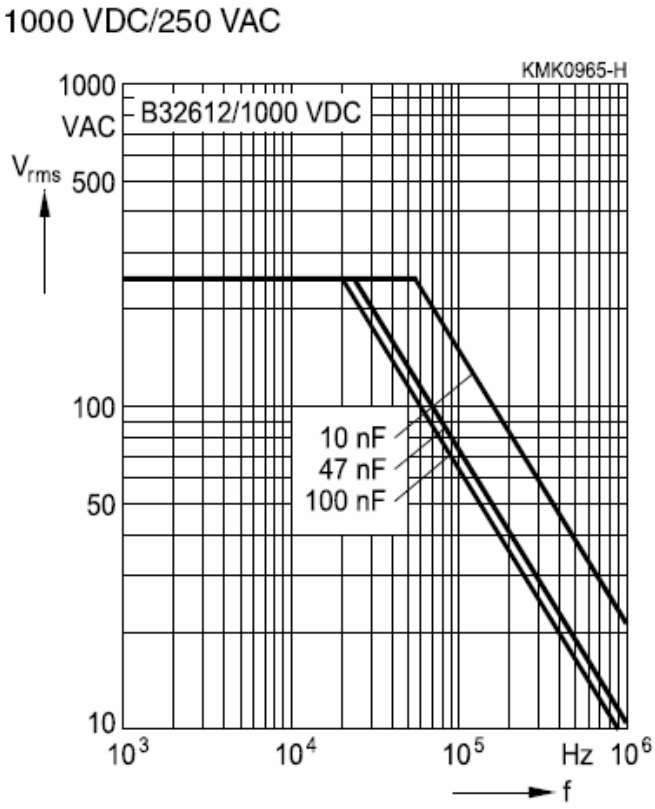
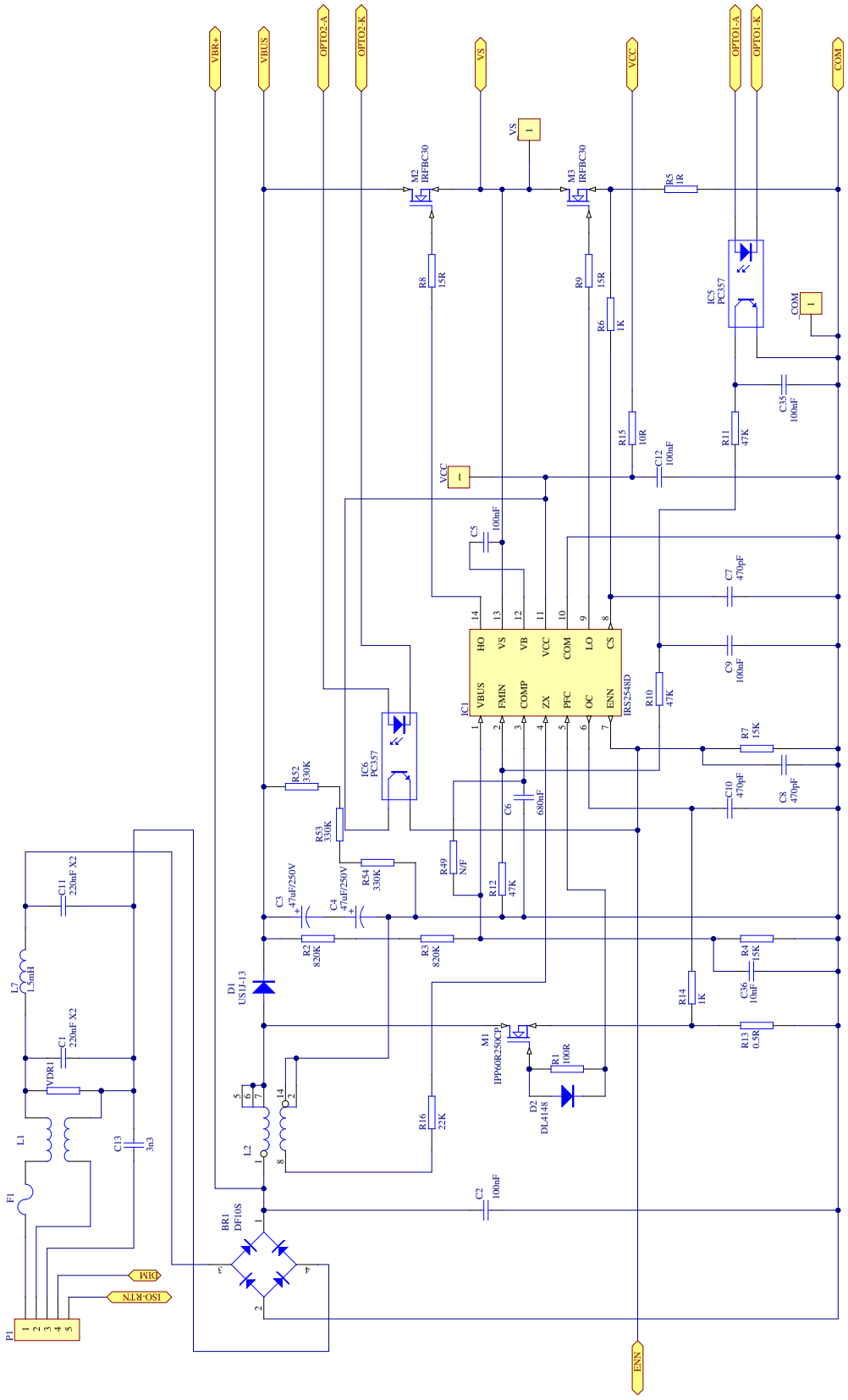
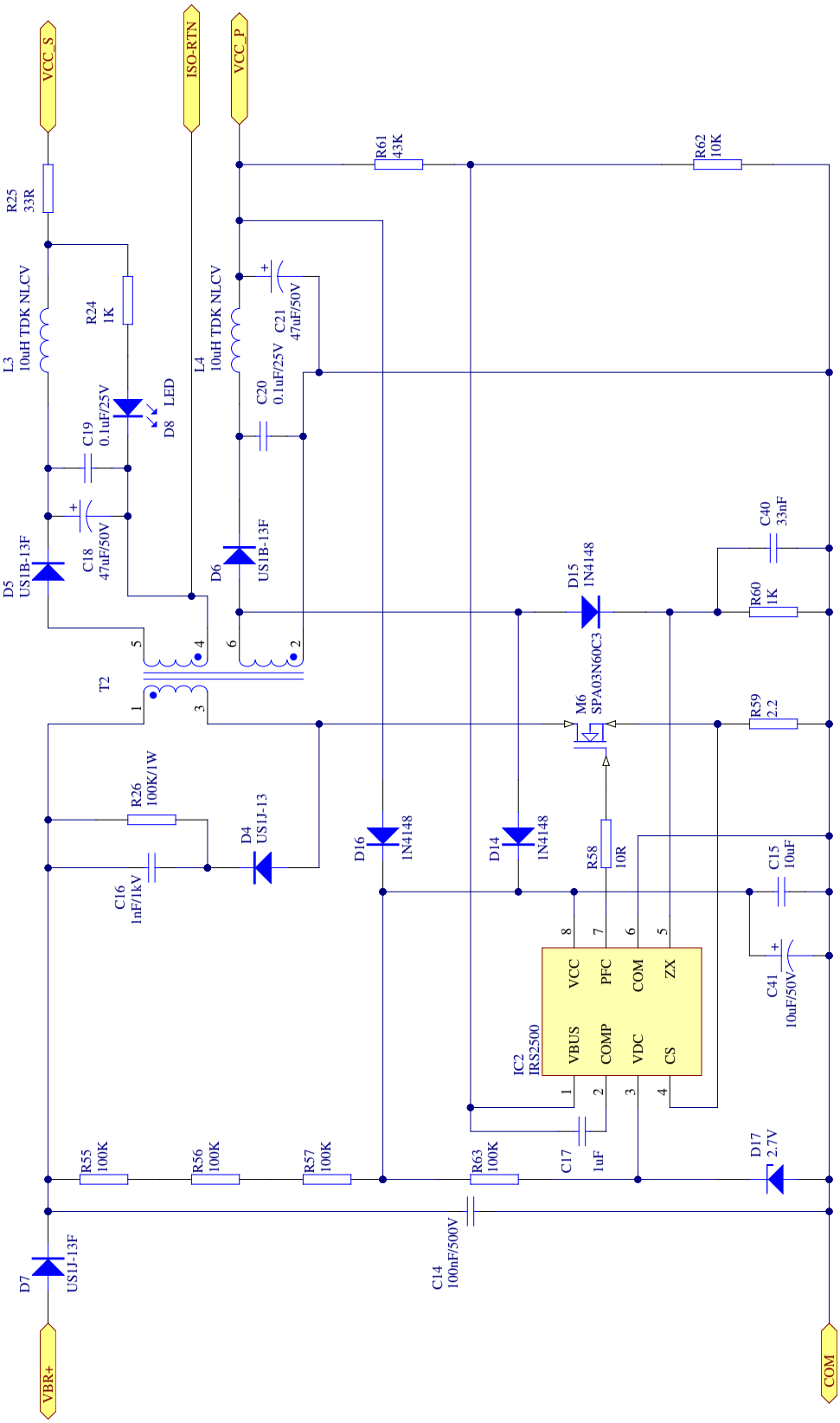


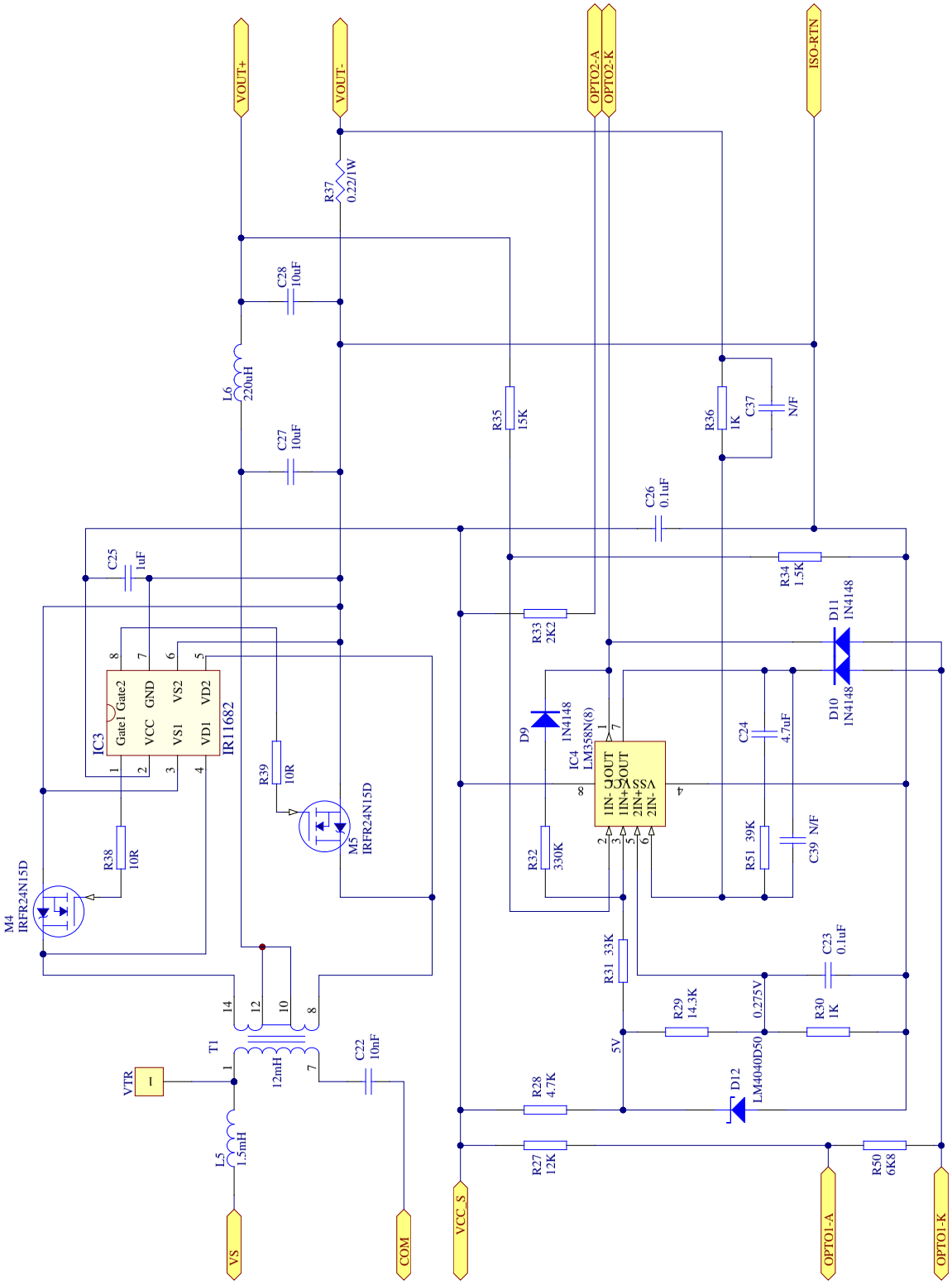
Figure 20: Vrms vs. frequency curve of MKP capacitor B32612 @ Ta<=90°C

In practice the transformer (T1) used on the IRPLLED5 board has a magnetizing inductance of 12mH and the series resonant inductor (L5) has a value of 1.5mH. This allows a low cost off the shelf inductor to be used for L5 while maintaining a similar ratio between Lm and Lr.

5. IRPLLED5 Board Schematics




VCC_S
ISO-RTN
VCC_P
R25 33R
L3 10uH TDK NLCV
R24 1K
D8 LED
C19 0.1uF/25V
C18 47uF/50V
D5 US1B-13F
L4 10uH TDK NLCV
C20 0.1uF/25V
C21 47uF/50V
D6 US1B-13F
R61 43K
R62 10K
C40 33nF
D15 1N4148
R60 1K
T2
M6 SPA03N60C3
R59 2.2
R26 100K/1W
D4 US1J-13
C16 1nF/1kV
D16 1N4148
D14 1N4148
R58 10R
C15 10uF
C41 10uF/50V
IC2 IRS2500
VCC
PFC
COM
ZX
VBUS
COMP
VDC
CS
R55 100K
R56 100K
R57 100K
R63 100K
C17 1uF
D17 2.7V
C14 100nF/500V
D7 US1J-13F
VBR+
COM


VOUT+
VOUT-
OPTO2-A
OPTO2-K
ISO-RTN
R37
0.22/1W
C28
10uF
L6
220uH
C27
10uF
R35
15K
R36
1K
C37
N/F
C26
0.1uF
C25
1uF
R34
1.5K
R33
2K2
D11
1N4148
D10
1N4148
D9
1N4148
IC3
IR11682
Gate2
GND
VS2
VD2
Gate1
VCC
VS1
VD1
R39
10R
M5
IRFR24N15D
IC4
LM358N(8)
1IN-
1OUT
1IN+
2OUT
2IN+
VSSA
2IN-
C24
4.7uF
R38
10R
M4
IRFR24N15D
R32
330K
R51
39K
C39
N/F
R31
33K
C23
0.1uF
R29
14.3K
0.275V
R30
1K
5V
T1
12mH
C22
10nF
VTR
D12
LM4040D50
R28
4.7K
L5
1.5mH
R27
12K
R50
6K8
VS
COM
VCC_S
OPTO1-A
OPTO1-K