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Application Note AN-1179

IRPLPFC1
90-265VAC PFC Pre-regulator

By Peter B. Green

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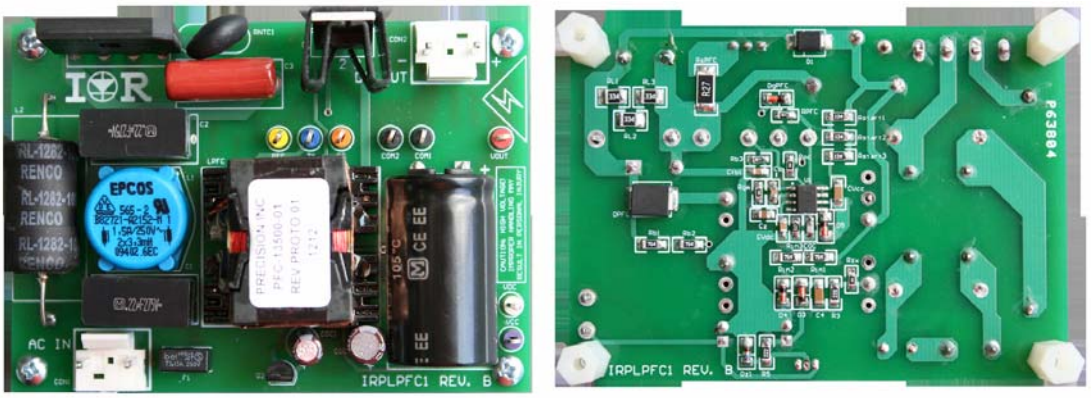
Safety Warning!

The IRPLPFC1 power factor correction pre-regulator is based on a non-isolated Boost SMPS circuit topology. The output is nominally 420VDC. When operating the output produces potentially dangerous voltages! Additionally short circuiting or overloading the output will damage the board. The IRPLPFC1 demo board should be handled by qualified electrical engineers only!

EVALUATION BOARD - IRPLPFC1



1. Introduction

Many offline applications require power factor correction circuitry in order to minimize transmission line losses and stress on electrical generators and transformers created by high harmonic content and phase shift. Electronic appliances often incorporate switching power supplies (SMPS) which include capacitive filter circuitry followed by a bridge rectifier and bulk capacitor supplying a load. Without power factor correction circuitry a SMPS draws a high peak current close to the line voltage peak and almost no current over much of the cycle, resulting in a power factor of around 0.5 with high total harmonic distortion.
Power factor correction circuitry can be added to enable the appliance to draw a sinusoidal current from the AC line with negligible phase shift and very low harmonic distortion. This represents the best type of load for the power transmission grid so that power can be supplied without creating additional conductive losses in transmission lines or additional burden on transformers and generators. Costs to electricity providers are therefore reduced, which passes savings on to the consumer. The trend towards more efficient power utilization for offline appliances, power supplies and lighting converters makes high power factor and low total harmonic distortion of the line input current (THDi) desirable.
Standards for power quality exist such as EN61000-3-2 in which specific current harmonic limits are detailed for various different applications. Compliance with class C limits is required for electronic lighting ballasts rated at 25W or above.
Market preferences often require LED converters and light fixtures to offer good performance at even lower power ratings.
For a product incorporating active power factor correction a THDi of less than 20% over a wide input voltage range, normally 100VAC to 305VAC is expected. In many cases THDi of less than 10% can be achieved over much or all of this voltage range.

Important Safety Information

The IRS2500 based PFC pre-regulator does not provide galvanic isolation of the output from the line input. Therefore if the system is supplied directly from a non-isolated input, an electrical shock hazard exists. The DC output voltage is high enough to produce a potentially lethal electrical shock therefore appropriate care should be taken when working on the IRPLPFC1 board.

It is recommended that for laboratory evaluation that the IRPLPFC1 board be used with an isolated AC or DC input supply. The IRS2500 series Boost topology is suitable only for front end applications where isolation is either not necessary or provided elsewhere in the system.

In addition since the IRPLPFC1 is a Boost converter there is no short circuit protection therefore care must be taken not to short circuit or overload the output.

2. Power Factor and THD

THD is defined as the RMS value of harmonic distortion from all components of an AC signal excluding the fundamental, expressed as a percentage of the RMS of the fundamental. In other words it quantifies the amount by which the signal deviates from a pure sinusoid;

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} An^2}}{A_1} = \frac{\sqrt{(A_{RMS} - A_1^2}}{A_1}$$

where A_1 is the RMS amplitude of the fundamental and A_{RMS} is the total RMS value of the complete current signal. THD of the current is often referred to as THDi to differentiate it from the voltage THD.

It should be noted that THDi is not the only quantity contributing to power factor (PF) reduction since phase shift between current and voltage inputs are not factored into the THD calculation. Power factor is defined as the ratio of the *real power*, which is utilized by the load, to the *apparent power* which also includes *reactive and distortion power*. Power factor (PF) includes *displacement* power factor resulting from phase displacement created by circuit reactances and *distortion* power factor created by harmonics.

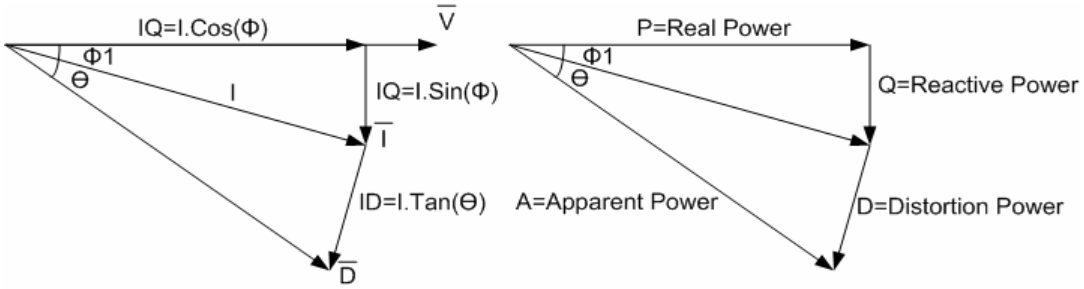


Figure 1. Power Vector Diagram

The general formula for power factor is:

$$PF = \frac{P_{RMS}}{V_{RMS} \cdot I_{RMS}}$$

where P_{RMS} is the real power consumed by the load.

The *displacement power factor* is given the formula:

$$DPF = COS(\phi)$$

where Φ is the phase shift between the voltage and sinusoidal current.

The following formula gives the *distortion power factor*:

$$DF = \frac{1}{\sqrt{1 + THD^2}}$$

The following formula combines these to give the total power factor:

$$PF = \frac{COS(\phi_1)}{\sqrt{1 + THD^2}}$$

where Φ_1 refers to the phase shift between the voltage and the fundamental component of the current and THD is expressed as a fraction.

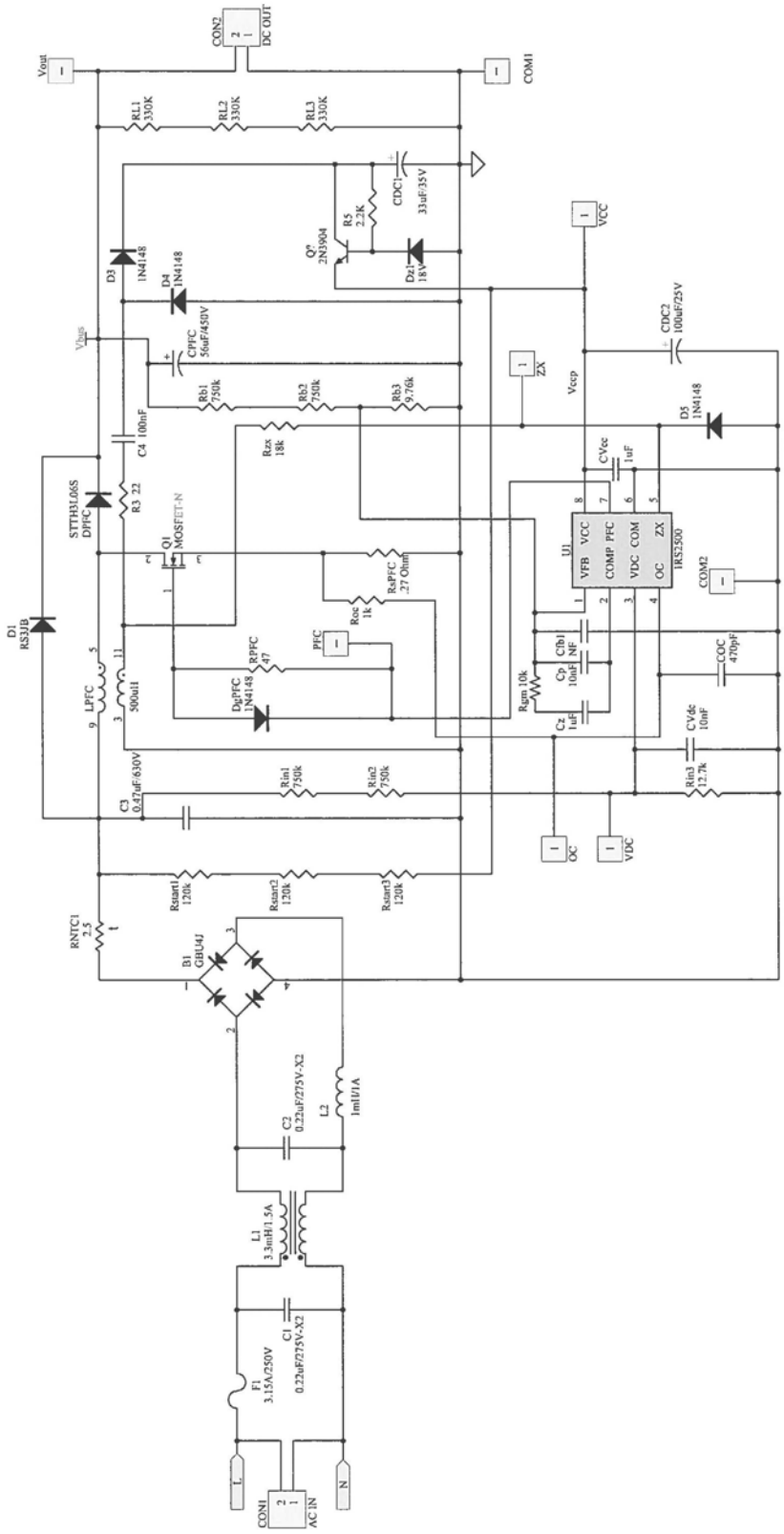


Figure 2: IRPLPFC1 Schematic

3. PFC Functional Description

Figure 2 shows the schematic for PFC pre-regulator based on a critical conduction mode Boost circuit. The IRS2500 pin out conforms to most industry standard power factor controllers and can be used as a drop in replacement for alternative parts in many applications and with minor modifications in many more. The IRPLPFC1 Boost PFC pre-regulator circuit consists of an EMI filter followed by a bridge rectifier which provides a full wave rectified voltage at the input to the Boost inductor LPFC. C3 provides an essential path for the circulating high frequency switching current. The EMI filter consisting of C1, L1, C2 and L2 provides reduction of common mode and series mode noise being conducted back onto the AC line. A series mode filter is necessary in PFC circuits operating in critical conduction mode since these produce higher current ripple than continuous mode systems. At power levels below 100W the benefits of critical conduction mode in the form of reduced switching losses outweigh the disadvantage of more filtering.
In critical conduction mode CrCM (also known as transition or boundary mode) the PWM gate drive signal to MPFC maintains a constant on time during the line cycle apart except where additional on time is added near the zero crossing. The off time varies during the AC line cycle. Each new switching cycle begins when the energy stored in LPFC has been fully transferred to the output therefore the off time varies during the AC line cycle becoming longer at the peak.

The on and off times not taking into account the additional on time modulation can be calculated by the following formulae:

$$T_{ON} = \frac{L.I_{L(pk)}}{\sqrt{2}.V_{in(rms)}}$$

$$T_{OFF} = \frac{L.I_{L(pk)}.\sin\theta}{V_{out} - \sqrt{2}.V_{in(rms)}.\sin\theta}$$

Where ILpk is the peak current in the inductor and Boost MOSFET Q1 at the peak of the AC line cycle and θ is the phase angle of the instantaneous AC line voltage, which varies over the cycle.

A feedback loop regulates the output voltage by adjusting the PWM on time. This takes place gradually over many line cycles so that the on time remains effectively constant over the period of a single line half cycle and therefore the input current follows the shape of the input voltage remaining sinusoidal.
When the MOSFET switch Q1 is turned on, the inductor LPFC is connected between the rectified line input (+) and (-) causing the current in LPFC to increase linearly. When Q1 is turned off, LPFC is connected between the rectified line input (+) and the DC bus capacitor CPFC through diode DPFC. The stored energy in LPFC is transferred to the output, supplying current into CPFC.

Q1 is turned on and off at frequencies ranging from 30kHz to several hundred kHz depending on the value of LPFC and the power throughput. The voltage at CPFC charges up to a specified level and the voltage feedback loop of the IRS2500 regulates the output by continuously monitoring the DC output and adjusting the on-time of MPFC as needed. If the output voltage is too high the on-time is decreased and if it is too low the on-time is increased. This negative feedback control loop operates with a slow loop speed relative to the AC line frequency and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage to obtain high power factor and low THD.

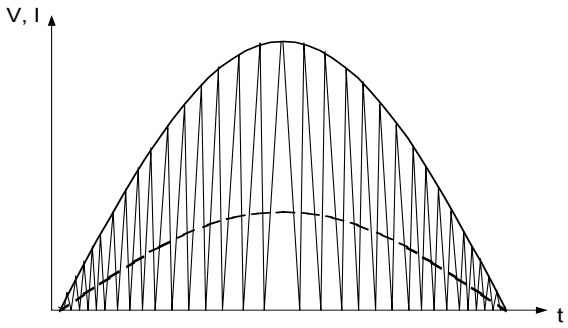


Figure 3: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage.

Adjustment of the output voltage can only occur over several line cycles. With a fixed on-time and an off-time determined by the inductor current discharging to zero, the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Figure 3) due to the much longer off time.
When the line input voltage is low (near the zero crossing) the inductor current will rise to a relatively low level so the discharge time will be short. When the input line voltage is high (near the peak), the inductor current will charge up to a much higher level and the discharge time will be longer.
The PFC control circuit of the IRS2500 U1 shown in the simplified schematic of figure 4, includes six control pins: VBUS, COMP, ZX, OUT, VDC and OC. The VBUS pin measures the DC bus voltage through an external resistor voltage divider. The error amplifier output appears at the COMP pin voltage, which determines the on-time and sets the feedback loop response speed with an external RC integrator or other compensation network. The ZX pin detects when the inductor current discharges to zero each switching cycle using a secondary winding from the PFC inductor. The OUT pin is the low-side gate driver output for the external MOSFET. The VDC pin senses the line input cycle providing phase information to control the on time modulation described in the next section. The OC pin senses the current flowing through MPFC and performs cycle-by-cycle over-current protection.

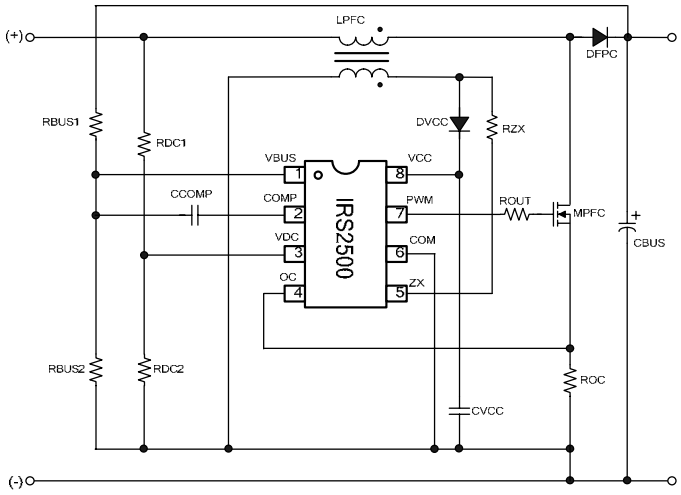


Figure 4: IRS2500 simplified PFC control circuit.

The VBUS pin is compared with a precision internal 2.5V reference voltage for regulating the DC output voltage. The feedback loop error amplifier increases or decreases the COMP pin voltage. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor shown in Figure 5 and therefore determines the on-time.

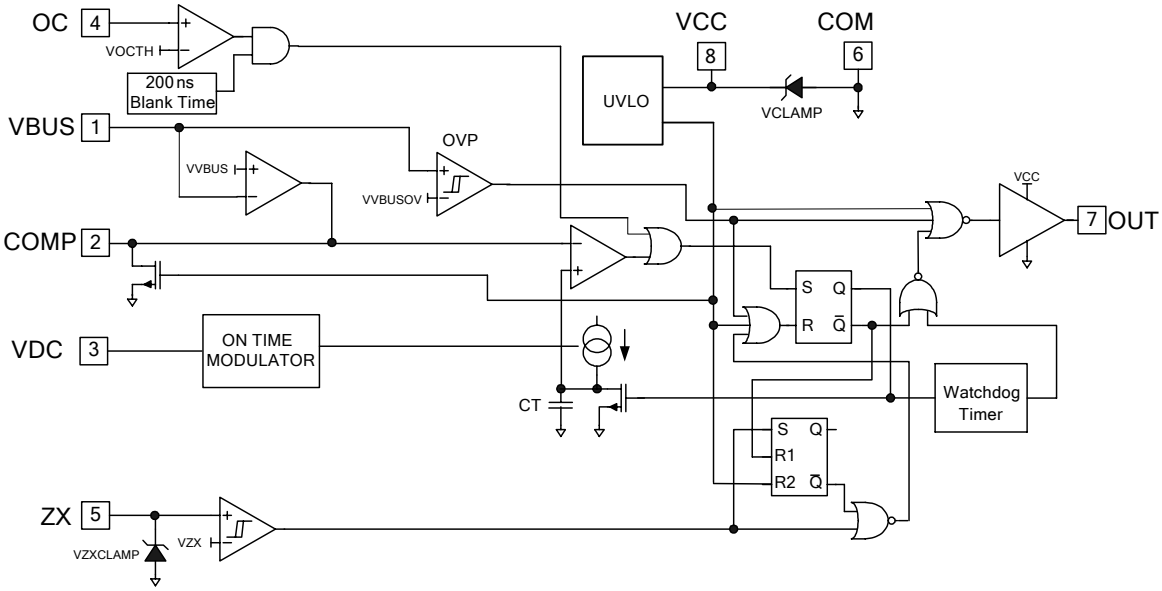


Figure 5: IRS2500 Internal Block Diagram.

The off-time is determined by the time it takes the LPFC current to discharge to zero. The zero current level is detected by a secondary winding on LPFC that is

connected to the ZX pin through an external current limiting resistor RZX. This winding typically has a 1:10 turns ratio relative to the main winding. A positive-going edge exceeding the internal threshold VZX+ signals the beginning of the off-time. A negative-going edge on the ZX pin falling below VZX- occurs when the LPFC current discharges to zero signaling the end of the off-time when the gate drive output OUT transitions high again (Figure 12). The ZX pin is internally biased to 1V so that a positive current must be supplied to the ZX input to set the ZX detector and a negative current must be supplied to indicate all of the energy has been discharged and the winding voltage polarity has reversed. A wide hysteresis prevents false triggering by ringing oscillations.

The cycle repeats indefinitely until the IRS2500 is disabled through an over-voltage condition on the DC bus or if the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, the gate drive output will remain off until the watch-dog timer forces a re-start. The watch-dog pulses occur every 300-400us (tW) indefinitely until a correct positive and negative-going signal is detected at the ZX pin and normal operation is resumed. Should the OC pin voltage exceed the VOCTH over-current threshold during the on-time the gate drive output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the output on again.

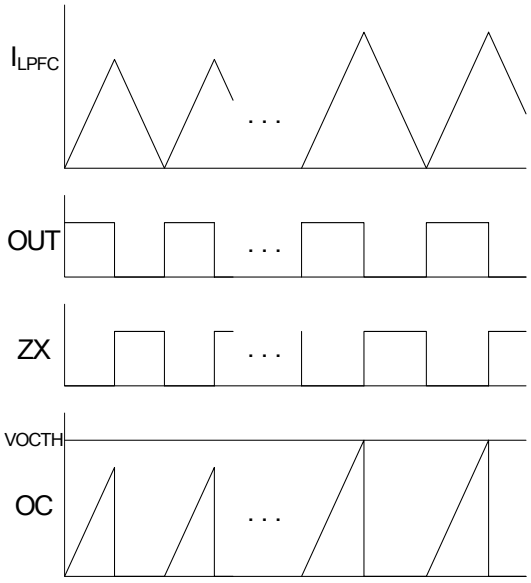


Figure 6: Inductor current, OUT pin, ZX pin and OC pin timing diagram.

A fixed on-time over an entire cycle of the line input voltage produces a peak inductor current that naturally follows the sinusoidal shape of the line input voltage. The smoothed, averaged line input current is in phase with the line input voltage for high power factor but some harmonic distortion of the current

remains. This is due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve lower harmonics that are acceptable for compliance with international standards and general market requirements, an additional on-time modulation circuit has been added to the PFC control. This IRS2500 dynamically increases the on-time as the line input voltage nears the zero-crossings (Figure 7). This causes the peak LPFC current, and therefore the smoothed line input current, to increase near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the current THD.

On time modulation is controlled by sensing the full wave rectified voltage at the bridge rectifier output through a resistor divider (RDC1, RDC2 in figure 4). This is scaled such that the peak voltage will be close to 1V at 120VAC and 3V at 265VAC. This function can be disabled if necessary by connecting a 10K resistor from pin 3 to VCC in place of the input signal.

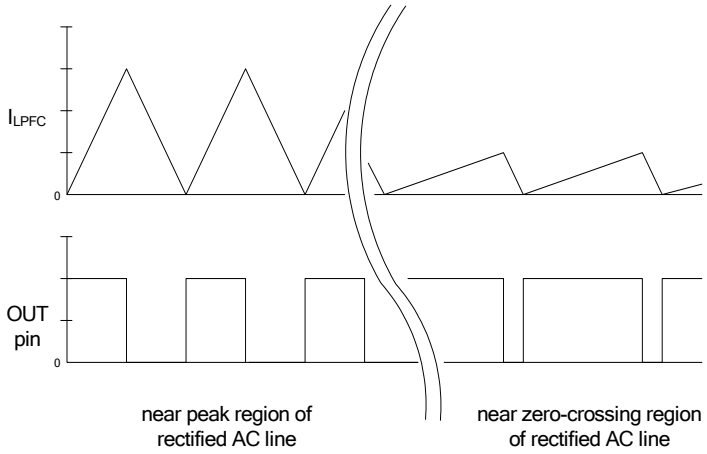


Figure 7: On-time modulation circuit timing diagram.

The IRS2500 incorporates both static and dynamic overvoltage protection. Static over voltage protection monitors the feedback voltage at the VBUS pin and disables the gate drive output if this voltage exceeds the target voltage by 8%. This is activated by an internal comparator set to detect a threshold of 2.7V, which is 8% above the regulation threshold of 2.5V.

However, under startup condition or when a load is removed from the output the error amplifier output voltage at the COMP pin swings low. Since the compensation capacitor CCOMP is connected from this output back to the VBUS input a current will flow during the COMP voltage transition. This pulls down the VBUS voltage, which allows the output voltage to exceed the desired regulation level during the transition and results in an overshoot before the voltage at the VBUS input exceeds the regulation threshold.

In order to compensate for this effect, the IRS2500 includes dynamic detection of the error amplifier output current. During a swing in the negative direction the

error amplifier output sink current peaks at a much high level than during steady state operation. This current surge is internally detected to trigger the overvoltage protection circuitry disabling the PWM output until the error amplifier output has settled to a new level. This prevents the output voltage from overshooting the desired level by a significant amount under the transient conditions described. For this reason the loop should be designed such that voltage ripple at COMP is minimized during steady state operation to avoid false tripping of the dynamic overvoltage protection.

The IRPLPFC1 board provides the VCC supply to IC1 by means of a charge pump supplied from the auxiliary winding consisting of R3,C4,D3 and D4. The initial startup voltage is supplied through Rstart1,Rstart2 and Rstart3. Since CDC1 and CDC2 are quite large there is a delay at switch on before the VCC voltage comes up and the PFC circuit begins to operate. This delay can be several seconds at low line voltages. In an application the VCC supply can be derived from various different means and the startup delay can also be reduced.

Q2, R5 and Dz1 form a regulator to limit the VCC voltage since the voltage from the auxiliary winding varies considerably with VAC.

4. Design Equations

Step 1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad \text{[Henries]}$$

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum RMS AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = Output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad \text{[Amps Peak]}$$

Note: The PFC inductor must not saturate at i_{PK} over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

Referring to the designators in figure 4:

Step 3: Calculate PFC over-current resistor ROC value:

$$R_{OC} = \frac{VOCTH}{i_{PK}}$$ where VOCTH = 1.1V [Ohms]

ROC power rating can be approximated:

$$PR_{OC} \geq \left(\frac{P_{OUT}}{VAC_{MIN} . \eta} \right)^2 \times R_{OC}$$ [Watts]

Step 4: Calculate start-up resistor RVCC value:

$$R_{VCC} < \frac{VAC_{MIN}}{IQCCUV}$$ [Ohms]

$$PRV_{CC} > \frac{V_{ACMAX}^2}{R_{VCC}}$$ [Watts]

RVCC is often comprised of several series resistors (Rstart1, Rstart2 and Rstart3 in the IRPLPFC1 circuit) in order to withstand the high voltage.

Step 5: Calculate VBUS feedback resistor divider network:

RBUS1 is often comprised of two series resistors (RBUS1A and RBUS1B in figure 4, Rb1 and Rb2 in the IRPLPFC1 circuit) in order to withstand the high voltage.

Select an initial value of 10K for RBUS2 (Rb3 in the IRPLPFC1 circuit)

$$R_{BUS1} = (V_{BUS} - 2.5) \times \frac{10000}{2.5}$$ [Ohms]

$$R_{BUS1A} = R_{BUS1B} = \frac{R_{BUS1}}{2}$$ [Ohms]

Choose the nearest preferred value for RBUS1A and RBUS1B.
Then re-calculate RBUS2:

$$R_{BUS2} = \frac{2.5 \times (R_{BUS1A} + R_{BUS1B})}{V_{BUS} - 2.5}$$ [Ohms]

Then choose the nearest E96 1% tolerance value for RBUS2.

Step 6: Calculate VDC resistor divider network:

RDC1 is often comprised of two series resistors (RDC1A and RDC1B in figure 4, Rin1 and Rin2 in the IRPLPFC1 circuit) in order to withstand the high voltage.

Select an initial value of 10K for RDC2 (Rin3 in the IRPLPFC1 circuit)

$$R_{DC1} = (\sqrt{2}.V_{ACMIN} - 1) \times 10000 \quad \text{[Ohms]}$$

Choose the nearest preferred value for RDC1A and RDC1B.

Then re-calculate RDC2:

$$R_{DC2} = \frac{R_{DC1A} + R_{DC1B}}{\sqrt{2}.V_{ACMIN} - 1} \quad \text{[Ohms]}$$

Then choose the nearest E96 1% tolerance value for RDC2.

Step 7: Calculate COMP capacitor:

CCOMP should be selected to roll off the gain of the error amplifier at approximately 20Hz.

$$C_{COMP} = \frac{1}{2\pi \times 20Hz \times R_{BUS2}} \quad \text{[Farads]}$$

Choose the nearest preferred value for CCOMP shown in figure 4.

A simple integrator network is normally sufficient for compensation in most PFC pre-regulators. For added flexibility the IRPLPFC1 board includes a single pole at 16Hz and a single zero at 1600Hz. This allows the gain to remain flat between these two frequencies. This gain is determined by the value of Rgm. Replacing Rgm with a zero Ohm resistor will convert the circuit to a simple integrator that crosses zero gain at 16Hz.

Step 8: Calculate RZX resistor:

Choose Izx as 0.5mA and assume ZX winding maximum voltage VZX of 20V at the ZX winding as an approximation. If the actual VZX is higher than 20V use the true value.

$$R_{ZX} \leq \frac{V_{ZX}}{I_{ZX}} \quad \text{[Ohms]}$$

Choose the next lowest preferred resistor value for RZX.

5. Factors affecting PF and THD

The PFC pre-regulator circuit described above draws a current from the line input which follows the shape of the voltage, however the following points should be considered when optimizing circuit performance:

1. Phase shift produced by filter capacitors.
The capacitors C1 and C2 used in the EMC filter draw AC current from the line input, which leads the voltage by 90º. The magnitude of this reactive current is dependent on the capacitor values and the AC line input voltage. This is one reason why the power factor always drops as line input voltage increases. For this reason these values should be kept as small as possible while making sure the input filter is adequate for EMC compliance.

2. Phase shift produced by the bridge capacitor.
The bridge capacitor C3 also causes some phase shift since the voltage across it is full wave rectified.
This should also be kept to a minimum though it must be sufficient to provide a high frequency AC current source for the switching regulator. The value of C3 also affects EMI.

3. Cross over distortion produced by the bridge capacitor.
C3 also contributes to cross over distortion while C1 and C2 do not. The circuit can be considered as a resistive load and therefore it is clear that as the AC line input voltage passes through each zero crossing, C3 needs to discharge through the load. Depending on the storage capacity of C3 and the load, the voltage on C3 never discharges completely to zero at each zero crossing always maintaining a residual voltage. This problem becomes worse in systems where the load is variable such as a dimmable electronic lighting ballast. As the load is reduced the residual voltage on C3 increases. Since this voltage does not reach zero, when the AC line input voltage drops below the minimum voltage at C3 there is no current drawn from the line input resulting in the characteristic crossover distortion dead band shown on the input current waveform in figure 8.
It should be noted that the two diode drops in the bridge rectifier B1 also contribute to cross over distortion to a small extent.
Crossover distortion can never be completely eliminated for these reasons, however by choosing the value of C3 to provide the best tradeoff and by the on time modulation provided by the IRS2500, this can be minimized.

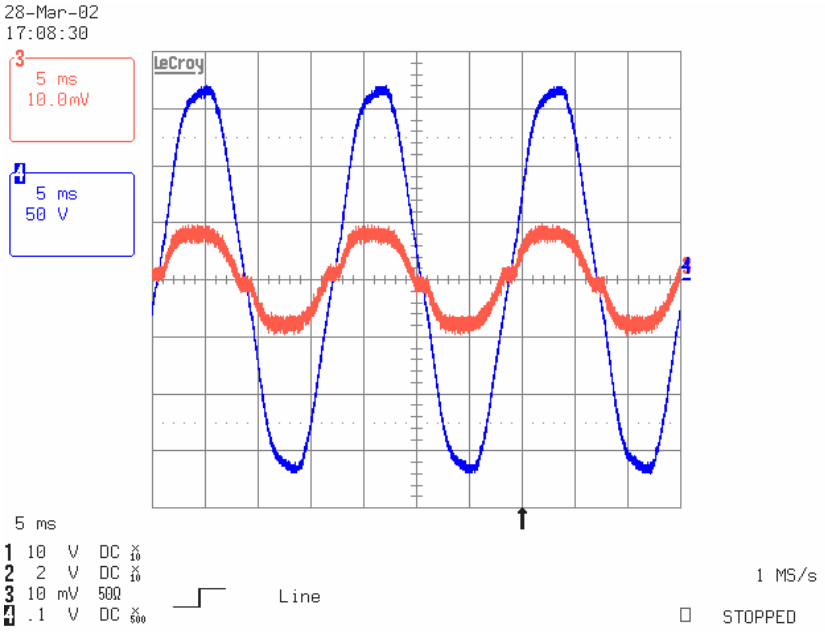


Figure 8: Line input and current in a typical PFC pre-regulator

4. Minimal energy transfer at the zero crossing.
At low line input voltage levels there may be insufficient energy stored in the Boost inductor LPFC to provide enough voltage at the drain of MPFC to forward bias the output diode DPFC. This is due to parasitic capacitances in the windings of LPFC as well as the drain to source capacitance of the MOSFET switch. This being the case it is necessary for the control IC to compensate for this by increasing the MOSFET on time when the voltage approaches zero in order to draw more current. This on time modulation has already been described. The line input voltage is generally detected through the divided input signal provided at pin 3 (VDC). It should be noted here that the residual voltage across C3 will be also be divided down through Rin1, Rin2 and Rin3 so that it also appears at pin 3, which prevents the IC from detecting the input voltage below the level of the residual voltage. In order to limit this problem, the IRS2500 is designed to produce sufficient on time modulation to discharge C3 as close to zero as possible and introduce this modulation before the residual voltage level is reached.

5. Ripple at the error amplifier output (COMP)
The output bus voltage from the PFC pre-regulator circuit will always contain some ripple at twice the line frequency (ΔV_{OUT}) superimposed on top of the regulated DC output. The magnitude of ΔV_{OUT} depends on the magnitude of the output storage capacitor CBUS. Since the output voltage is divided and fed back to the inverting input of the error amplifier, a component of ripple will also be fed to the input and compared with the internal 2.5V reference of the IRS2500. This may result in a component of ripple appearing at the error amplifier output

(COMP) which determines the PWM on time. It is necessary for the compensation capacitor CZ to be large enough to roll off the error amplifier gain at a frequency well below twice the line frequency in order to reduce this ripple to a very small level. Ripple at the COMP output results in modulation of the on time causing distortion of the current waveform and should therefore be eliminated as far as possible without slowing down the loop response too much.

6. Delay before next switching cycle

In critical conduction mode an auxiliary wining on the Boost inductor provides a signal to the ZX (zero crossing) pin of the controller to signal when the energy from the inductor has been fully transferred to the output by transitioning from high to low. When this transition is detected the PWM output drive goes high to start the next cycle, however if there is delay then the converter is actually operating in discontinuous mode due to the delay. This can cause some distortions in the current waveform. Delay is minimized in the IRS2500. Capacitors should not be added at the ZX pin.

6. PCB Layout Considerations

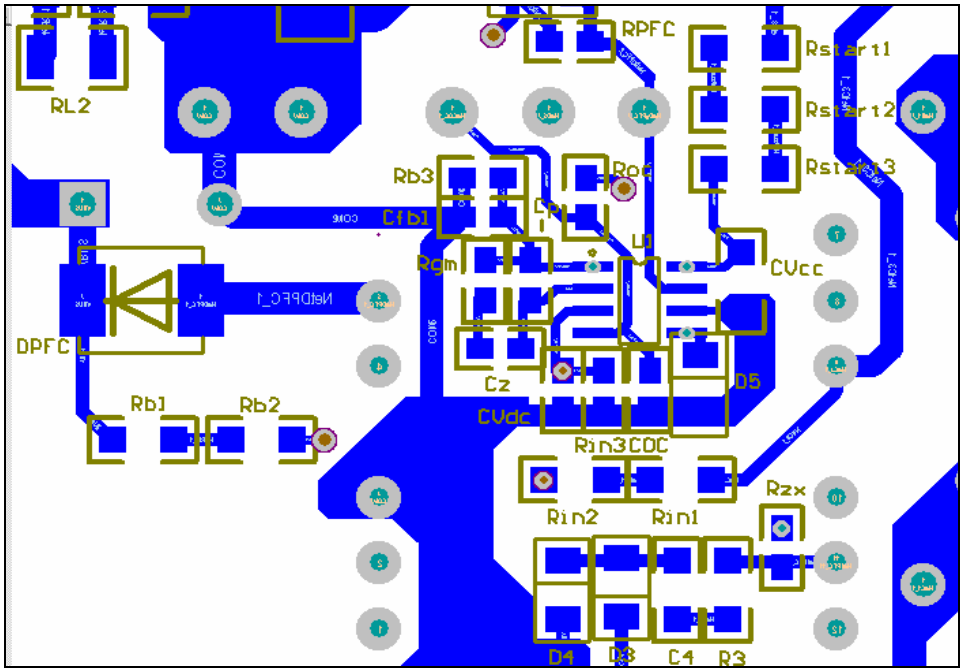


Figure 9: IRPLPFC1 PCB Bottom Layer

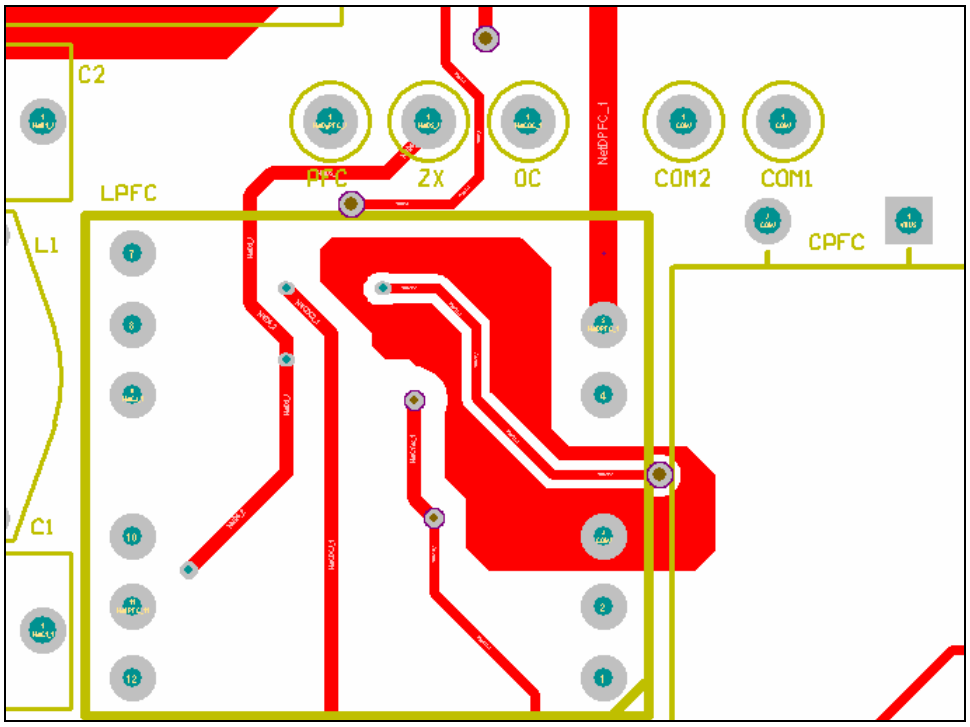


Figure 10: IRPLPFC1 PCB Top Layer

For correct operation of the IRS2500, the PCB has been designed to avoid noise coupling to the control inputs and ground loops according to the layout recommendations listed in the IRS2500 datasheet:

1. As a general rule the circuit signal and power grounds should be separated and joined together at one point only. The signal ground should be a star point located close to the COM pin of the IRS2500.
2. A noise decoupling capacitor CVCC is located between the VCC and COM pins of the IRS2500 located as close to the IC as possible.
3. All traces to the VBUS input have been kept as short as possible. This means that resistors and capacitors that are connected to this input (Rb2,Rb3,Cp and Rgm) are be located as close to the IRS2500 as possible. The voltage feedback divider resistor (Rb3) connected to COM is be connected to a signal ground close to the COM pin.
4. Traces carrying high voltage switching signals such as those connected to the MOSFET drain or gate drive signals are not be located close to traces connected directly to the VBUS input.
5. The divider network resistor (Rin2 and Rin3) and filter capacitor (CVdc) connected to the VDC input of the IRS2500 are located as closely to the IC as possible with the grounded end connected to the circuit signal ground.
6. The over current detection filter resistor (ROC) and capacitor (COC) should be located as close to the IRS2500 as possible with COC connected to the circuit signal ground.

7. The zero crossing detection resistor Rzx is located close to the IRS2500 if possible to prevent possible noise appearing at this input.

Figure 9 and 10 show the IRPLPFC1 PCB layout where the IRS2500 is located on the bottom side of the PCB. The bottom side traces are shown in blue and the top side traces in red. The circuit power ground can be seen at the CPFC negative (COM1,COM2) node with the signal ground located around IC1 from Rb3 to CVdc which is connected to Rin3, COC and CVCC and to pin 6 (COM) of IC1 (D5 is not fitted). The signal ground traces from IC1 pin 6 also connect to the LPFC ground pin and VCC capacitors CDC1 and CDC2. A ground plane on the top copper layer also connects to the signal ground although this is not essential. The power ground begins at the junction of CBUS and the shunt resistor RsPFC which carries the high current from the switching MOSFET Q1 and the output return current back to the AC line through the bridge B1. C3 is connected between the power ground and rectified DC voltage from B1.

7. Bill of Materials

Item	Description	Part Number	Manufacturer	Quantity	Reference
1	IC, PFC Controller	IRS2500S	International Rectifier	1	IC1
2	Bridge Rectifier, 600V, 4A	GBU4J	Micro Commercial	1	B1
3	Diode, 600V, 3A, Fast recovery	STTH3L06S	STMicro	1	DPFC
4	Diode, 600V, 3A, Fast recovery	RS3JB-13-F	Diodes Inc	1	D1
5	Diode, 75V, 0.15A, SOD-80	DL4148-TP	Micro Commercial	4	D3,D4,D5 ,DgPFC
6	Diode, Zener 18V, 500mW, SOD-80	FLZ18VC	Fairchild	1	Dz1
7	MOSFET, 650V, 0.25 Ohm, TO-220	IPP60R250CP	Infineon	1	Q1
8	Transistor, NPN, 40V, 200mA, TO-92	2N3904TF	Fairchild	1	Q2
9	Capacitor, 220nF, 275VAC, Radial 0.6"	ECQ-U2A224ML	Panasonic-ECG	2	C1,C2
10	Capacitor, 470nF, 400V, Radial 0.6"	QXK2G474KTP	Nichicon	1	C3
11	Capacitor, 0.1uF, 50V, 10%, 1206	C3216X7R1H104K	TDK	1	C4
12	Capacitor, 33uF, 35V, Electrolytic Radial, 105C	EKZE350ELL300ME11D	United Chemi-Con	1	CDC1
13	Capacitor, 100uF, 25V, Electrolytic Radial, 105C	EKZE250ELL101MF11D	United Chemi-Con	1	CDC2
14	Capacitor, 1uF, 25V, 10%, 1206	C3216X7R1E105K	TDK	1	CVCC1
15	Capacitor, 1nF, 50V, 10%, 0805	C2012X7R1H102K	TDK	1	CFB1
16	Capacitor, 470pF, 100V, 5%, 0805	C2012COG2A471J	TDK	1	COC
17	Capacitor, 1uF, 25V, 10%, 0805	C2012X7R1E105K	TDK	1	CZ
18	Capacitor, 10nF, 50V, 10%, 0805	C2012X7R1H103K	TDK	2	CP,CVDC
19	Capacitor, 56uF, 450V, Electrolytic Radial, 105C	EEU-EE2W560	Panasonic-ECG	1	CPFC
20	Inductor, 3.3mH, 1.5A, common mode	B82721A2152N1	Epcos	1	L1
21	Inductor, 1mH, 1A, Axial	RL-1282-1000	Renco	1	L2
22	Inductor, 500uH	PFC-13500-01	Precision Inc	1	LPFC
23	Resistor, 22Ohm, 0.25W, 5%, 1206	ERJ-8GEYJ220V	Panasonic-ECG	1	R3

24	Resistor, 2.2kOhm, 0.25W, 5%, 1206	ERJ-8GEYJ222V	Panasonic-ECG	1	R5
25	Resistor, 750kOhm, 0.25W, 5%, 1206	ERJ-8GEYJ754V	Panasonic-ECG	4	RB1,RB2, RIN1,RIN 2
26	Resistor, 8.87kOhm, 0.125W,5%, 0805	RC0805FR-078K87L	Yageo	1	RB3
27	Resistor, 10kOhm, 0.125W, 5%, 0805	ERJ-6GEYJ103V	Panasonic-ECG	1	RGM
28	Resistor, 12.7kOhm, 0.125W, 5%, 0805	RC0805FR-0712K7L	Yageo	1	RIN3
29	Resistor, 330kOhm, 0.5W, 5%, 1210	ERJ-14YJ334U	Panasonic-ECG	3	RL1,RL2, RL3
30	Resistor, 1KOhm, 0.125W, 5%, 0805	ERJ-6GEYJ102V	Panasonic-ECG	1	ROC
31	Resistor, 47Ohm, 0.125W, 5%, 0805	ERJ-6GEYJ470V	Panasonic-ECG	1	RPFC1
32	Resistor, 0.27Ohm, 1W, 1%, 2512	ERJ-1TRQJR27U	Panasonic-ECG	1	RSPFC
33	Resistor, 120kOhm, 0.25W, 5%, 1206	ERJ-8GEYJ124V	Panasonic-ECG	3	Rstart1,R start2,RSt art3
34	Resistor, 18KOhm, 0.25W, 5%, 0805	ERJ-6GEY183V	Panasonic-ECG	1	RZX
35	Resistor, NTC, 2.5Ohm	B57236S0259L002	Epcos	1	RNTC2
36	Test point, 0.063"D Orange	5008	Keystone	1	VCC
37	Test point, 0.063"D White	5007	Keystone	1	ZX
38	Test point, 0.063"D Yellow	5009	Keystone	1	PFC
39	Test point, 0.063"D Red	5005	Keystone	1	VOUT
40	Test point, 0.063"D Black	5006	Keystone	2	COM,CO M2
41	Test point, 0.063"D Purple	5124	Keystone	1	OC
42	Test point, 0.063"D Blue	5122	Keystone	1	VDC
43	Header, 3 position, 0.156" vertical	26-60-4030	Molex	2	CON1,CO N3
44	Fuse, 3.15A/250VRadial	RST 3.15	Bel Fuse Inc	1	F1
45	PCB	IRPLPFC1 Rev A		1	
46	Standoff, HEX 0.65"L 4-40THR Nylon	1902F	Keystone	4	
47	Screw, Phillips 4-40 x 1/4	PMS 440 0025 PM	B & F Fastener	4	
48	Heatsink, TO-220	591202B00000G	Aavid Thermalloy	1	

8. Test Results

The IRPLLED1 board was tested using the following test equipment:
Oscilloscope: LeCroy Wave Surfer 454
Power Analyser: Chroma 6630
AC Power Source: California Instruments 801P
Electronic Load: Chroma 6314 frame + 63105 module

Using an electronic AC power source ensures that the input voltage waveform will be a nearly pure sine wave and this will give the most accurate possible current THD and power factor measurements. Measurements made with supplied connected through auto transformers and/or isolation transformers can give slightly worse results as the voltage waveform applied to the IRPLPFC1 input is not a pure sinusoid.

Input frequency was 60Hz in all tests, load was 90W, output voltage was 425V.

Input Voltage (RMS)	Power Factor	THDi (%)
90	0.995	7.0
100	0.995	6.5
110	0.995	6.0
120	0.994	5.6
130	0.993	5.3
140	0.992	5.0
150	0.991	4.9
160	0.989	4.9
170	0.988	5.0
180	0.986	5.2
190	0.980	7.3
200	0.976	7.9
210	0.973	8.1
220	0.970	8.5
230	0.966	9.0
240	0.962	9.5
250	0.957	10.1
260	0.952	10.6
270	0.947	11.3

Table 1: 90W PF and THDi Results

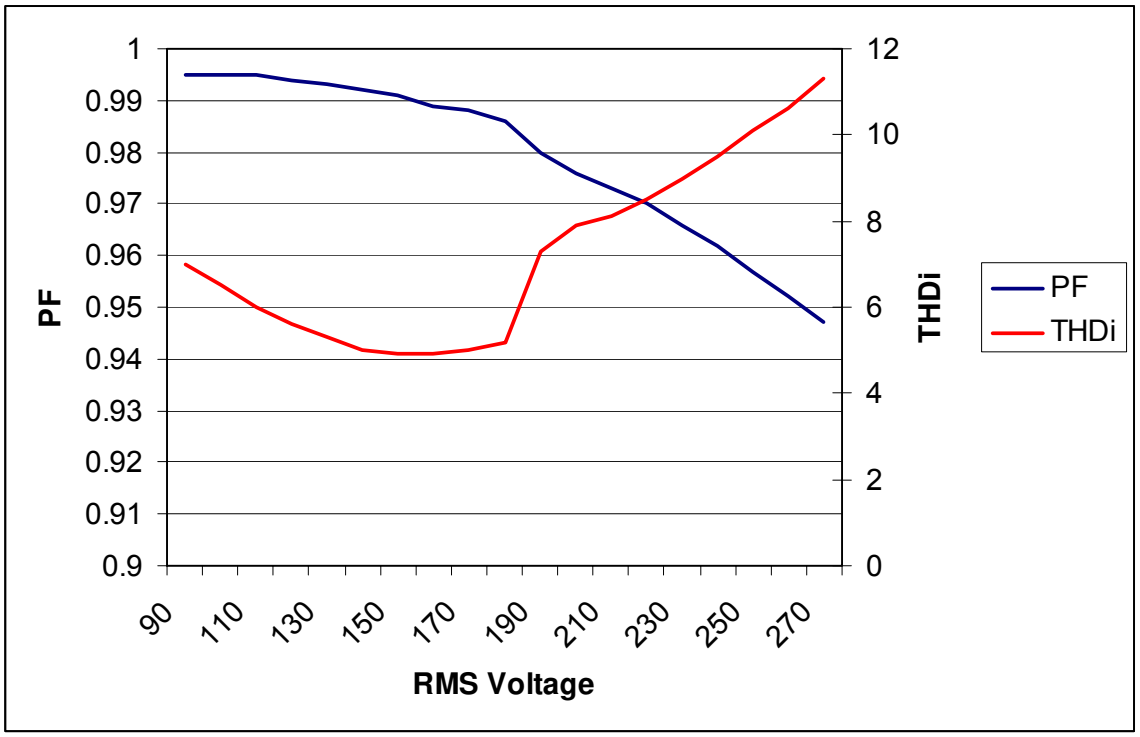


Figure 11: 90W PF and THDi vs input voltage at dull load

Figure 11 shows the results from table 1 in graphical form with 90W load as the input voltage varies from 90 to 270Vrms. The THDi remains under 10% over most of this range measuring 5.5% at 120Vrms and 8.4% at 220Vrms.

Tests carried out at 120VAC input:

Input Power (W)	Power Factor	THDi (%)
10.0	0.894	22.2
20.2	0.961	13.0
30.3	0.979	8.7
39.5	0.987	6.1
50.0	0.990	5.1
60.5	0.992	5.0
69.8	0.993	5.2
80.4	0.994	5.5
89.8	0.994	5.5

Table 2: Power factor and THDi vs load at 120VAC

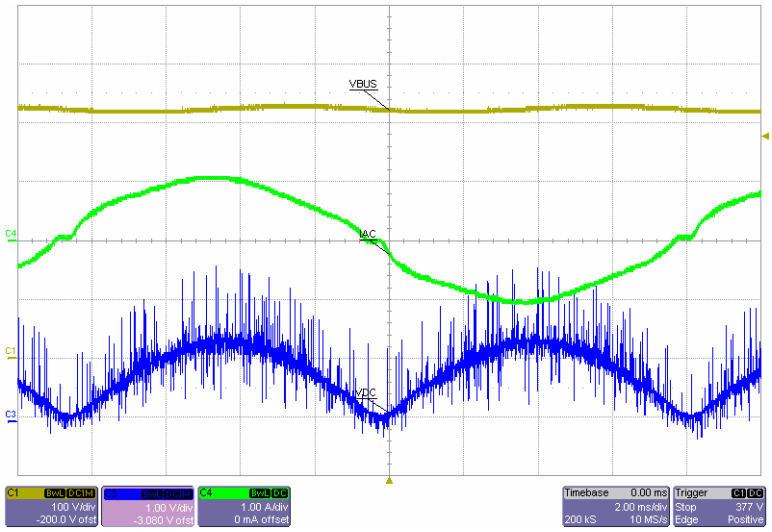


Figure 12 : VBUS, IAC and VDC at 120VAC, 90W

The green trace in Figure 12 shows the sinusoidal shape of the power factor corrected current at 120VAC line input and 90W load. The 425V nominal DC bus voltage is also in the brown trace along with the VDC pin input consisting of the divided rectified bridge voltage used to determine the on time modulation which minimizes cross over distortion as seen.
Table 2 shows the IRPLPFC1 reference design at low line the power factor remains high and THDi remains under 10% down to below 30% of maximum load.

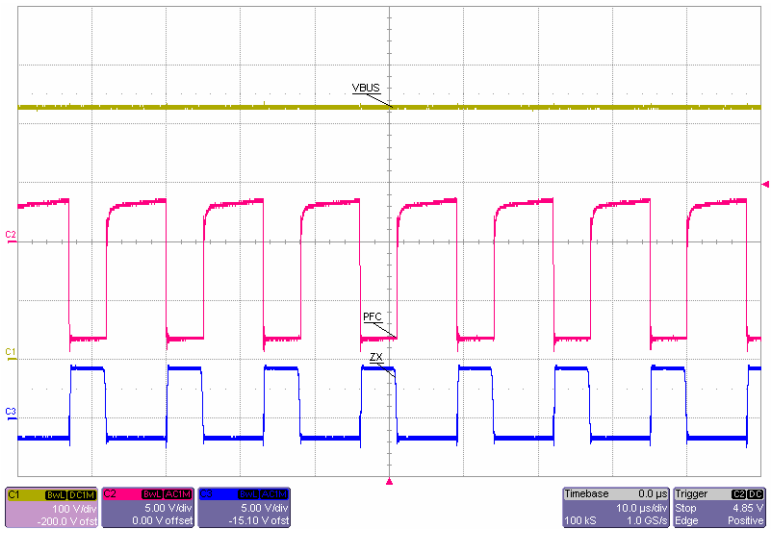


Figure 13 : VBUS, Gate Drive and ZX at 120VAC, 90W, line peak

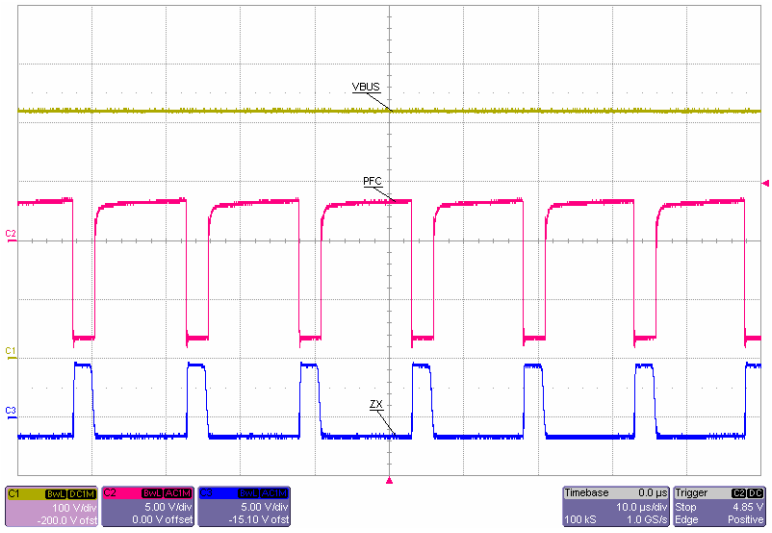


Figure 14 : VBUS, Gate Drive and ZX at 120VAC, 90W, line valley

Figures 13 and 14 show on time modulation functioning by displaying the red MOSFET gate drive voltage and the ZX input voltage. Close to the AC input zero crossing the on time is increased, shown in figure 14.

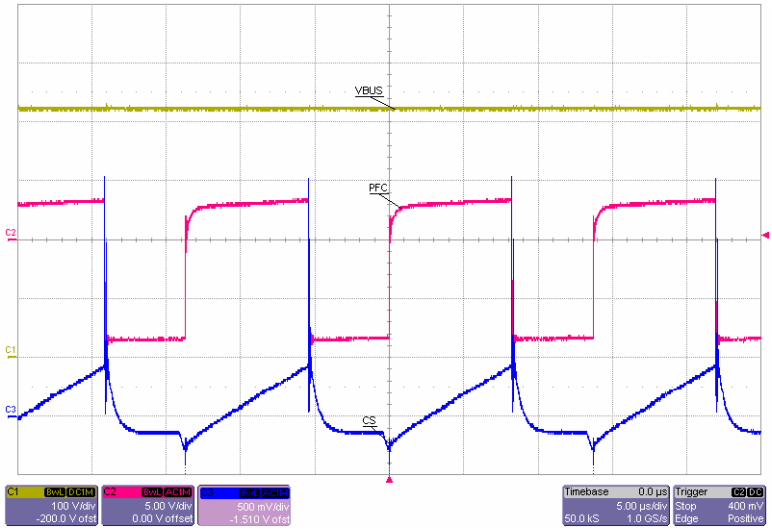


Figure 15 : VBUS, Gate Drive and OC at 120VAC, 90W

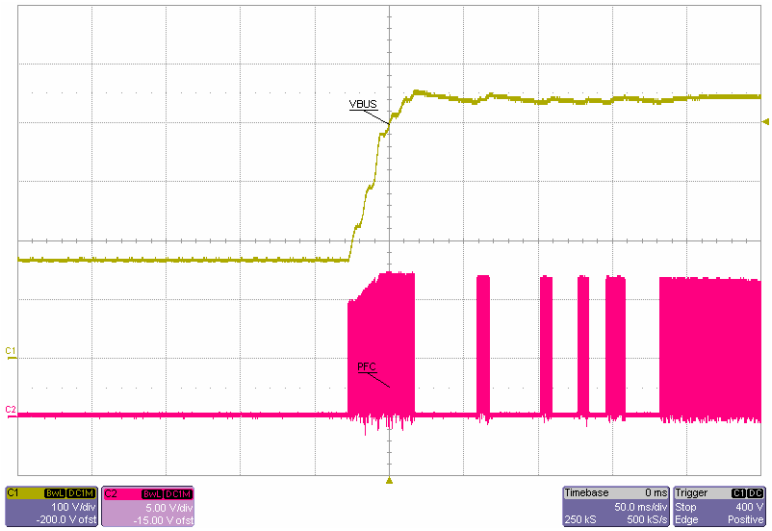


Figure 16: VBUS and Gate Drive at startup, 120VAC, 10W

Figure 15 shows the OC input reaching a peak of close to 500mV at full load. This increases when the line voltage is reduced but remains sufficiently below the 1.1V OC threshold to prevent cycle by cycle current limiting occurring during normal operation. It is important to correctly size the current sense resistor to prevent current limiting under low line, high load conditions as this distorts the AC line current, reduces the power factor and increases THDi.
Figure 16 shows the dynamic over voltage protection operating at startup at very light load to prevent the voltage from overshooting. The gate drive shown in the red trace is disabled when the bus voltage exceeds the nominal level. This is necessary since the error amplifier control loop operates slowly over many cycles