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DS33R41
Inverse-Multiplexing Ethernet Mapper with Quad Integrated T1/E1/J1 Transceivers

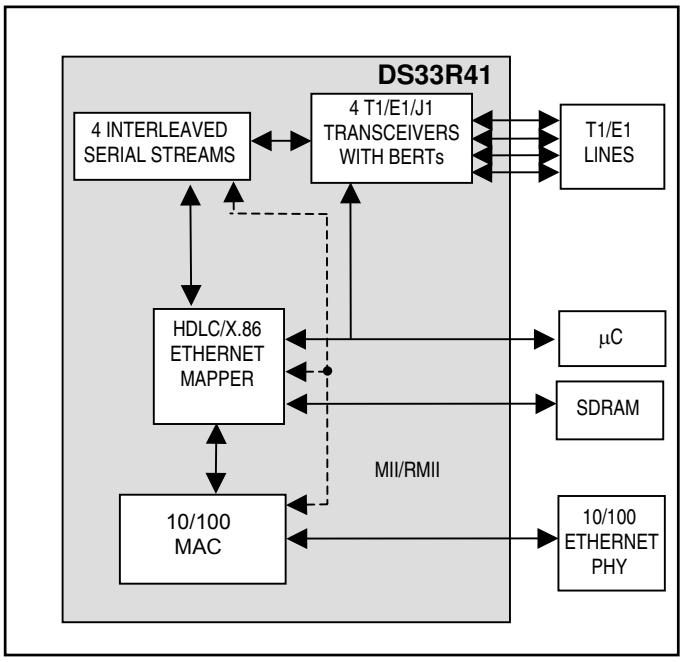
www.maxim-ic.com

GENERAL DESCRIPTION

The DS33R41 extends a 10/100 Ethernet LAN segment by encapsulating MAC frames in HDLC or X.86 (LAPS) for transmission over four interleaved T1/E1/J1 lines using a robust, balanced, and programmable inverse multiplexing. Four integrated T1/E1/J1 transceivers provide framing and line interfacing functionality.

The device performs store-and-forward of packets with full wire-speed transport capability. The built-in committed information rate (CIR) controller provides fractional bandwidth allocation up to the line rate in increments of 512kbps.

FUNCTIONAL DIAGRAM



FEATURES

- **10/100 IEEE 802.3 Ethernet MAC (MII and RMII) Half/Full Duplex with Automatic Flow Control**
- **Layer 1 Inverse Multiplexing Over Four T1/E1/J1 Lines Through the Integrated Framers and LIUs**
- **Supports Up to 7.75ms Differential Delay**
- **Aggregate Bandwidth from Up to Four T1/E1/J1 Links**
- **T1/E1 Signaling Capability for OAM**
- **HDLC/LAPS Encapsulation with Programmable FCS, Interframe Fill**
- **CIR Controller Provides Fractional Allocations in 512kbps Increments**
- **Programmable BERTs**
- **External 16MB, 100MHz SDRAM Buffering**
- **Parallel Microprocessor Interface**
- **1.8V, 3.3V Power Supplies**
- **IEEE 1149.1 JTAG Support**

Features continued on page 11.

APPLICATIONS

Bonded Transparent LAN Service
LAN Extension
Ethernet Delivery Over T1/E1/J1

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS33R41	-40°C to +85°C	400 BGA

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here:* ***www.maxim-ic.com/errata****.*

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1 DESCRIPTION

The DS33R41 provides interconnection and mapping functionality between Ethernet packet systems and T1/E1/J1 WAN time-division multiplexed (TDM) systems. The device is composed of a 10/100 Ethernet MAC, packet arbiter, committed information rate controller (CIR), HDLC/X.86 (LAPS) mapper, SDRAM interface, control ports, four bit error-rate testers (BERTs), and four integrated T1/E1/J1 transceivers. The packet interface consists of an MII/RMII Ethernet PHY interface. The Ethernet interface can be configured for 10Mbps or 100Mbps service. The DS33R41 encapsulates Ethernet traffic with HDLC or X.86 (LAPS) encoding to be transmitted over up to four T1, E1, or J1 lines. The T1/E1/J1 interfaces also receive encapsulated Ethernet packets and transmit the extracted packets over the Ethernet ports. Access is provided between the serial port and the integrated T1/E1/J1 transceivers to the intermediate signal bus that is based on the Dallas Semiconductor integrated bus operation (IBO), running at 8.192Mbps.

The device includes four software-selectable T1, E1, or J1 transceivers for short-haul and long-haul applications. Each transceiver is composed of a line interface unit (LIU), framer, and two additional HDLC controllers. The transceivers are software compatible with the popular DS2155 and DS21455.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock/data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns and alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

The transmit and receive paths of the integrated transceivers also have two HDLC controllers. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 128-bit FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time required handles SS7 applications.

The backplane interface of the integrated transceivers provides a method of sending and receiving data from the integrated Ethernet Mapper over an interleaved 8.192MHz TDM (IBO) bus. The elastic stores are required for IBO operation and they manage slip conditions.

An 8-bit parallel microcontroller port provides access for control and configuration of all the features of the device. The internal 100MHz SDRAM controller interfaces to a 32-bit wide 128Mbit SDRAM. The SDRAM is used to buffer the data from the Ethernet and WAN ports for transport. The external SDRAM can accommodate up to 8192 frames with a maximum frame size of 2016 bytes. Diagnostic capabilities include SDRAM BIST, loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection. The DS33R41 operates with a 1.8V core supply and 3.3V I/O supply.

The integrated Ethernet mapper is software compatible with the DS33Z41 quad inverse-multiplexing Ethernet mapper. There are a few things to note when porting a DS33Z41 application to this device:

- RSER has been renamed to RSERI.
- RCLK has been renamed to RCLKI.
- TSER has been renamed to TSERO.
- TCLK has been renamed to TCLKE.

The integrated T1/E1/J1 transceivers are software compatible with the DS21458 quad T1/E1/J1 transceiver. There are a few things to note when porting a DS21458 application to this device:

- The facilities data link (FDL) support is available through software only. The TLINK, RLINK, TLCLK, RLCLK pins are not available on the DS33R41.
- Multiplexed microprocessor bus mode is not supported on the DS33R41.
- The extended system information bus (ESIB) is not supported on the DS33R41.
- The RSIGF signaling freeze indication hardware pin is not available.
- The user output pins UOP1, UOP2, UOP3, and UOP4 are not available.

2 FEATURE HIGHLIGHTS

2.1 General

- 400-pin, 27mm BGA package
- 1.8V and 3.3V supplies
- IEEE 1149.1 JTAG boundary scan
- Software access to device ID and silicon revision
- Development support includes evaluation kit, driver source code, and reference designs
- Programmable output clocks for fractional T1, E1, H0, and H12 applications

2.2 Microprocessor Interface

- Parallel control port with 8-bit data bus
- Nonmultiplexed Intel and Motorola timing modes
- Internal software reset and external hardware reset input pin
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Global interrupt output pin

2.3 Link Aggregation (Inverse Multiplexing)

- Link aggregation for up to four T1/E1 links
- 8.192Mbps IBO interface to Dallas Semiconductor Framers/Transceivers
- Differential delay compensation up to 7.75ms for the 4 T1/E1 links
- Handshaking protocol between local and distant end for establishment of aggregation

2.4 HDLC Ethernet Mapping

- Dedicated HDLC controller engine for protocol encapsulation
- Compatible with polled or interrupt driven environments
- Programmable FCS insertion and extraction
- Programmable FCS type
- Supports FCS error insertion
- Programmable packet size limits (minimum 64 bytes and maximum 2016 bytes)
- Supports bit stuffing/destuffing
- Selectable packet scrambling/descrambling (X^{43}+1)
- Separate FCS errored packet and aborted packet counts
- Programmable inter-frame fill for transmit HDLC

2.5 X.86 (Link Access Protocol for SONET/SDH) Ethernet Mapping

- Programmable X.86 address/control fields for transmit and receive
- Programmable 2-byte protocol (SAPI) field for transmit and receive
- 32-bit FCS
- Transmit transparency processing—7E is replaced by 7D, 5E
- Transmit transparency processing—7D replaced by 7D, 5D
- Receive rate adaptation (7D, DD) is deleted.
- Receive transparency processing—7D, 5E is replaced by 7E
- Receive transparency processing—7D, 5D is replaced by 7D
- Receive abort sequence the LAPS packet is dropped if 7D7E is detected
- Self-synchronizing X^{43} + 1 payload scrambling.

2.6 Additional HDLC Controllers in the Integrated T1/E1/J1 Transceiver

- Two additional independent HDLC controllers
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt driven environments
- Bit-oriented code (BOC) support

2.7 Committed Information Rate (CIR) Controllers

- CIR controller limits transmission of data from the Ethernet Interface to the serial interface
- CIR granularity at 512kbps
- CIR Averaging for smoothing traffic peaks

2.8 SDRAM Interface

- Interface for 128Mbit, 32-bit wide SDRAM
- SDRAM Interface speed up to 100MHz
- Auto refresh timing
- Automatic precharge
- Master clock provided to the SDRAM
- No external components required for SDRAM connectivity

2.9 T1/E1/J1 Framer

- Fully independent transmit and receive functionality
- Full receive- and transmit-path transparency
- T1 framing formats include D4, ESF, J1-D4, J1-ESF and SLC-96
- Japanese J1 support for CRC6 and yellow alarm
- E1 framing formats include FAS, CAS, and CRC-4
- Detailed alarm- and status-reporting with optional interrupt support
- Large path- and line-error counters for:
- T1—BPV, CV, CRC6, and framing bit errors
- E1—BPV, CV, CRC-4, E-bit, and frame alignment errors
- Timed or manual update modes
- User-defined Idle Code Generation on a per-channel basis in both transmit and receive paths
- Digital milliwatt code generation on the receive path
- ANSI T1.403-1998 support
- G.965 V5.2 link detect
- RAI-CI, AIS-CI detection and generation
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Three independent, In-band repeating-pattern generators and detectors
- Patterns from 1 bit to 8 bits or 16 bits in length
- RCL, RLOS, RRA, and RAIS alarms interrupt on change of state
- Flexible signaling support
- Software- or hardware-based
- Interrupt generated on change of signaling data
- Receive-signaling freeze on loss of sync, carrier loss, or frame slip
- Hardware pins to indicate carrier loss and signaling freeze
- Automatic RAI generation to ETS 300 011 specifications
- Expanded access to Sa and Si bits
- Option to extend carrier-loss criteria to a 1ms period as per ETS 300 233

2.10 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.276MHz, or 12.552MHz for T1-only operation
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -12dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal-mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

2.11 MAC Interface

- MAC port with standard MII (less TX_ER) or RMII
- 10Mbps and 100Mbps data rates
- Configurable DTE or DCE modes
- Facilitates auto-negotiation by host microprocessor
- Programmable half- and full-duplex modes
- Flow control for both half-duplex (back-pressure) and full-duplex (PAUSE) modes
- Programmable Maximum MAC frame size up to 2016 bytes
- Minimum MAC frame size: 64 bytes
- Discards frames greater than programmed maximum MAC frame size and runt, nonoctet bounded, or bad-FCS frames upon reception
- Programmable threshold for SDRAM queues to initiate flow control and status indication
- MAC loopback support for transmit data looped to receive data at the MII/RMII interface

2.12 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered line clock or master clock

2.13 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.14 System Interface

- Dual two-frame, independent receive and transmit elastic stores
  - Independent control and clocking
  - Controlled-slip capability with status
  - Minimum-delay mode supported
- Supports T1 to E1 conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation with rates of 4.096MHz, 8.192MHz, and 16.384MHz
- Hardware-signaling capability
  - Receive-signaling reinsertion to a backplane, multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
- Access to the data streams in between the framer/formatter and the elastic stores
- User-selectable synthesized clock output

2.15 Test and Diagnostics

- IEEE 1149.1 Support
- Programmable on-chip BERT
- Patterns include Pseudorandom QRSS, Daly, and user-defined repetitive patterns
- Error insertion for a single bit or continuous
- Insertion options include continuous and absolute number with selectable insertion rates
- Total-bit and errored-bit counters
- Payload Error Insertion
- Errors can be inserted over the entire frame or selected channels
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel payload loopback)

2.16 Specifications Compliance

The DS33R41 meets relevant telecommunications specifications. The following table provides the specifications and relevant sections that are applicable to the DS33R41.

Table 2-1. T1-Related Telecommunications Specifications

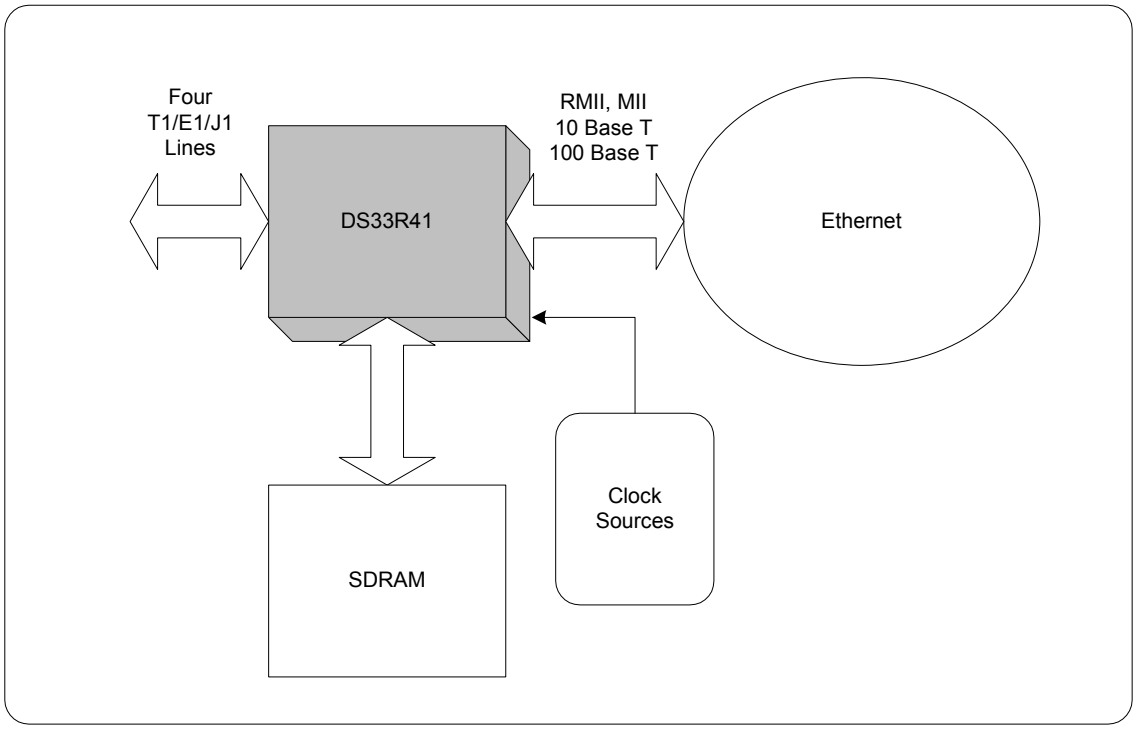
IEEE 802.3-2002 - CSMA/CD access method and physical layer specifications.
RFC1662 - PPP in HDLC-like Framing
RFC2615 - PPP over SONET/SDH
X.86 - Ethernet over LAPS
RMII - Industry Implementation Agreement for “Reduced MII Interface,” Sept 1997
ANSI - T1.403-1995, T1.231-1993, T1.408
AT&T: TR54016, TR62411
ITU: G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, O.161
ETS: ETS 300 011, ETS 300 166, ETS 300 233, CTR4, CTR12
Japanese: JTG.703, JTI.431, JJ-20.11 (CMI coding only)

3 APPLICATIONS

- Bonded Transparent LAN Service
- LAN Extension
- Ethernet Delivery over T1/E1/J1

Also see *Application Note 3411: DS33Z11—Ethernet LAN to Unframed T1/E1 WAN Bridge* for an example of a complete LAN to WAN design.

Figure 3-1. Quad T1E1 SCT to DS33R41



4 ACRONYMS AND GLOSSARY

- BERT - Bit Error Rate Tester
- DCE - Data Communication Interface
- DTE- Data Terminating Interface
- FCS - Frame Check Sequence
- HDLC - High Level Data Link Control
- MAC - Media Access Control
- MII - Media Independent Interface
- RMII - Reduced Media Independent Interface
- WAN - Wide Area Network

Note 1: Previous versions of this document used the term “Subscriber” to refer to the Ethernet Interface function. The register names have been allowed to remain with a “SU.” prefix to avoid register renaming.

Note 2: Previous versions of this document used the term “Line” to refer to the Serial Interface. The register names have been allowed to remain with a “LI.” prefix to avoid register renaming.

Note 3: The terms “Transmit Queue” and “Receive Queue” are with respect to the Ethernet Interface. The Receive Queue is the queue for the data that arrives on the MII/RMII interface, is processed by the MAC and stored in the SDRAM. Transmit queue is for data that arrives from the Serial port, is processed by the HDLC and stored in the SDRAM to be sent to the MAC transmitter.

Note 4: This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125μs T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1 each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last. The term “locked” is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

TIME SLOT NUMBERING SCHEMES

Time Slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Phone Channel		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

5 MAJOR OPERATING MODES

Microprocessor control is possible through the 8-bit parallel control port and provides configuration for all the features of the device. The Ethernet Link Transport Engine in the device can be configured for HDLC or X.86 encapsulation.

The integrated transceivers can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, two additional HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations.

The LIUs are composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths.

More information on microprocessor control is available in Section 8.1.

6 BLOCK DIAGRAMS

Figure 6-1. Detailed Block Diagram

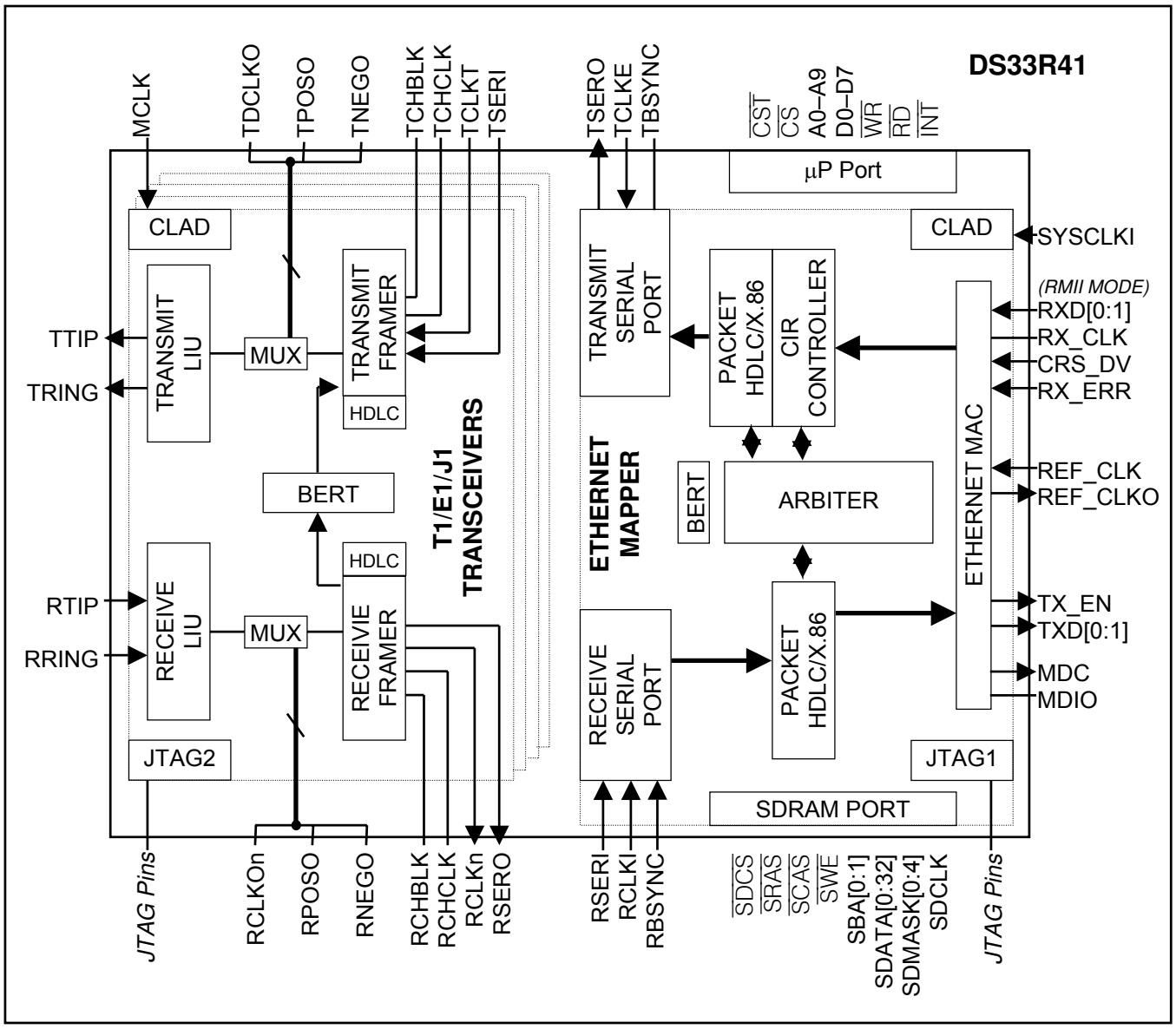
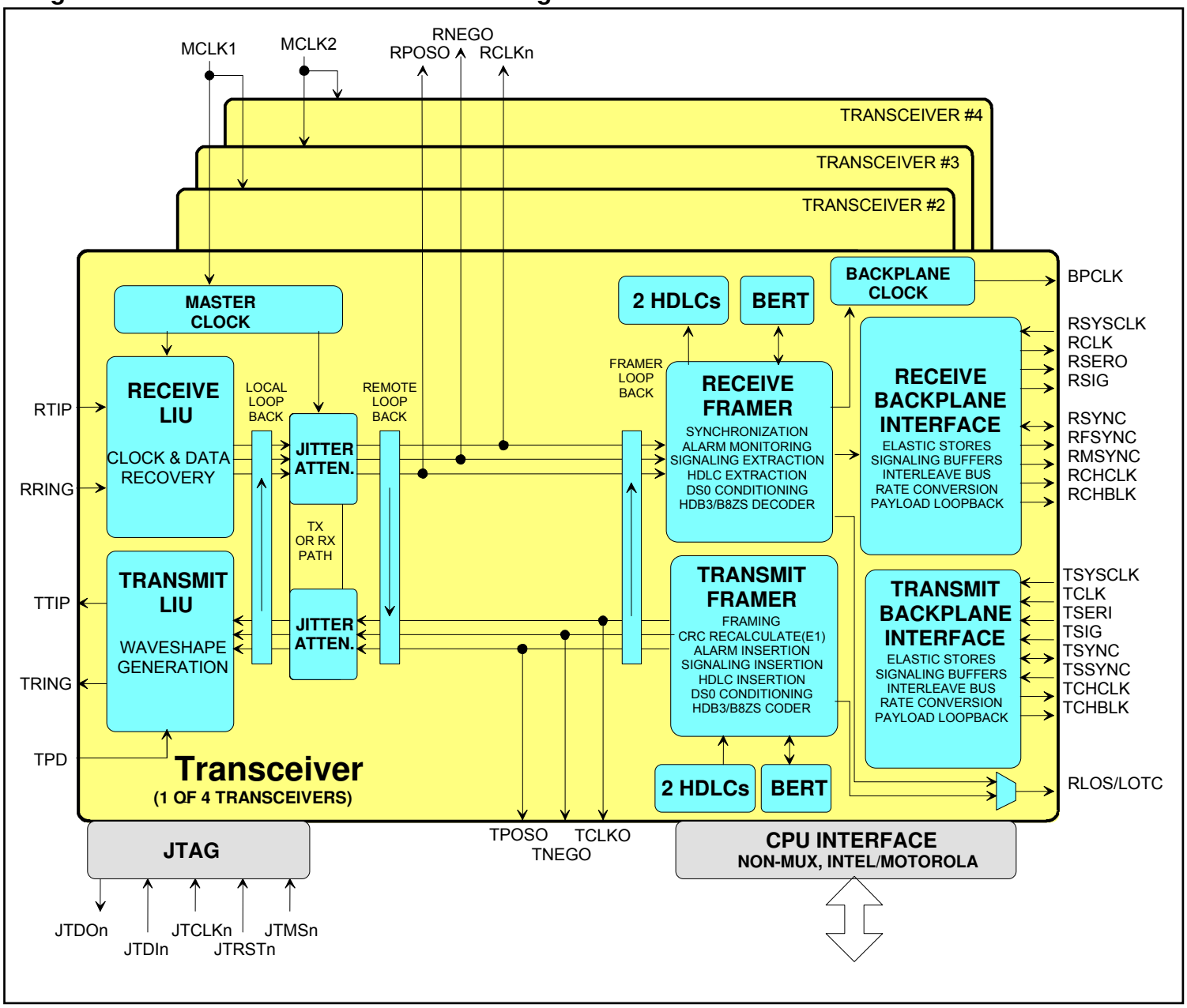


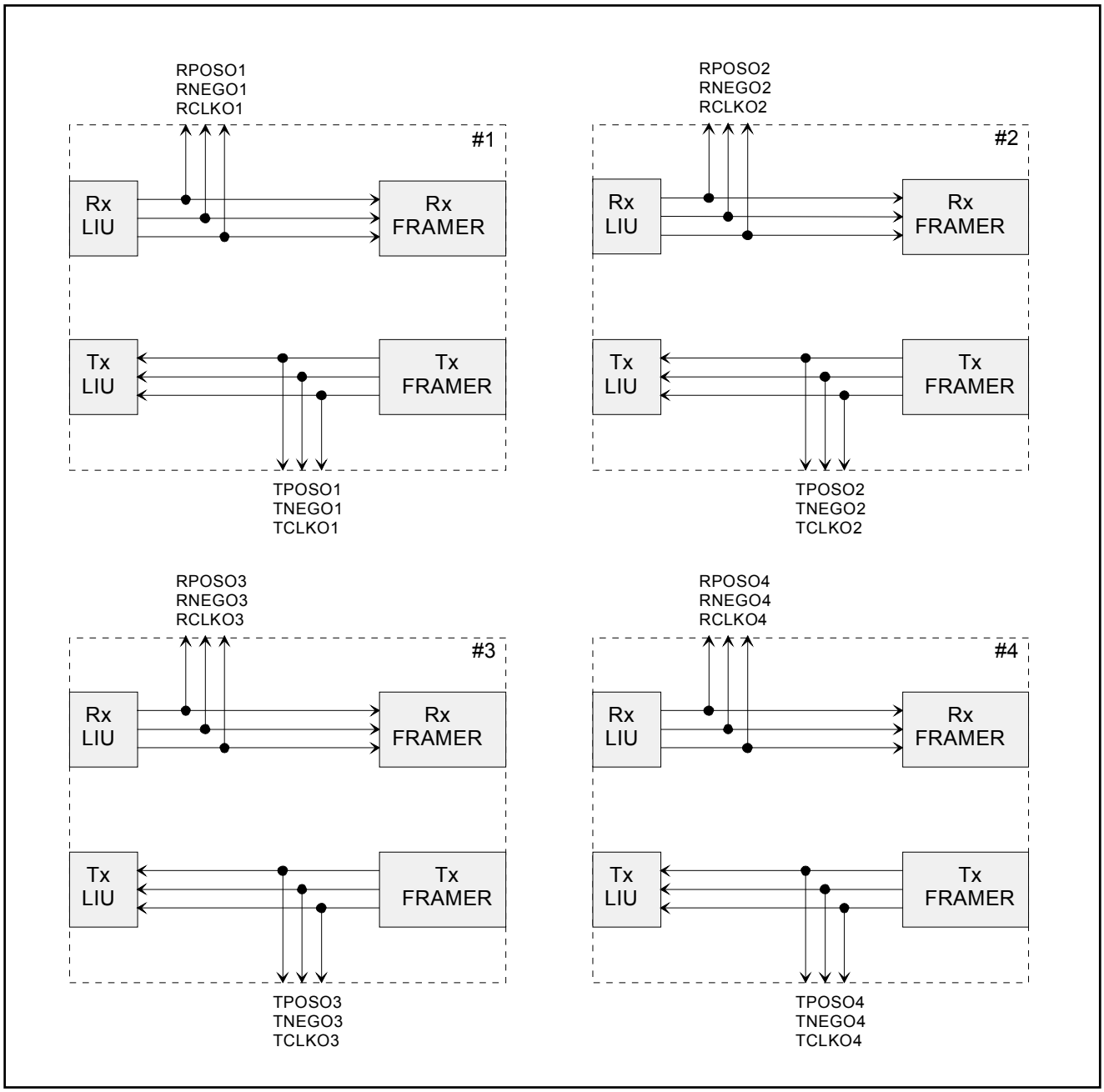
Figure 6-2. T1/E1/J1 Transceiver Block Diagram



6.1 Framer/LIU Interim Signals

The user has limited access to clock and data signals between the framer and LIU on all transceivers as shown in Figure 6-3. Access to the clock and bipolar data signals between the framer and LIU function can be used for specialized applications.

Figure 6-3. Framer/LIU Interim Signals



7 PIN DESCRIPTIONS

7.1 Pin Functional Description

Note that all digital pins are inout pins in JTAG mode. This feature increases the effectiveness of board level ATPG patterns.

I = input, O = output, Ipu = input with pullup, Oz = output with tri-state, IO = bidirectional pin, IOz = bidirectional pin with tri-state

Table 7-1. Detailed Pin Descriptions

NAME	PIN	TYPE	FUNCTION
MICROPROCESSOR PORT			
A0	A19	I	**Address Bit 0.** Address bit 0 of the microprocessor interface. Least Significant Bit.
A1	A20	I	**Address Bit 1.** Address bit 1 of the microprocessor interface.
A2	C18	I	**Address Bit 2.** Address bit 2 of the microprocessor interface.
A3	B18	I	**Address Bit 3.** Address bit 3 of the microprocessor interface.
A4	E18	I	**Address Bit 4.** Address bit 4 of the microprocessor interface.
A5	A18	I	**Address Bit 5.** Address bit 5 of the microprocessor interface.
A6	E17	I	**Address Bit 6.** Address bit 6 of the microprocessor interface.
A7	C17	I	**Address Bit 7.** Address bit 7 of the microprocessor interface.
A8	D17	I	**Address Bit 8.** Address bit 8 of the microprocessor interface.
A9	C16	I	**Address Bit 9.** Address bit 9 of the microprocessor interface.
D0	G17	IOZ	**Data Bit 0.** Bidirectional data bit 0 of the microprocessor interface. Least Significant Bit. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D1	A17	IOZ	**Data Bit 1.** Bidirectional data bit 1 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D2	F17	IOZ	**Data Bit 2.** Bidirectional data bit 2 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D3	F16	IOZ	**Data Bit 3.** Bidirectional data bit 3 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D4	E16	IOZ	**Data Bit 4.** Bidirectional data bit 4 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D5	D16	IOZ	**Data Bit 5.** Bidirectional data bit 5 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D6	B15	IOZ	**Data Bit 6.** Bidirectional data bit 6 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D7	C15	IOZ	**Data Bit 7.** Bidirectional data bit 7 of the microprocessor interface. Most Significant Bit. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
$\overline{WR}$/R$\overline{W}$	A16	I	**Write (Intel Mode).** The DS33R41 captures the contents of the data bus (D0–D7) on the rising edge of $\overline{WR}$ and writes them to the addressed register location. $\overline{CS}$ must be held low during write operations. **Read Write (Motorola Mode).** Used to indicate read or write operation. R$\overline{W}$ must be set high for a register read cycle and low for a register write cycle.
$\overline{RD}$/$\overline{DS}$	F15	I	**Read Data Strobe (Intel Mode).** The DS33R41 drives the data bus (D0–D7) with the contents of the addressed register while $\overline{RD}$ and $\overline{CS}$ are both low. **Data Strobe (Motorola Mode).** Used to latch data through the microprocessor interface. $\overline{DS}$ must be low during read and write operations.

NAME	PIN	TYPE	FUNCTION
$\overline{CS}$	H16	I	**Chip Select for Protocol Conversion Device.** This pin must be taken low for read/write operations. When $\overline{CS}$ is high, the $\overline{RD}/\overline{DS}$ and $\overline{WR}$ signals are ignored.
$\overline{CST}$	W6	I	**Chip Select for the T1/E1/J1 Transceivers.** Must be low to read or write the T1/E1/J1 Transceivers
$\overline{INT}$	E15	OZ	**Interrupt Output.** Outputs a logic zero when an unmasked interrupt event is detected. $\overline{INT}$ is deasserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is programmable in register GL.CR1. This pin is deasserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is programmable in register GL.CR1.
MII/RMII PHY PORT			
COL_DET	N20	I	**Collision Detect (MII).** Asserted by the MAC PHY to indicate that a collision is occurring. In DCE Mode this signal should be connected to ground. This signal is only valid in half duplex mode, and is ignored in full duplex mode
RX_CRS/ CRS_DV	N19	I	**Receive Carrier Sense (MII).** Should be asserted (high) when data from the PHY (RXD[3:0) is valid. For each clock pulse 4 bits arrive from the PHY. Bit 0 is the least significant bit. In DCE mode, connect to V_{DD}. **Carrier Sense/Receive Data Valid (RMII).** This signal is asserted (high) when data is valid from the PHY. For each clock pulse 2 bits arrive from the PHY. In DCE mode, this signal must be grounded.
RX_CLK	K19	IO	**Receive Clock (MII).** Timing reference for RX_DV, RX_ERR and RXD[3:0], which are clocked on the rising edge. RX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation).
RXD[0] RXD[1] RXD[2] RXD[3]	J19 H18 J18 H19	O	**Receive Data 0 through 3 (MII).** Four bits of received data, sampled synchronously with the rising edge of RX_CLK. For every clock cycle, the PHY transfers 4 bits to the DS33R41. RXD[0] is the least significant bit of the data. Data is not considered valid when RX_DV is low. **Receive Data 0 through 1 (RMII).** Two bits of received data, sampled synchronously with REF_CLK with 100Mbps Mode. Accepted when CRS_DV is asserted. When configured for 10Mbps Mode, the data is sampled once every 10 clock periods.
RX_DV	K18	I	**Receive Data Valid (MII).** This active high signal indicates valid data from the PHY. The data RXD is ignored if RX_DV is not asserted high.
RX_ERR	K20	I	**Receive Error (MII).** Asserted by the MAC PHY for one or more RX_CLK periods indicating that an error has occurred. Active High indicates Receive code group is invalid. If CRS_DV is low, RX_ERR has no effect. This is synchronous with RX_CLK. In DCE mode, this signal must be grounded. **Receive Error (RMII).** Signal is synchronous to REF_CLK;
TX_CLK	L18	IO	**Transmit Clock (MII).** Timing reference for TX_EN and TXD[3:0]. The TX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation).

NAME	PIN	TYPE	FUNCTION
TXD[0] TXD[1] TXD[2] TXD[3]	L20 M19 M18 M20	O	**Transmit Data 0 through 3(MII).** TXD [3:0] is presented synchronously with the rising edge of TX_CLK. TXD [0] is the least significant bit of the data. When TX_EN is low the data on TXD should be ignored. **Transmit Data 0 through 1(RMII).** Two bits of data TXD [1:0] presented synchronously with the rising edge of REF_CLK.
TX_EN	L19	O	**Transmit Enable (MII).** This pin is asserted high when data TXD [3:0] is being provided by the DS33R41. The signal is deasserted prior to the first nibble of the next frame. This signal is synchronous with the rising edge TX_CLK. It is asserted with the first bit of the preamble. **Transmit Enable (RMII).** When this signal is asserted, the data on TXD [1:0] is valid. This signal is synchronous to the REF_CLK.
REF_CLK	C20	I	**Reference Clock (RMII and MII).** When in RMII mode, all signals from the PHY are synchronous to this clock input for both transmit and receive. This required clock can be up to 50MHz and should have ±100ppm accuracy. When in MII mode in DCE operation, the DS33R41 uses this input to generate the RX_CLK and TX_CLK outputs as required for the Ethernet PHY interface. When the MII interface is used with DTE operation, this clock is not required and should be tied low. In DCE and RMII modes, this input must have a stable clock input before setting the RST pin high for normal operation.
REF_CLKO	G19	O	**Reference Clock Output (RMII and MII).** A derived clock output up to 50MHz, generated by internal division of the SYSCLKI signal. Frequency accuracy of the REF_CLKO signal will be proportional to the accuracy of the user-supplied SYSCLKI signal. See Section 9.1.2 for more information.
DCEDTES	L17	I	**DCE or DTE Selection.** The user must set this pin high for DCE Mode selection or low for DTE Mode. In DCE Mode, the DS33R41 MAC port can be directly connected to another MAC. In DCE Mode, the Transmit clock (TX_CLK) and Receive clock (RX_CLK) are output by the DS33R41. Note that there is no software bit selection of DCEDTES. Note that DCE Mode is only relevant when the MAC interface is in MII mode.
RMIIMIIS	K13	I	**RMII or MII Selection.** Set high to configure the MAC for RMII interfacing. Set low for MII interfacing.
PHY MANAGEMENT BUS			
MDC	E20	O	**Management Data Clock (MII).** Clocks management data between the PHY and DS33R41. The clock is derived from the SYSCLKI, with a maximum frequency is 1.67MHz. The user must leave this pin unconnected in the DCE Mode.
MDIO	F20	IO	**MII Management data IO (MII).** Data path for control information between the PHY and DS33R41. When not used, pull to logic high externally through a 10kΩ resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in 32 PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY. The user must leave this pin unconnected in the DCE Mode.
SDRAM CONTROLLER			
$\overline{\text{SCAS}}$	R14	O	**SDRAM Column Address Strobe.** Active low output, used to latch the column address on the rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SRAS}}$	P15	O	**SDRAM Row Address Strobe.** Active low output, used to latch the row address on rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SDCS}}$	R15	O	**SDRAM Chip Select.** Active low output enables SDRAM access.

NAME	PIN	TYPE	FUNCTION
$\overline{SWE}$	T15	O	**SDRAM Write Enable.** This active low output enables write operation and auto precharge.
SBA[0] SBA[1]	R16 W15	O	**SDRAM Bank Select.** These 2 bits select 1 of 4 banks for the read/write/precharge operations. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required.
SDATA[0] SDATA[1] SDATA[2] SDATA[3] SDATA[4] SDATA[5] SDATA[6] SDATA[7] SDATA[8] SDATA[9] SDATA[10] SDATA[11] SDATA[12] SDATA[13] SDATA[14] SDATA[15] SDATA[16] SDATA[17] SDATA[18] SDATA[19] SDATA[20] SDATA[21] SDATA[22] SDATA[23] SDATA[24] SDATA[25] SDATA[26] SDATA[27] SDATA[28] SDATA[29] SDATA[30] SDATA[31]	W11 M15 Y11 M14 U12 T13 R13 W13 V13 W12 V12 V11 R12 T11 T12 U11 T18 W18 P19 P20 W19 Y20 V19 W20 U20 U19 T20 T19 Y19 U18 V18 R18	IO	**SDRAM Data Bus Bits 0 through 31.** The 32 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high-impedance. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required.
SDA[0] SDA[1] SDA[2] SDA[3] SDA[4] SDA[5] SDA[6] SDA[7] SDA[8] SDA[9] SDA[10] SDA[11]	T17 U16 Y17 W17 U17 W16 Y16 V16 T16 V15 R17 P16	O	**SDRAM Address Bus 0 through 11.** The 12 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA0 to SDA11 at the rising edge of clock. Column address is determined by SDA0–SDA9 and SDA11 at the rising edge of the clock. SDA10 is used as an auto-precharge signal. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required.
SDMASK[0] SDMASK[1] SDMASK[2] SDMASK[3]	Y13 P14 P18 V17	O	**SDRAM Mask 0 through 3.** When high, a write is done for that byte. The least significant byte is SDATA7 to SDATA0. The most significant byte is SDATA31 to SDATA24.
SDCLKO	U14	O 4mA	**SDRAM CLK Out.** System clock output to the SDRAM. This clock is a buffered version of SYSCLKI.

NAME	PIN	TYPE	FUNCTION
T1/E1/J1 ANALOG LINE INTERFACES			
RTIP1	N1	I	**Receive Analog Tip Input for Transceiver 1.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RRING1	M1	I	**Receive Analog Ring Input for Transceiver 1.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RTIP2	J13	I	**Receive Analog Tip Input for Transceiver 2.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RRING2	J12	I	**Receive Analog Ring Input For Transceiver 2.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RTIP3	E6	I	**Receive Analog Tip Input for Transceiver 3.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RRING3	F6	I	**Receive Analog Ring Input for Transceiver 3.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RTIP4	T9	I	**Receive Analog Tip Input for Transceiver 4.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
RRING4	R9	I	**Receive Analog Ring Input for Transceiver 4.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details.
TTIP1	T1, U1	O	**Transmit Analog Tip Output for Transceiver 1.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TRING1	V1, W1	O	**Transmit Analog Ring Output for Transceiver 1.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TTIP2	A12, B12	O	**Transmit Analog Tip Output for Transceiver 2.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TRING2	A11, B11	O	**Transmit Analog Ring Output for Transceiver 2.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TTIP3	E1, E2	O	**Transmit Analog Tip Output for Transceiver 3.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TRING3	F1, F2	O	**Transmit Analog Ring Output for Transceiver 3.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.
TTIP4	W8, Y8	O	**Transmit Analog Tip Output for Transceiver 4.** Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details.