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Flexible Power Management Unit

IRPS5401

FEATURES

- Full power system including 5 integrated outputs
  - 4A, 4A, 2A and 2A Switching Regulators
  - 500mA Source/Sink Linear regulator
- Single rail operation 5.5V to 12V
- Output Range from 0.25V to 5.1V for outputs A-D and 0.5V to 3.6V for LDO
- Allows combining outputs and/or the use of an external PowIRstage to increase output current to as high as 50A
- Emulated current mode control without external compensation
- Differential voltage sensing on Switcher A for higher accuracy
- I2C / PMBus with integrated level shifter
- Advanced Sequencing control
- Extensive PMBus command set of 74 commands
- Integrated current sensing and full telemetry including voltage, current, temperature and faults
- Rated for -40°C to +125°C T_J operation
- Pb-Free, RoHS6, 7x7mm, 56-pin, 0.4mm pitch QFN

DESCRIPTION

The IRPS5401 is a complete power management unit delivering up to 5 output voltages to processors, FPGA's and other multi-rail power systems. Four high efficiency configurable switching regulators and a Source/Sink Linear regulator provide the typical rails required such as core voltage, memory voltage and I/O voltages.

Integrated, accurate current, voltage and temperature sensing allows telemetry and fault reporting through the I2C/PMBus.

The IRPS5401 switching regulators utilize fixed frequency Emulated current mode control, and thus no external compensation is required.

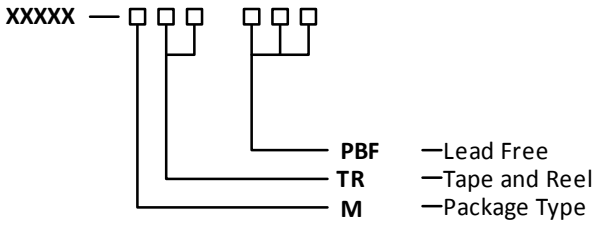
The IRPS5401 is highly flexible. Switchers A and B deliver 2A each. Switchers C and D, deliver 4A each and can also be combined to deliver 8A. Further, Switcher A can be configured to use an external powIRstage® to deliver up to 50A or more.

APPLICATIONS

- High density ASIC, FPGA & CPU multi-rail systems
- Embedded Computing systems
- Communications and Storage systems

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRPS5401	QFN 7 mm x 7 mm	Tape and Reel	3000	IRPS5401MTRPBF



BASIC APPLICATION

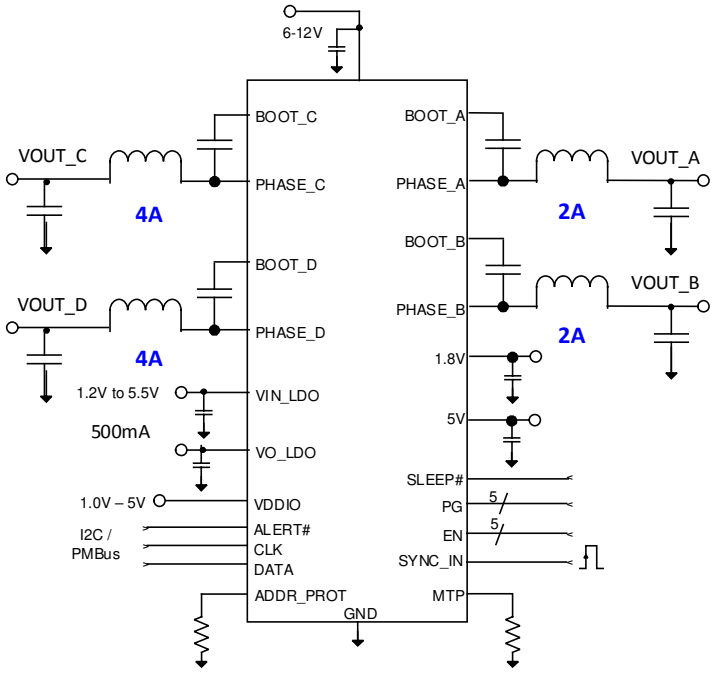


Figure 1: IRPS5401 Basic Application Circuit

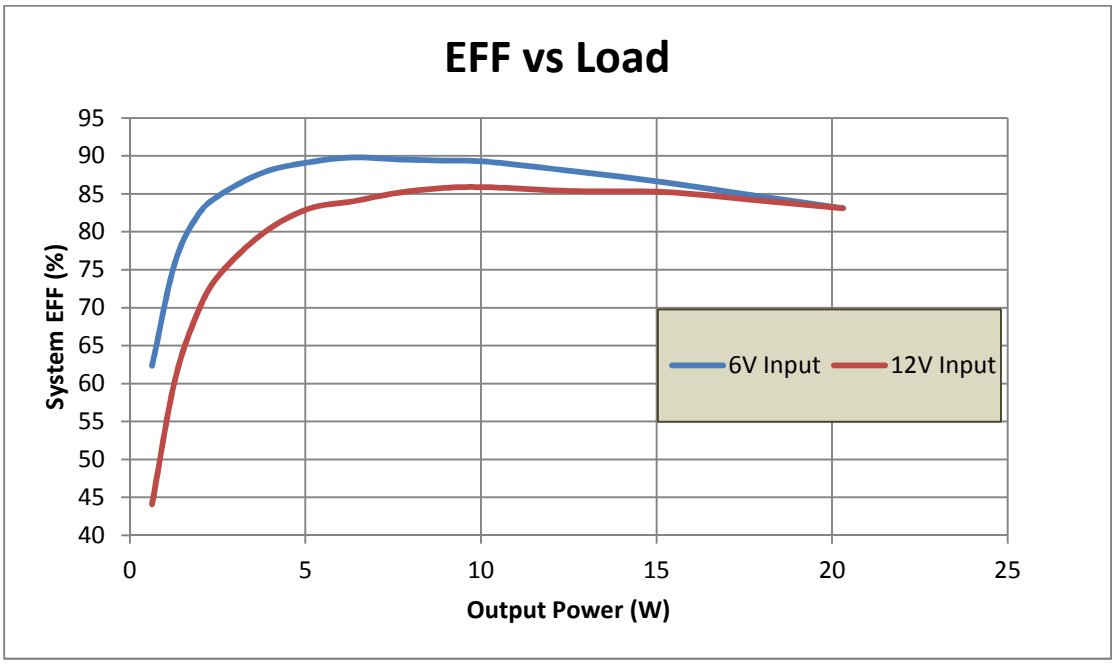


Figure 2: System Efficiency with VO= 2.5V, FSW=800KHz, Tj=45°C

PINOUT DIAGRAM

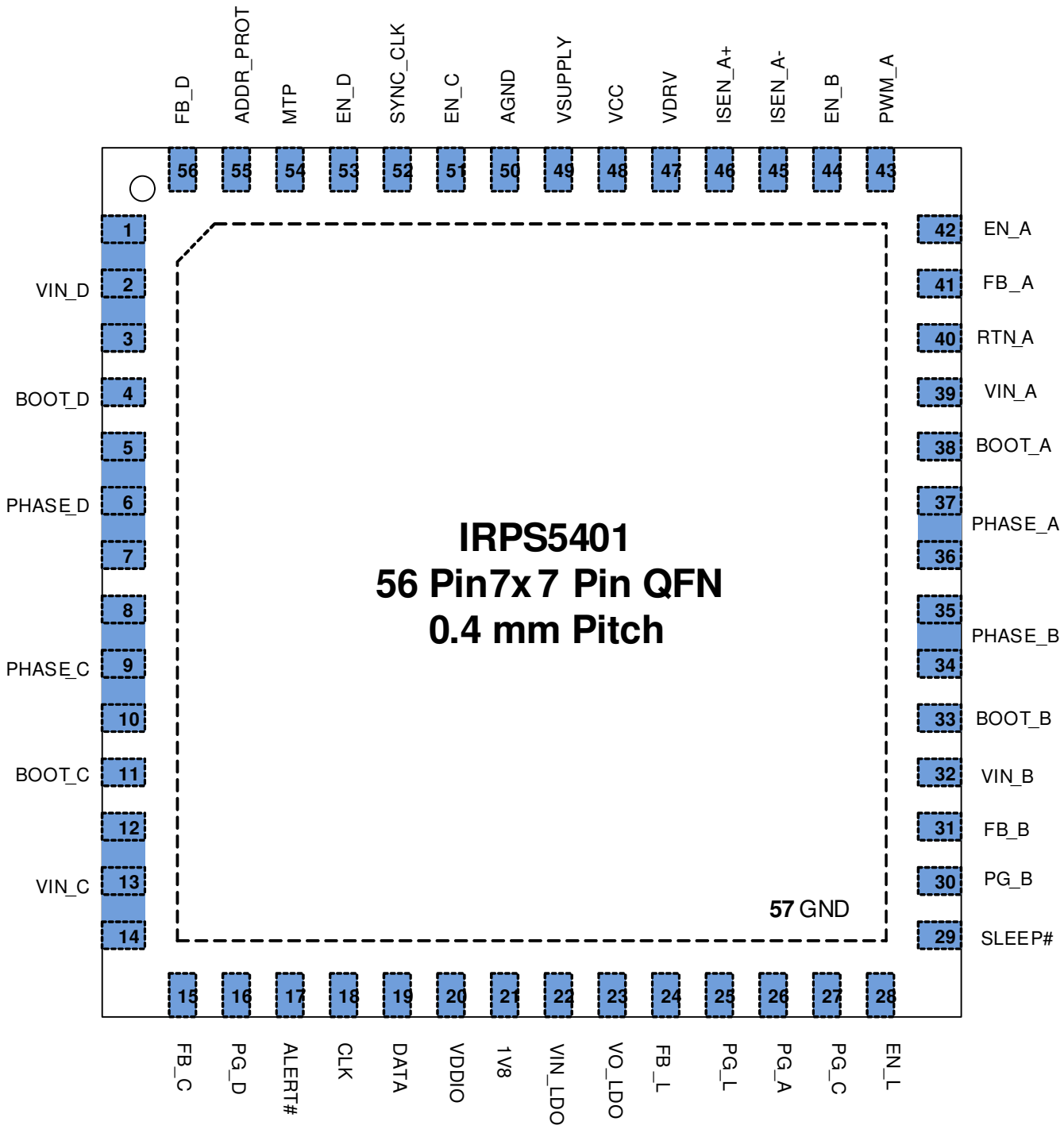


Figure 3: 7mm x 7mm QFN (Top View)

PIN FUNCTION

PIN				IF NOT USED
#	NAME	TYP	DESCRIPTION	
1,2,3	VIN_D	P [I]	Input supply voltage pins for Switcher D. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
4	BOOT_D	A [B]	Supply input for Switcher D high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ D pins. An internal diode is connected between VDRV and this pin	Open
5,6,7	PHASE_D	P [O]	Switch node of Switcher D. Connect directly to the output inductor.	
8,9,10	PHASE_C	P [O]	Switch node of Switcher C. Connect directly to the output inductor.	
11	BOOT_C	A [B]	Supply input for Switcher C high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_C pins. An internal diode is connected between VDRV and this pin	
12,13, 14	VIN_C	P [I]	Input supply voltage pins for Switcher C. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
15	FB_C	A [I]	Switcher C feedback input. Connect directly to VOUT_C for output voltages less than 2.55V. Connect to VOUT_C with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
16	PG_D	D [O]	Open drain power good output indicating Switcher D is powered up	
17	ALERT#	D [O]	I2C/PMBus Alert line. This alert signal can indicate one or more faults, allowing the system bus manager to poll the device and identify the root cause. All faults or customer selected faults such as overcurrent or over-temperature may be specifically masked to this pin.	
18	CLK	D [B]	I2C/PMBus Data Line. Pull up to VDDIO with 4.7K	n/a
19	DATA	D [B]	I2C/PMBus Clock Line. Pull up to VDDIO with 4.7K	
20	VDDIO	P [I]	Pull-up signal voltage for I2C communications. Connect to the same I/O rail used by the I2C master.	
21	1V8	A [O]	1.8V reference used by the device for internal analog and digital control. Decouple using a 1.0uF X7R type ceramic capacitor	
22	VIN_LDO	P [I]	Input to the linear regulator. See linear regulator section for specific requirements. This voltage can range from 1.2V to 5.5V, with restrictions on overall power dissipation	Short To GND
23	VO_LDO	A[O]	LDO output	Open
24	FB_L	A [I]	LDO feedback input	
25	PG_L	D[I]	Open drain power good output indicating LDO is powered up. Pull up to 5V with 10K	
26	PG_A	D[I]	Open drain power good output indicating switcher A is powered up. Pull up to 5V with 10K	
27	PG_C	D[I]	Open drain power good output indicating switcher C is powered up. Pull up to 5V with 10K	
28	EN_L	D[I]	LDO enable input control. Active High, external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
29	SLEEP#	D[I]	Active low signal to place the device in a low power mode LVTTL threshold levels. 'SLEEP ENABLED' threshold is 0.8V maximum	Short to VCC
30	PG_B	D[I]	Open drain power good output indicating switcher B is powered up. Pull up to 5V with 10K	Open
31	FB_B	A [I]	Switcher B feedback input. Connect directly to VOUT_B for output voltages less than 2.55V. Connect to VOUT_B with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
32	VIN_B	P [I]	Input supply voltage pin for Switcher B. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
33	BOOT_B	A [B]	Supply input for Switcher B high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ B pins. An internal diode is connected between VDRV and this pin	Open
34,35	PHASE_B	P [O]	Switch node of Switcher B. Connect directly to the output inductor.	
36,37	PHASE_A	P [O]	Switch node of Switcher A. Connect directly to the output inductor.	

PIN				IF NOT USED
#	NAME	TYP	DESCRIPTION	
38	BOOT_A	A [B]	Supply input for Switcher A high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_A pins. An internal diode is connected between VDRV and this pin	
39	VIN_A	P [I]	Input supply voltage pin for Switcher A. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
40	RTN_A	A [I]	Differential feedback return signal for Switcher A. This can be connected remotely to the return location of VOUT_A.	Short together
41	FB_A	A [I]	Differential feedback positive signal for Switcher A. Connect directly to VOUT_A for output voltages less than 2.55V. Connect to VOUT_A with a 2:1 resistor divider for output voltages greater than 2.55V.	
42	EN_A	D [I]	Switcher A enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
43	PWM_A	A [O]	PWM signal for Switcher A to be used when Switcher A is configured for use with an external powIRstage®. This PWM pin drives a powIRstage® such as an IR3555 powIRstage®, and is a tri-state or tri-level signal. Leave floating if this pin is not used	Open
44	EN_B	D [I]	Switcher B enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
45	ISEN_A-	A[I]	Negative (return) sense point for Switcher A external IOUT sense.	Short together
46	ISEN_A+	A[I]	Positive sense point for Switcher A external IOUT sense.	
47	VDRV	A [O]	5V drive voltage used to power the internal MOSFET drivers. Use a 2Ω, 1uF filter from VCC to insure noise from this switching node is not injected into the VCC pin. See the application section. Terminate decoupling cap to GND (pin 57)	n/a
48	VCC	A [O]	5V source used by the device to power internal analog and digital control. When VCC is self-generated by the device (from VSUPPLY), do not load this pin with any load other than VDRV. Decouple using a 1uF X7R type ceramic capacitor. Terminate decoupling cap to AGND (pin 50)	
49	VSUPPLY	A [I]	Input voltage for internal LDO for internally generated VCC	Short to VCC
50	AGND		Ground reference for the analog and digital control.	n/a
51	EN_C	D[I]	Switcher C enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
52	SYNC_CLK	D[I]	External Synchronization pin. LVTTL threshold levels. 'HIGH' threshold is 2.1V minimum, 'LOW' is 0.8V maximum	
53	EN_D	D [I]	Switcher D enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	
54	MTP	A [I]	A resistor placed to ground on this pin selects which of 15 MTP banks of memory are used. By allowing up to 15 MTP memory banks, a user can use up to 15 identical IRPS5401 devices on a single board using just one customer-configuration file. If this pin is above 2V when POR occurs, the device will not load OTP and the I2C address will be 0Ah. Decouple with 0.01uF cap.	n/a
55	ADDR_PROT		Use a resistor on this pin to set the I2C and/or PMBus Address offset for the device If the I2C register R/W protect security function is used and 'PIN' protect is enabled, this pin must be asserted high to disable the R/W protection. Decouple with 0.01uF cap.	
56	FB_D	A [I]	Switcher D feedback input. Connect directly to VOUT_D for output voltages less than 2.55V. Connect to VOUT_D with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
57	GND		Ground. The large metal pad on the bottom must be connected to Ground.	n/a

BLOCK DIAGRAM

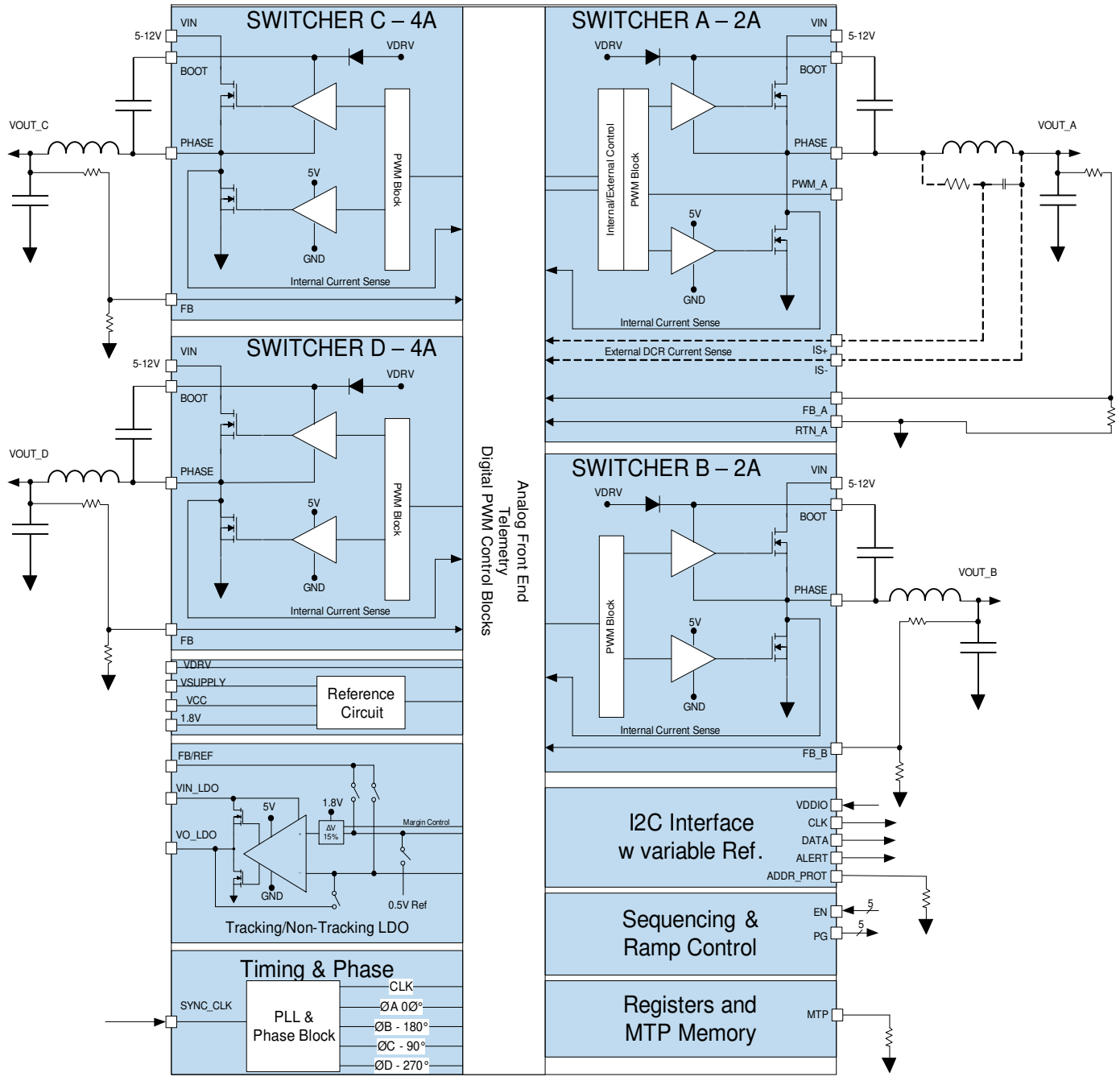


Figure 4: IRPS5401 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Voltage Ratings	
Vin [A_B_C_D], VSUPPLY	-0.3V to 16V
VCC, VDRIVE	-0.3V to 6V
1V8	-0.3V to 2V
BOOT [A_B_C_D]	-0.3V to 22V
BOOT [A_B_C_D] <10nS transient	-0.3V to 24V
SW [A_B_C_D]	-0.3V to 16V
SW [A_B_C_D] <10nS transient	-4V to 18V
BOOT to SW [A_B_C_D]	-0.3V to VCC +0.3V (Note1)
Input / Output Pins	-0.3V to VCC +0.3V (Note1)
GND to AGND	-0.3V to +0.3V
THERMAL INFORMATION	
Junction to Ambient Thermal Resistance Θ_{JA}	13.5°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	3°C/W
Maximum Storage Temperature Range	-55°C To 150°C
Maximum Junction Operating Temperature Range	-40°C To 125°C (Note 2)
Maximum Lead Temperature (Soldering 10s)	300°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.
Note 2: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

Recommended Operating Ambient Temperature Range	-40°C to 85°C
VIN [A to D]	1.2V to 14V (with external VCC)
VSUPPLY (for Internal VCC)	6V to 14V
External VCC and VDRIVE Voltage Range	4.5V to 5.5V
SWA and SWB Output Load	0A to 2A
SWC and SWD Output Load	0A to 4A
Combined SWC+SWD Output Load	0A to 8A

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VCC (Externally Supplied)	**VCC/GND**					
UVLO Turn-on Threshold				4.2	4.5	V
UVLO Turn-off Threshold			3.6	3.9		V
Supply Current	I_{VCC}	All outputs disabled (low power disabled)		40	45	mA
Supply Current	I_{VCC}	All outputs disabled (low power enabled)		25	30	mA
Supply Current	I_{VCC}	SLEEP# = low (Sleep Mode Enabled)		10	25	uA
VDRV						
UVLO Turn-on Threshold				4.2	4.5	V
UVLO Turn-off Threshold			3.6	3.9		V
Supply Current	I_{vdrv}	All outputs Enabled, Fsw =800KHz		15		mA
Internal Supply VCC LDO						
Input Voltage			6	-	14	V
Output Voltage (on Vcc pin)	V_{cc}	Ta=25°C, 6.0V<VSUPPLY<14V, 0mA<Iout<50mA	4.6	4.85	5.1	V
Output Current	I_{outmax}			-	75	mA
VDDIO						
Input Voltage[1]		I2C termination voltage	1.62	-	5.5	V
Input High Voltage		% of VDDIO	60	-	-	%
Input Low Voltage		% of VDDIO	-	-	30	%
Input Leakage		Vpad = 0 to 5.5V	-1	-	1	µA
Reference Voltage (DAC) [A to D]						
Range			0.25		2.55	V
Resolution				5		mV
Accuracy (0°C to 85°C junction temperature)		VID = 1.0 to 2.55V	-0.8	-	0.8	%
		VID = 0.5V to 0.995V	-8	-	8	mV
		VID = 0.25V to 0.495V	-10	-	10	mV
Accuracy[1] (-40°C to 125°C junction temperature)		VID = 1.0 to 2.55V	-1.5	-	1.5	%
		VID = 0.5V to 0.995V	-15	-	15	mV
		VID = 0.25V to 0.495V	-20	-	20	mV
Oscillator & PWM Generator						
Internal Oscillator[1]			-	48	-	MHz
Frequency Accuracy		0°C to 85°C junction temperature	-3	-	3	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Accuracy		-40°C to 125°C	-6.25		+6.25	%
PWM Frequency Range[1]			200	-	2000	KHz
PWM Resolution[1]			-	2.6	-	ns
Digital Inputs – TTL	**ADDR_PROT, EN_x**					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 5.5V	-1	-	1	µA
Digital Inputs – TTL	**SLEEP#**					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 5.5V	-10	-	10	µA
External Sync	**SYNC**					
Frequency range			200		1000	KHz
Voltage Range			0		5	Vdc
Input High voltage			2.1			V
Input Low Voltage					0.8	V
Input Leakage current		Vpad = 0 to 5.5V			±5	µA
Sync pin capacitance		Vpad = 0 to 5.5V			10	pF
Synchronization Range (From OTP setting)		0°C to 85°C	-6.25		+6.25	%
Synchronization Range (From OTP setting)		-40°C to 125°C	-3		+3	%
Sync signal Duty Cycle			45	50	55	%
Remote Voltage Sense Inputs	**FB [A to D], RTN_A**					
FB_x Input Current		VOUT = 0.25V to 2.55V	-35	-	90	µA
RTN_A Input Current			-	-50	-	µA
Differential Input Voltage Range[1]		RTN_A = ±100mV	0		2.55	V
RTN_A Input CM Voltage[1]			-100	-	100	mV
Remote Current Sense Inputs	**ISEN_A+/ISEN_A-**					
Common Mode Voltage Range[1]			-0.1	-	Vcc-1	V
Differential Voltage Range[1]			-10	-	60	mV
Analog Address/Level Inputs	**ADDR_PROT, MTP**					
Output Current[1]		Vpad = 0 to 1.2V	96	100	104	µA
Open-Drain Outputs	**PG_x, DATA, ALERT#**					
Output Low Voltage		4mA	-	-	0.3	V
Output Leakage		Vpad = 0 to 5.5V	-	-	±5	µA
PWM I/O	**PWM_A**					
Output Low Voltage		I = -4mA	-	-	0.4	V
Output High Voltage		I = +4mA	2.9	-	-	V
Tri-State Leakage		Vpad = 0 to Vcc	-	-	±1	µA
I2C/PMBus						
Bus Speed[1]		Normal	-	100	-	KHz
		Fast	-	400	-	KHz
		Maximum	-	1000	-	KHz
Telemetry Reporting - Switching Outputs [A to D]						
Iout, Iin, Vin and Temperature Filter Rate[1]		Selectable (Selected Frequency applies to all parameters for all loops)	-	0.97, 1.9, 3.8, 7.7, 15.5, 31, 63, 126	-	Hz
Iout, Iin, Vin, Temperature Update Rate[1]			-	25	-	kHz
Vin Reporting Range[1]			0	-	17.5	V
Vin Reporting Accuracy		VIN = 12V	-2	-	2	%
Vin Reporting Accuracy		VIN = 5V	-5	-	5	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Vin Reporting Resolution[1]			-	31.25	-	mV
Vout Reporting Range[1]		With 2:1 scaling	-	-	5.1	V
Vout Reporting Accuracy[1]		READ_VOUT reports DAC setting		0.5		%
Vout Reporting Resolution[1]	User Selectable per output through VOUT_MODE command. Actual resolution is 5mV/10mV depending on VOUT_SCALING		-	0.244 1.953 3.906	-	mV
Iout Reporting Gain Accuracy[1]	gain_error	Iread=Iout(1±gain_error)±I_os*full scale	-5		5	%
Iout Reporting Offset Accuracy[1]	I_os	full Scale = 2A for A/B and 4A for C/D	-2.5		2.5	%
Iout Reporting Resolution[1]			-	15.625	-	mA
Iin Reporting Resolution[1]			-	7.8125	-	mA
P_in Reporting Resolution[1]			-	31.25	-	mW
P_out Reporting Resolution[1]			-	31.25	-	mW
Temperature Reporting Resolution[1]				0.25		°C
Temperature Reporting Accuracy[1]			-2		2	%
Telemetry Reporting - Switching Output A with External PowIRstage ®						
Iout Reporting Resolution[1]			-	125	-	mA
Iout Reporting Accuracy[1]		At 100% full load. Assumes ± 5% accurate external source	-6		6	%
Iin Reporting Resolution[1]			-	62.5	-	mA
P_in Reporting Resolution[1]			-	250	-	mW
P_out Reporting Resolution[1]			-	250	-	mW
Telemetry Reporting - LDO						
Vin Reporting Range[1]			0	-	8	V
Vin Reporting Resolution[1]			-	7.812	-	mV
Vin Reporting Accuracy			-2	-	2	%
Vout Reporting Range[1]		Vout is measured	0	-	4	V
Vout Reporting Resolution[1]		User Selectable through VOUT_MODE command.	-	0.244 1.953 3.906	-	mV
Vout Reporting Accuracy			-2	-	2	%
Iout Reporting Range[1]			0	-	0.72	A
Iout Reporting Resolution[1]			-	0.976	-	mA
Iout Reporting Accuracy[1]		At 500mA	-10		10	%
P_in Reporting Resolution[1]			-	15.625	-	mW
P_out Reporting Resolution[1]			-	15.625	-	mW
Fault Protection - Switchers [A to D]						
OVP Threshold During Start-up (until output reaches 1V)			1.2	1.35	1.5	V
OVP Threshold During Start-up (until output reaches 1V)			2.4	2.75	3.0	V
OVP and UVP Operating Threshold[1] Range and Resolution		Relative to VID, 1:1 scaling	50	-	400	mV
			-	50	-	mV
OVP and UVP Operating Threshold[1]		Relative to VID, 2:1 scaling	100		800	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Range and Resolution			-	100	-	
OVP and UVP delay[1]		After exceeding threshold	-	-	150	ns
OVP and UVP threshold Tolerance[1]		For thresholds > 200mV	-20		20	%
OC WARN and FAULT Range[2]		Switcher A and B	0	-	4	A
OC WARN and FAULT Range[2]		Switcher C and D	0	-	8	A
OC WARN and FAULT Range[2]		Switcher C in C+D mode	0	-	15.97	A
OC WARN and FAULT Resolution			-	31.25	-	mA
OC FAULT Threshold Tolerance (0°C to 85°C junction temperature)		At 3A for A and B, 6A for C and D, at 12A for C+D	-10		+10	%
OC FAULT Threshold Tolerance[1] (-40°C to 125°C junction temperature)		At 3A for A and B, 6A for C and D, at 12A for C+D	-20		+20	%
OT WARN and FAULT Range[1]			0		255	°C
OT WARN and FAULT Resolution[1]			-	1	-	°C
Fault Protection - Switcher A with External PowIRstage ®						
OC WARN and FAULT Range[2]			0	-	255	A
OC WARN and FAULT Resolution			-	0.25	-	A
External ISENSE Filter Bandwidth			-	62	-	KHz
Fault Protection - LDO						
OV FAULT		Read Only, % of VOUT as set in ldo_target_register - Non tracking Or measured VIN/2 - Tracking	-	125	-	%
OV WARN			-	112.5	-	%
UV FAULT			-	75	-	%
UV WARN			-	87.5	-	%
OC FAULT		Read Only	-	0.72	-	A
OC WARN Range			0	-	0.72	A
OC WARN Resolution			-	3.9	-	mA
MOSFET - Switcher A and B						
High Side Switch Resistance		Tj = 20°C, BOOT-PHASE = 5V	-	150	-	mΩ
Low Side Switch Resistance		Tj = 20°C, VDRV = 5V	-	45	-	mΩ
MOSFET – Switcher C and D						
High Side Switch Resistance		Tj = 20°C, BOOT-PHASE = 5V	-	85	-	mΩ
Low Side Switch Resistance		Tj = 20°C, VDRV = 5V	-	25	-	mΩ
LDO						
Input Voltage	V_{in_ldo}		1.2	-	5.5	V
Output Voltage	V_{out_ldo}		0.5	-	3.6	V
Dropout Voltage	$V_{dropout\_ldo}$	Iout=0.5A, Tj=125°C	-	-	0.5	V
Output Current	I_{out_ldo}		-	-	0.5	A
Reference Voltage	V_{ref_ldo}	Ta = 25°C	490	500	510	mV
		-40°C<Tj < 85°C	475	500	525	mV
Timing Information						
Automatic Configuration from MTP[1]		Time from POR to end of configuration loaded from NVM to working registers	-	1	-	ms
Isense AMP Automatic Trim Time[1]			-	1	-	ms

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Delay from Enable high to ramp start [1]		Low power mode disabled	-	3	-	µs
Delay from Enable high to ramp start [1]		Low power mode enabled	-	600	-	µs

Notes:

[1] Guaranteed by design.

[2] Actual OC limit (MAX sustained load the VR can handle) is a function of inductor ISAT and system thermal solution. SW A and B limited to 2A max DC load. SW C and D limited to 4A max DC load

TYPICAL APPLICATION DIAGRAMS

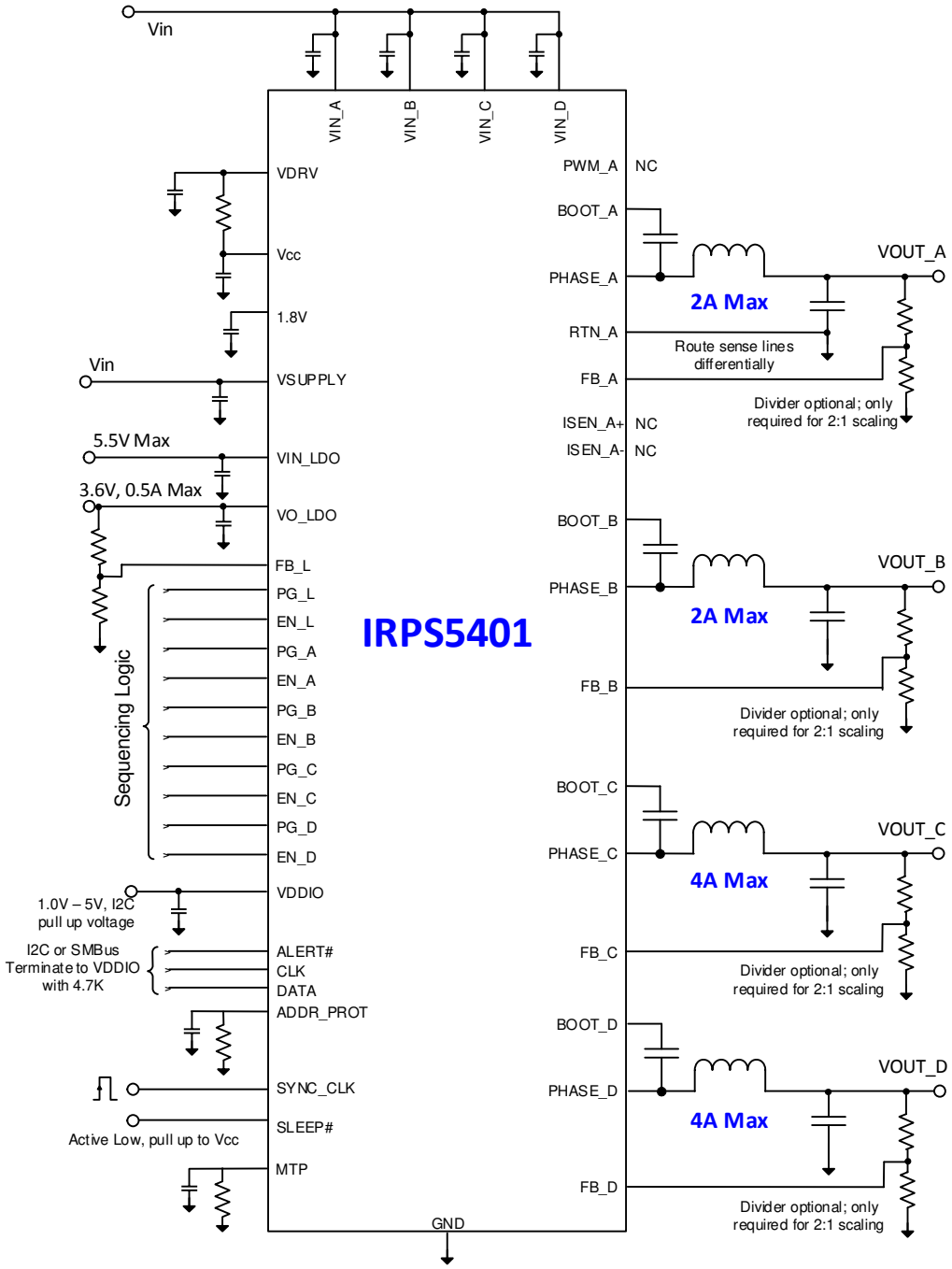


Figure 5: IRPS5401 in 5 output configuration with Vcc from internal LDO

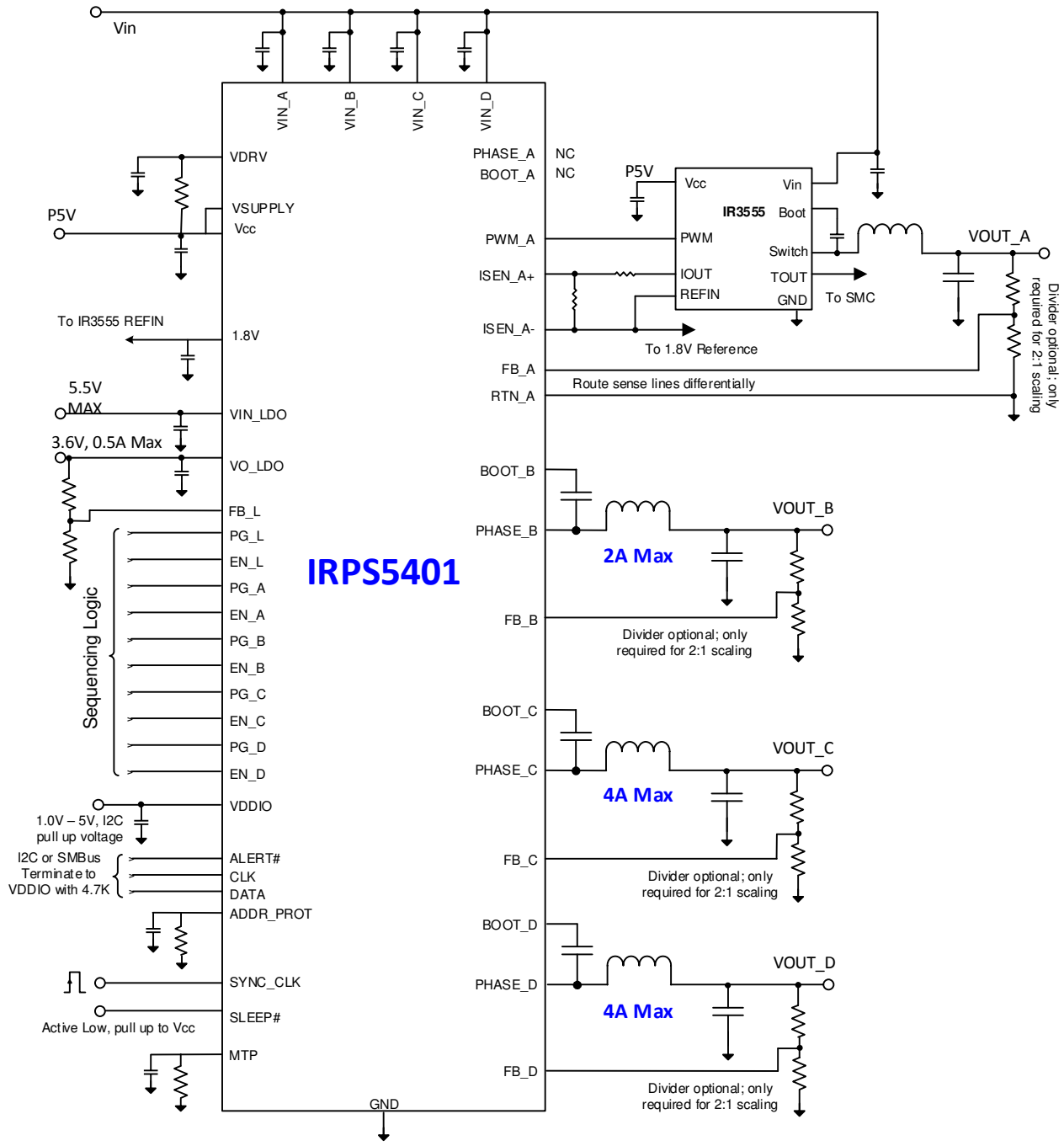


Figure 6: IRPS5401 using external PowIRstage® for high Current Output

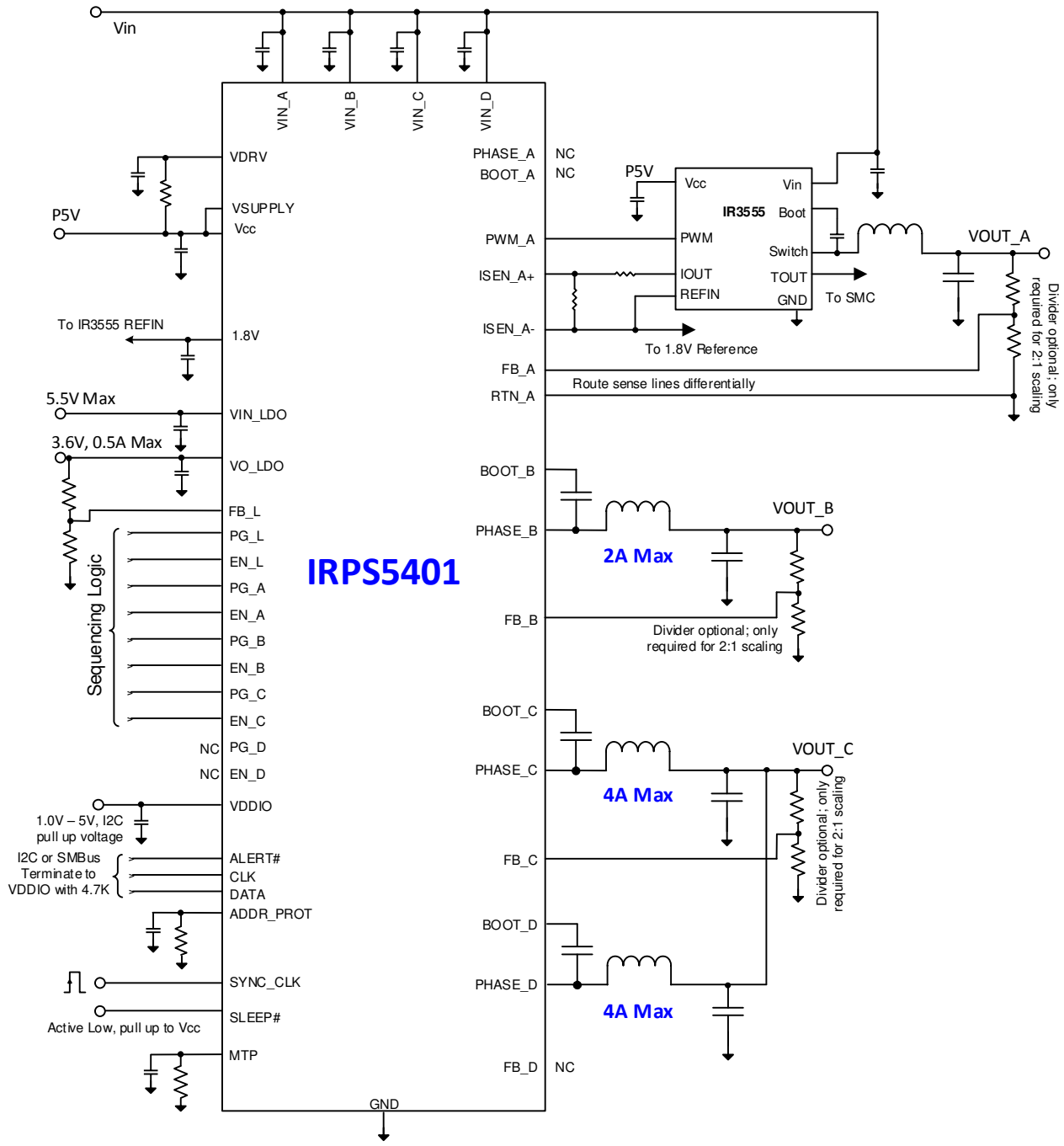
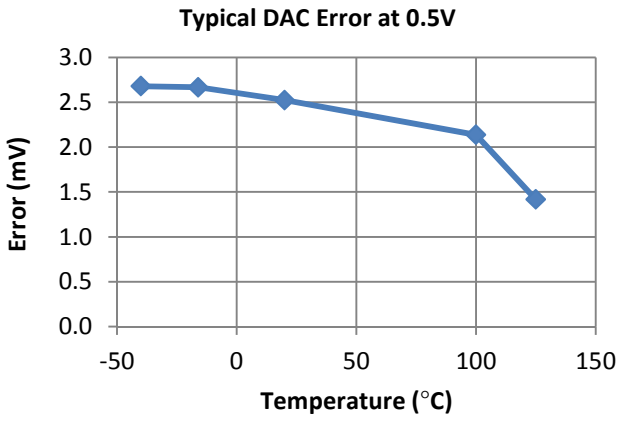
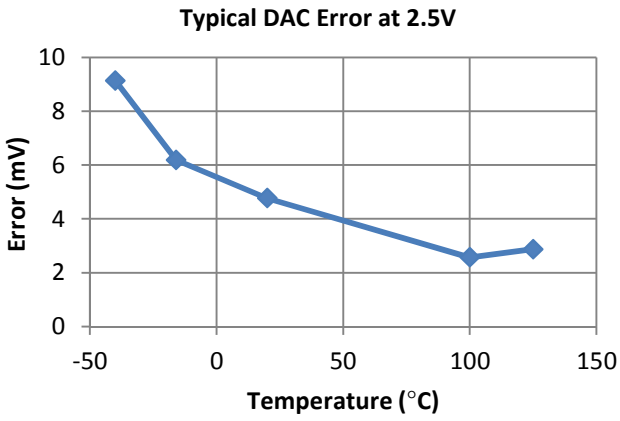


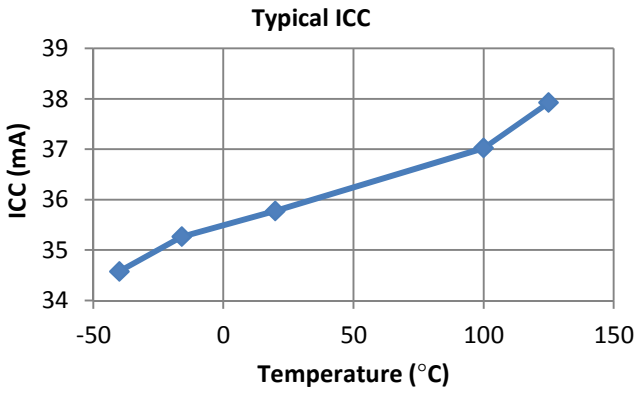
Figure 7: IRPS5401 using Switcher C and Switcher D in parallel for higher current applications

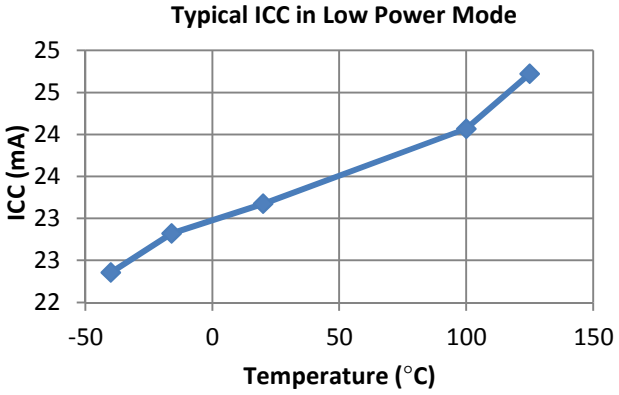
TYPICAL OPERATING CHARACTERISTICS

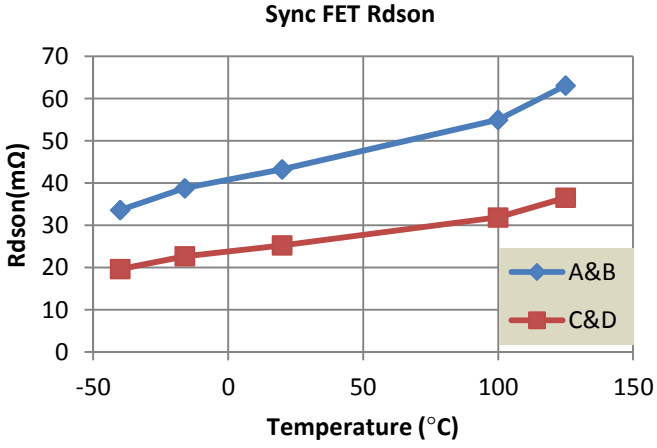
VCC=5V, -40°C to 125°C

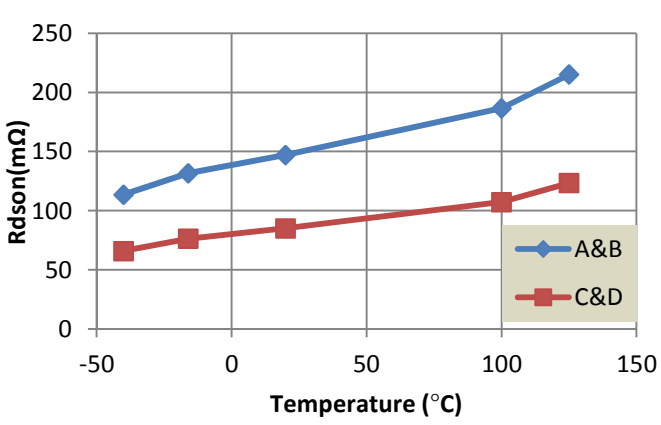












THEORY OF OPERATION

DESCRIPTION

The IRPS5401 is a digitally configurable flexible power management unit, with an I2C/PMBus interface. It can support up to 5 rails, with 4 independent switching regulators and one linear regulator.

The switching frequency is programmable from 200 KHz to 2MHz and provides the capability of optimizing the design in terms of size and performance.

The IRPS5401 switchers provide precisely regulated output voltages programmable from 0.25V to 2.55V without a resistor divider and up to 5.1V with a resistor divider.

The IRPS5401 can operate with an internal bias supply (LDO), typically 5.0V. This allows operation with a single supply by connecting the input of the LDO (VSUPPLY) to the bus voltage (Vin_x). A 1uF capacitor should be used at the VSUPPLY pin for decoupling purposes. The output of this LDO is brought out at the Vcc pin and must be bypassed to the analog ground (pin 50) with a 1.0uF decoupling capacitor. An additional voltage, VDRV, required by the internal driver circuitry is derived by using a 2 ohm-1uF filter from the Vcc pin to the VDRV pin. Note that the 1uF at the VDRV pin must be bypassed to the system power ground (pin 57). The Vcc pin may also be connected to the VSUPPLY pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing for an extended operating bus voltage (Vin_x) range from 1.2V to 14V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as the current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistors.

ONE-TIME PROGRAMMABLE (OTP) MEMORY

The IRPS5401 has 64K of OTP non-volatile memory. The OTP design is based on a patented split-channel non-volatile anti-fuse memory cell. The OTP memory has a data retention rating of 10 years and an operating temperature range of -40°C to 150°C (-55°C to 150°C storage rating)

This memory space is divided up into 20 OTP segments that can be programmed 1 time. The memory space is therefore referred to as Multiple-times Programmable (MTP). This allows the user to; a) change the configuration registers and reprogram the MTP up to 20 times or b) save up to 15 configuration files during initial programing and use the MTP pin to choose which file to load at start up. If option b is used, the remaining unused MTP segments are available for the user to make additional changes to the configuration file and save to MTP using the Rocky GUI device programmer utility.

MTP PIN (PIN 54)

The table below shows the MTP segment that will be selected with a given resistor value connected to the MTP pin. The resistor must be connected to the AGND pin and bypassed with a 10nF X7R type multi-layer ceramic capacitor.

***Do not use these values for applications with ambient temperatures <0°C**

MTP pin Resistor	MTP Segment selected
*0.845KΩ	+0
*1.30KΩ	+1
*1.78KΩ	+2
2.32KΩ	+3
2.87KΩ	+4
3.48KΩ	+5
4.12KΩ	+6
4.75KΩ	+7
5.49KΩ	+8
6.19KΩ	+9
6.98KΩ	+10
7.87KΩ	+11
8.87KΩ	+12
10.00KΩ	+13
11.00KΩ	+14

The number of segments that the user chooses to program with multiple configuration files is set by a configuration register called *max_prog*. The *max_prog* register value needs to be set to the number of configuration files that will be programmed. For example, if the user programs segments +0, +1, and +2, then the *max_prog* register needs to have a value of 3. For applications with junction temperatures below 0°C, segments +0, +1, and +2 are not available.

DEVICE POWER-UP AND INITIALIZATION

During the power-up sequence, when VIN is brought up, the internal LDO converts it to a regulated 5.0V at VCC. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of the VCC pin and the P1V8 pin, and holds the POR low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes an MTP load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use I2C/PMBus to re-configure the registers to suit the specific VR design requirements if desired, irrespective of the status of the enable pins.

In the default configuration, power conversion for a given loop is enabled only when the corresponding En_x pin voltage is asserted high, the Vin_x bus voltage exceeds its under voltage threshold (as stored in the MTP registers and commanded by the PMBus commands VIN_ON and VIN_OFF), the contents of the MTP have been fully loaded into the working registers and the device address has been read. IRPS5401 provides additional options to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus.

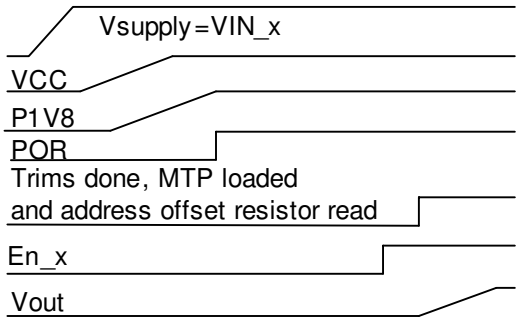


FIGURE 8: Power up sequence

ADDRESSING THE IRPS5401

The IRPS5401 has two 7-bit registers that are used to set the base I2C address and base PMBus address of the device, as follows.

Register	Description	Default
i2c_device_address	The chip I2C address. An address of 0 will disable I2C communication	10h
pmb_device_address	The chip PMBus address. An address of 0 will disable PMBus communication.	40h

Setting another bit, i2c_take_addr_from_ext, to 1, will allow the user to offset the base address of the device using a resistor from ADDR_PROT to AGND. In such a case, the table below provides the resistor values needed to realize up to 15 offsets from the base address. For applications with junction temperatures below 0°C, address offsets of +0, +1, and +2 are not available.

***Do not use these values for applications with ambient temperatures <0°C**

ADDR_PROT Resistor	I2C Address Offset
*0.845KΩ	+0
*1.30KΩ	+1
*1.78KΩ	+2

2.32KΩ	+3
2.87KΩ	+4
3.48KΩ	+5
4.12KΩ	+6
4.75KΩ	+7
5.49KΩ	+8
6.19KΩ	+9
6.98KΩ	+10
7.87KΩ	+11
8.87KΩ	+12
10.00KΩ	+13
11.00KΩ	+14
12.10KΩ	+15

Another bit **i2c_pmb_addr_lock,** if set, allows the user to lock the I2C and PMBus addresses.

SWITCHING FREQUENCY

The switching frequency (Fsw) setting of the IRPS5401 is stored in MTP and can be configured by using the PMBus command FREQUENCY_SWITCH.

The IRPS5401 with will ACK any FREQUENCY_SWITCH command from 200KHz to 2MHz in increments of 1KHz (increments of 2KHz with commands above 1MHz). Internally the command is decoded and the actual FSW is set to the nearest value that can be supported with a 48MHz internal clock. For example, 500KHz can be supported with ninety-six (96) 48MHz clocks. So if you ask for 500KHz, you get exactly 500KHz. But if you wanted 450KHz, the number of clocks required is 106.6667 (48/0.45). In this case, the frequency would be set to one hundred and seven (107) 48MHz clocks or 448.6KHz. Fractional values of 0.5 and above are rounded up to the next whole number.

Because of the enforced phase relationship between the four switching regulators, the switching frequency for all four switching regulators is determined by the FREQUENCY_SWITCH command sent to Switcher C. FREQUENCY_SWITCH commands sent to Switchers A, B, and D will be ACK'd and ignored. A FREQUENCY_SWITCH read command sent to Switchers A, B, or D will respond with the value that the user wrote into the device but the actual switching frequency for Switcher B and D will be the switching frequency of Switcher C. The switching frequency of Switcher A will be the switching of Switcher C if the FREQUENCY_SWITCH value for Switcher A is the same as or greater than Switcher C. The switching frequency of Switcher A will be one half of the switching frequency of Switcher C if the FREQUENCY_SWITCH value for Switcher A is less than Switcher C. The switching frequency of Switcher A will be ½ of Switcher C even when synced to an external CLK. This frequency relationship between Switcher A and Switcher C is the same with Switcher A using internal mode or external power stage mode. Switcher A will have the same switching frequency as Switcher C if Switcher C frequency is less than 400KHz.

Even when running off an internal clock, all four switchers exhibit fixed phase relationships with one another, with Switcher A leading Switcher C by 90^0 which in turn leads loop B by 90^0. Finally loop D lags loop B by 90^0. Thus loops A and B are out of phase by 180^0 as are loops C and D.

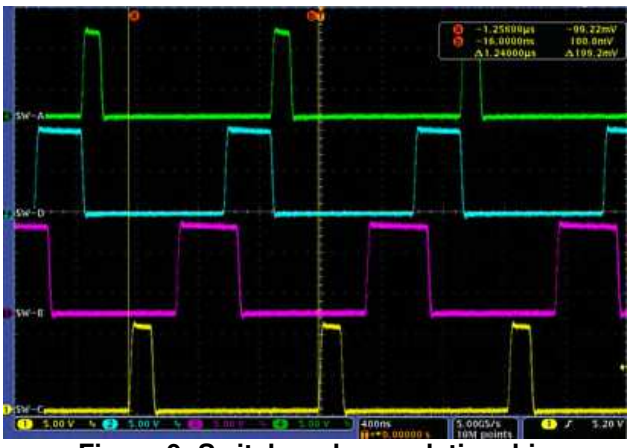


Figure 9: Switcher phase relationship

SYNCHRONIZING TO AN EXTERNAL CLOCK

IRPS5401 implements a frequency lock loop which forces all four switcher loops to operate at the same frequency as an external synchronization clock. The four switchers still maintain the same phase relationships with each other as they do when running from an internal clock. Switcher A shows a small phase offset (~80ns) from the sync clock.

1. If the sync clock is within ± 6.25% of the programmed frequency, the device will phase and frequency lock to the incoming sync clock.
2. If the sync clock is more than ± 12.5% away from the programmed frequency, the device will lose sync and will relax gradually to the programmed frequency.
3. Once the device is in sync, it will have a ±± 10 ns uncertainty or jitter with respect to the sync clock.
4. It takes about 110us for the circuit to lock to the Sync clock.

SWITCHER A IN EXTERNAL POWERSTAGE MODE

Switchers B, C and D can only be operated in internal power stage mode, and their PWM signals are not brought out to a pin. However, using an MTP register bit, sw_a_use_internal_driver, Switcher A can be configured to operate in either internal power stage mode (sw_a_use_internal_driver=1) or in external power stage mode (sw_a_use_internal_driver = 0). In the external power stage mode, the PWM output of Switcher A is brought out to the PWM_A pin and can be connected to the PWM input pin of industry standard tri-state type drivers or Infineon PowIRstage® devices. The logic of operation for the tri-state drivers is depicted in the figure below.

Note that the PWM_A output is tri-stated whenever the Switcher A is disabled, the shut-down ramp has completed or before the soft-start ramp is initiated.

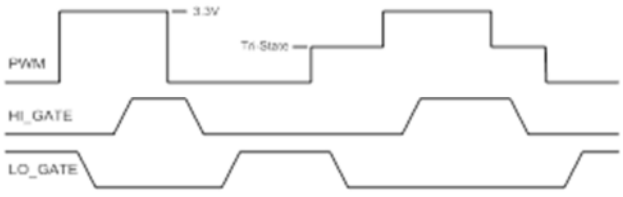


FIGURE 10: PWM_A TRI-STATE DETAILS

DIGITAL CONTROLLER & PWM

For the switcher loops A, B, C and D, Rocky uses a proprietary emulated current mode control scheme, which makes it possible to use PI control to stabilize the loop for all types of inductors and capacitors, including MLCC. The digitized error voltage from the high-speed voltage error ADC is processed by a digital compensator, the proportional (K_p) and Integral (K_i) coefficients, which are programmable. The output of the compensator is then compared with an emulated current signal to generate the PWM signal, with a resolution of 2.6ns to avoid limit cycling. As a close realization to a Type II analog compensator, the control engine also implements a low pass, programmable single pole (K_{pole}) filter. This defaults to 1.1MHz and in general, it should not be necessary to change the location of this pole over a wide range of applications.

Ordinarily, a power stage using low ESR capacitors such as MLCCs requires the use of Type III compensation or PID control, but, in the IRPS5401, the emulated current mode modulator provides another pole-zero pair, unburdening the compensator and allowing a simple PI compensator to stabilize even such demanding applications.

The compensator transfer function is defined as

$$(Kp + \frac{Ki}{s}) \bullet \left(\frac{1}{1 + \frac{s}{\omega p_1}} \right)$$

Where, ωp_1 is the pole typically positioned to filter noise and ripple, and programmable through the register K_{pole1}[3:0]

K_p is the proportional coefficient, programmable through the register k_p[5:0]

And K_i is the integral coefficient programmable through the register k_i[5:0].

DIODE EMULATION / DISCONTINUOUS MODE OPERATION/AOT

Under very light loads, efficiency can become dominated by MOSFET switching losses. Using the manufacturer specific PMBus command MFR_FCCM, it is possible to enhance the light load efficiency by allowing the controller to work in an adaptive on time (AOT) or diode emulation mode.

ADAPTIVE ON-TIME CONTROL PARAMETERS

MTP Register	Function	Default
diode_emu_thresh	Sets the error voltage at which an on-time pulse is started in 2mV steps	0h
diode_emu_pw	Sets the duration of the on-time pulse	4h
de_off_time_adjust	Reduces the calculated low-side FET on-time in 62.5ns steps. Useful for compensating for DrMOS or other drivers' tri-state delay for a better prediction of the zero-crossing	0h
le_th	Error threshold to go from discontinuous conduction mode to continuous conduction mode; 4 mV resolution. If Vout drops by this amount, the control will be handed to PWM and diode-emulation is ended.	1h
Inductor_ni_thresh	Total current threshold below which it is assumed that the inductor current has a negative component.	00h

When the current reading drops below ni_thresh, the controller determines that the inductor current has a negative component, and if MFR_FCCM=0, will allow AOT mode operation. Internal circuitry determines, using diode_emu_pw and the read values of Vinx and Voutx, when the inductor current declines to zero on a cycle by cycle basis and shuts off the low-side MOSFET at the appropriate time in each cycle. This reduces conduction losses and also lowers the switching frequency resulting in improved efficiency because the inductor and low-side MOSFET are not sinking power from the output capacitors at light loads.

In AOT mode, if Vout drops below a certain threshold (le_th) due to applying a fast transient load, the operation is switched to continuous current mode (CCM) instantly.

Industry standard tri-state drivers typically have slow tri-state entry times, which allows negative current to build up reducing efficiency and causing ringing. The *off_time_adjust* variable allows the designer to compensate for the tri-state delay by reducing the low-side FET on-time by an equivalent amount.

OUTPUT VOLTAGE SENSING, TELEMETRY AND FAULTS

The IRPS5401 provides true differential remote sensing for the Switcher A output. The FB_A and RTN_A pins are connected to the load sense pins of the Switcher A output voltage to provide true differential remote voltage sensing with high common-mode rejection. This allows Switcher A (in external power stage mode) to provide excellent regulation even in high current applications. Switcher loops B, C and D have single ended feedback connections for sensing and regulation. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC. This digitized error is used for Vout under voltage fault and warning detection as well as for Vout overvoltage fault warning detection. Vout is reported using the READ_VOUT PMBus command. The reported Vout is the DAC reference value and not the actual measure output voltage

As shown in the figure below, the Vsen and Vrtn inputs have a 20KΩ pull-up to an internal 1V rail. This causes some current flow in the Vsen and Vrtn lines so external impedance should be kept to a minimum to avoid creating an offset in the sensed output voltage.

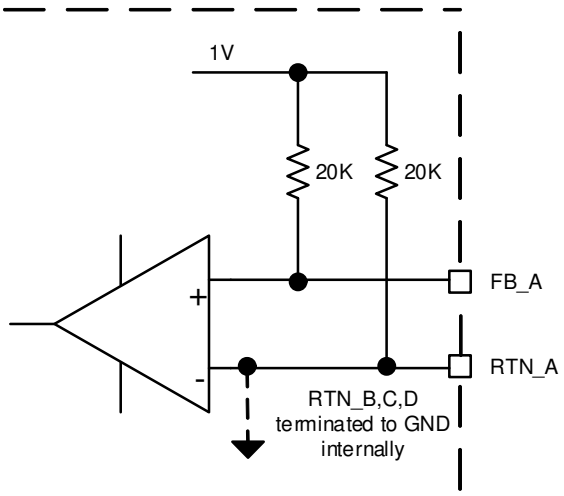


Figure 11: Output Voltage Sensing impedance

Output Over Voltage Protection (OVP)

If the output voltage exceeds a user-programmable (through PMBUS) threshold, the IRPS5401 detects an output over-voltage fault and latches on the low-side MOSFET to limit the output voltage rise

It should be noted, however, that although the overvoltage threshold is programmable to any value using the PMBus command, VOUT_OV_FAULT_LIMIT, internally it is translated into an offset from the commanded or reference voltage, with a resolution of 50 mV (100 mV if a 2:1 divider is used) and with a minimum value of 50 mV (100 mV if a 2:1 divider is used) and maximum value of 400 mV (800 mV if a 2:1 divider is used).

Under OVP conditions, depending on the setting of the VOUT_OV_FAULT_RESPONSE, the converter can be configured to keep regulating or to go into a latched shutdown, where the high side FET or Control FET is turned off and low side FET or Sync FET is turned on. Note however that there is an MTP register, vpu_high_release_en, that allows the low side FET operation to be configured in one of two ways: a) remain latched on indefinitely or b) remain latched on until the output voltage falls below 200mV at which time the low-side FET is released. This release mode can reduce or prevent undershoot of the output voltage.

During soft-start, OVP is triggered at the fixed soft-start level. This level can be chosen, using an MTP register, from two different values of 1.35V or 2.75V respectively. If a 2:1 divider is used, these values automatically scale to 2.7V and 5.5V respectively. In fact, it is this value which limits the maximum output voltage the IRPS5401 can support to 5.5V.

Note that in the FET release mode, if the output voltage rises above the fixed OVP level, the low side MOSFET's will again be turned on until Vout drops below the release threshold level.

The user can cycle out of a latched over voltage fault by cycling En_x, VCC or the PMBus Operation command.

The other output are unaffected by the OVP event unless global_fault_en=1

Figure 12: OVP with vpu_high_release_en=1

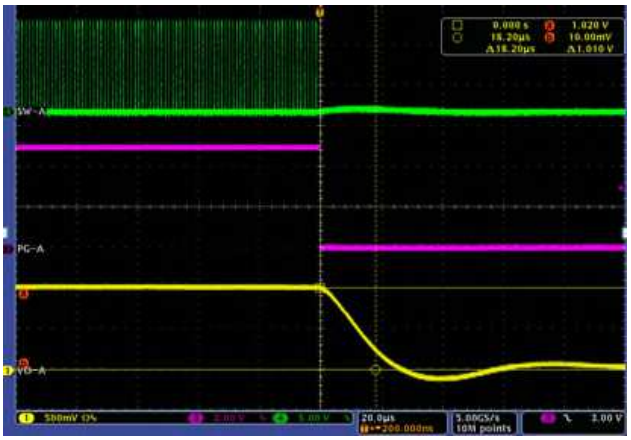


Figure 13: OVP with vpu_high_release_en=0

Output Under Voltage Protection (UVP)

The IRPS5401 detects an output under-voltage condition if the sensed voltage is below the user-programmable (through PMBus) UVP threshold. Upon detecting of an output under-voltage condition, the IRPS5401 can be configured using the PMBus command, VOUT_UV_FAULT_RESPONSE to keep regulating or to go into a latched shutdown.

It should be noted, however, that although the undervoltage threshold is programmable to any value using the PMBus command, VOUT_UV_FAULT_LIMIT, internally the UV threshold depends upon the setting of a register bit, vout_uv_by_adc, which can be set to either 0 (Vout undervoltage mechanism is through an analog comparator) or to 1 (Vout undervoltage mechanism is through the hign speed error ADC saturation).

If the Vout undervoltage mechanism by comparator is selected, the VOUT_UV_FAULT_LIMIT is translated into an offset from the commanded or reference voltage, with a resolution of 50 mV (100 mV if a 2:1 divider is used) and with a minimum value of 50 mV (100 mV if a 2:1 divider is used) and maximum value of 400 mV (800 mV if a 2:1 divider is used).

On the other hand, if the ADC saturation mechanism is selected, the undervoltage threshold is implicitly 250 mV (500 mV if a 2:1 divider is used) below the commanded or reference value.

The user can cycle out of a latched under voltage fault by cycling Enable, VCC or the PMBus Operation command.

CURRENT SENSING, TELEMETRY AND FAULTS

The IRPS5401 has two different current sense mechanisms; a) Sync FET Rdson current sensing in internal powerstage mode and b) DCR, shunt current sensing, or Rdson sense in external powerstage mode.

a) Current sensing for Switchers B, C and D is always across the Rdson of the Sync FET. Current sensing for Switcher A is also across the Sync FET Rdson if in internal powerstage mode. A proprietary patented scheme allows reconstruction of the average inductor current from the voltage sensed across the Sync FET Rdson. It should be noted here that in internal powerstage mode it is this reconstructed average inductor current that is digitized by the monitor ADC and used for output current reporting. However, in this mode, the overcurrent protection mechanism relies on an analog comparator and does not depend on the ADC or on the output current reporting.

b) If Switcher A is operated in external powerstage mode, the current is sensed through the drop across a precision current shunt, the drop across the inductor DCR, or the IOUT signal of an Infineon Rdson powIRstage ® like the IR3555 and is fed to a differential current sense amplifer at the ISEN_A+ and ISEN_A- pins of the IRPS5401.

For DCR sensing, a suitable resistor-capacitor network of R_{sen} and C_{sen} is connected across the inductor as shown in the figure below. The time constant of this RC network is set to be equal to the inductor time constant (L/DCR) such that the voltage across the capacitor C_{sen} is equal to the voltage across the inductor DCR. A 100K NTC thermistor is also recommended across C_{sen} to compensate for the positive temperature coefficient of inductor DCR

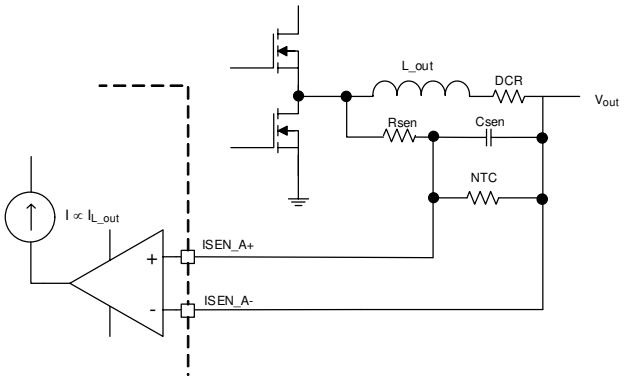


Figure 14: DCR Current Sensing

The recommended value for C_{sen} is a 220nF NPO type capacitor.

$$Rsen = (L\_out) / (DCR * Csen)$$

For example, if L_out is a 1uH, 2mΩ inductor, then Rsen would be set to 5KΩ (with Csen = 0.1uF)

These components must be placed close to the IRPS5401 pins.

For Rdson current sense, the signal from the powIRstage® IOUT pin is reporting IOUT with a gain of 5mV/A. This signal should be attenuated with a 5:1 divider so that the input to the ISENSE amp is 1mV/A. For noise immunity reasons, the differential ISENSE signal is offset above GND by connecting the ISEN_A- pin to a reference voltage. This is usually the 1.8V reference provided by the internal 1.8V LDO

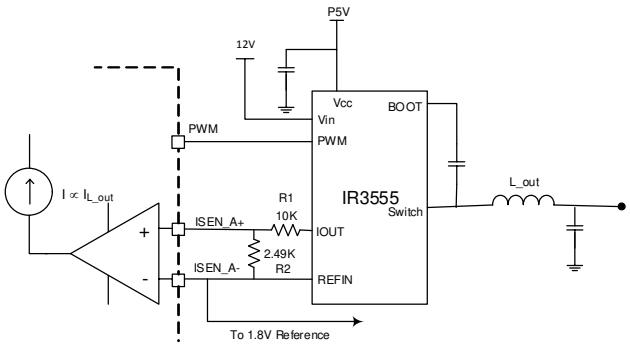


Figure 15: Rdson Current Sensing

The output of this differential current sense amplifier, the gain of which is programmable through an MTP register d2a_ecs_gain [2:0], is digitized by the monitor ADC. The output code of the ADC is then converted using the MTP register ecs_scale [7:0] into output current (in Amps), which is reported on the bus and also used for overcurrent fault detection.

Current is reported using the READ_IOUT PMBus command.

Over-current Protection (OCP)

In internal powerstage mode, the over current (OC) protection is implemented by sensing current through the $R_{DS(on)}$ of the Synchronous MOSFET (Sync FET). This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and eliminates any layout related noise issues. The current limit scheme in the IRPS5401 uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Sync FET. As a result, the over-current trip threshold remains almost constant over temperature. Moreover, the IRPS5401 also incorporates Vgs compensation that limits the OCP variation with changes in VCC voltage.

The OCP circuit samples the current at the center point of the Sync FET conduction time, and trips the analog overcurrent comparator if it is more than the overcurrent protection setting as dictated by the PMBus command IOUT_OC_FAULT_LIMIT. Although the PMBus comand will allow setting the OC threshold up to a maximum of 15.97A (for internal driver), the internal circuitry saturates the current limit at 4A for Switchers A and B with the 2A internal power stages and to 8A for Switchers C and D with the 4A power stages. Moreover, the threshold set by the PMBus command is rounded to the closest higher 250 mA for the 2A power stages and to the closest higher 500 mA for the 4A power stages.

In external power stage mode, an over current fault is flagged when the digital reading of the output current exceeds IOUT_OC_FAULT_LIMIT.

Additionally, through the PMBus command IOUT_OC_FAULT_RESPONSE, the user can choose between 3 types of responses to an overcurrent fault.

OCP Response Mode
Immediate shutdown and then latch off
Immediate shutdown and retry 6 times before latching off, 22msec period
Immediate shutdown and retry indefinitely, 22msec period

The user can cycle out of a latched over current fault by cycling En_x, VCC, VINx, or the PMBus OPERATION command (with correct ON_OFF_CONFIG setting).

Additionally, in both the internal and external power stage modes, an over current warning is flagged if the digital reading of the output current exceeds IOUT_OC_WARN_LIMIT.

INPUT VOLTAGE SENSING, TELEMETRY AND FAULTS

For the switchers, the input voltage is fed through a 14:1 divider to a monitor ADC. The digitized voltage is reported over the PMBus using the READ_VIN command. It is also used to implement an input under voltage lockout threshold, an input voltage warning threshold and an input voltage over voltage threshold through the following PMBus commands

Function	PMBus Command	Default
UVLO	VIN_ON	F001h
	VIN_OFF	F000h
Under voltage warning	VIN_UV_WARN_LIMIT	E000h
Overvoltage	VIN_OV_FAULT_LIMIT	E200h

fault		

Additionally, through the PMBus command VIN_OV_FAULT_RESPONSE, the user can choose between 2 types of responses

VIN OV Response Mode
Ignore
Immediate shutdown and then latch off

The user can cycle out of a latched VIN Overvoltage fault by cycling En_x, VCC, or the PMBus Operation command.

DIE TEMPERATURE SENSING, TELEMETRY AND FAULTS

The IRPS5401 uses on-die temperature sensing for accurate temperature reporting and over temperature detection. Also, to account for temperature gradients across the die, temperature sensing is actually done by two separate sense circuits at different locations on the die. So, Switchers A and B share one temperature sensor, while Switchers C and D as well as the LDO share another temperature sensor. Therefore, the READ_TEMPERATURE PMBus command reports the same temperature on Switchers A and B. Also, Switchers C and D as well as the LDO report the same temperature. The reporting resolution is 0.250°C.

PMBus commands OT_FAULT_LIMIT and OT_WARN_LIMIT allow the user to set the over temperature fault and warning thresholds respectively.

Additionally, through the PMBus command OT_ _FAULT_RESPONSE, the user can choose between 3 types of responses to an over temperature fault, i.e., when the digital reading of the temperature exceeds OT_FAULT_LIMIT.

OT Response Mode
Ignore
Immediate shutdown and then latch off
Auto restart if fault condition disappears

The user can cycle out of a latched over temperature fault by cycling En_x, VCC or the PMBus Operation command.

POWER SEQUENCING AND GLOBAL FAULTS

The IRPS5401 provides flexibility in sequencing the startup and shutdown of the five outputs via the following PMBus commands:

Output	Sequencing Function	PMBus command	Default
Switchers A,B,C and D	Startup	TON_DELAY	F800h
		TON_RISE	F004h
	shutdown	TOFF_DELAY	F800h
		TOFF_FALL	F004h
LDO	startup	TON_DELAY	F800h

The figure below shows the four outputs starting up and shutting down with each output delayed 0.5ms from the previous.

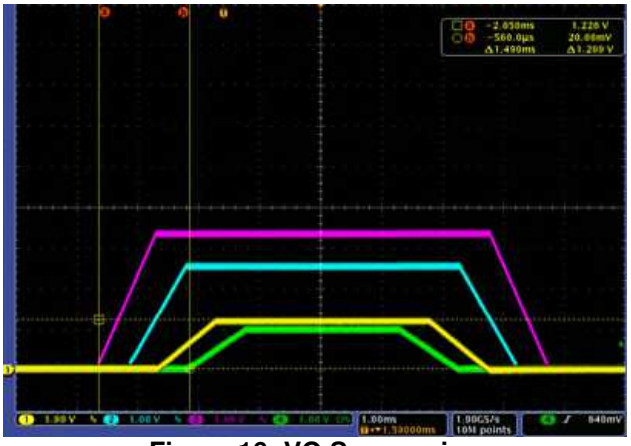


Figure 16: VO Sequencing

An extra level of flexibility in sequencing the different outputs is provided by the Global Faults feature in IRPS5401. This is a useful feature that forces all 5 rails to shut down in response to a fault that shuts down any one of the rails. This is enabled by setting an MTP register bit global_fault_en. The figure below shows the response of all the IRPS5401 outputs in response to a shutdown of Switcher A by an output over voltage fault when global_fault_en=1, enabling global fault shutdown and global_fault_en=0, disabling global fault shutdown.