Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

International
IOR Rectifier

April 21st, 2008

IRS21571D
FULLY INTEGRATED BALLAST CONTROL IC

IC Features

- Programmable preheat time and frequency
- Programmable ignition ramp
- Protection from failure-to-strike
- Lamp filament sensing and protection
- Protection from operation below resonance -
- 0.2V CS threshold sync'd to falling edge on LO
- Protection from low-line condition
- Automatic restart for lamp exchange
- Thermal overload protection
- Programmable deadtime
- Integrated 600V level-shifting gate driver
- Integrated bootstrap MOSFET
- Integrated 15.6V zener clamp diode on VCC
- Low micro-power start-up
- Latch immunity and ESD on all pins

Typical Application

- Fluorescent lamp ballast

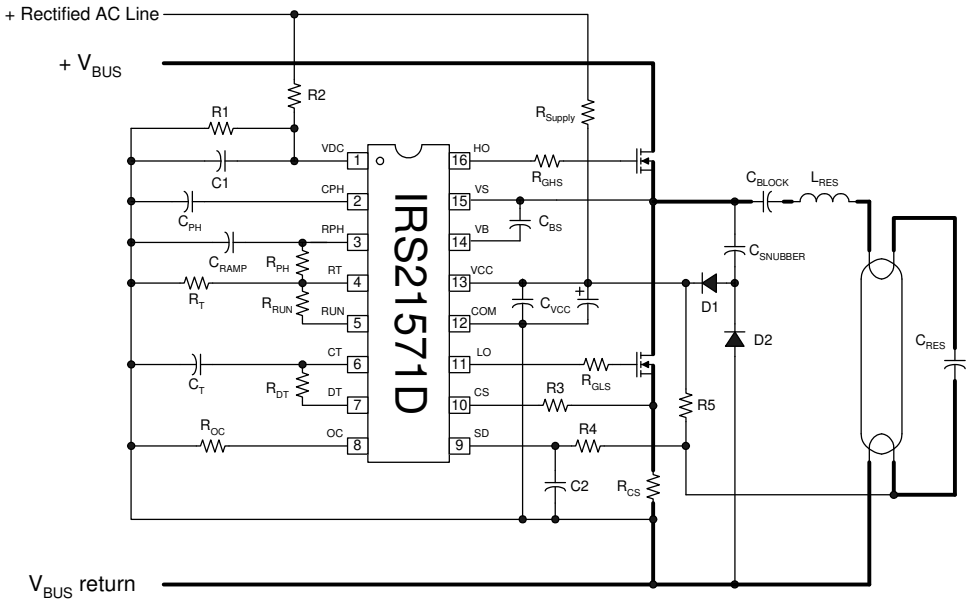
Product Summary

Topology	Half-Bridge
V_{OFFSET}	600 V
I_{O+} & I_{O-} (typical)	180 mA & 260 mA
Oscillator Frequency	+/- 5%
Start-up current (typical)	150 µA

Package Options

16-Lead SOIC (Narrow Body)

Typical Connection Diagram



Description

The IRS21571D is a fully integrated, fully protected 600V ballast control IC designed to drive virtually all types of rapid start fluorescent lamp ballasts. Externally programmable features such as preheat time and frequency, ignition ramp characteristics, and running mode operating frequency provide a high degree of flexibility for the ballast design engineer. Comprehensive thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of this control IC is a variable frequency, 50% duty cycle oscillator with externally programmable deadtime. An integrated bootstrap MOSFET is also included to supply the high-side gate drive circuitry. The IRS21571D is available in 16 pin narrow body SOIC package.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC16N	MSL2††† (per IPC/JEDEC J-STD-020)
ESD	**Machine Model**	Class C (per JEDEC standard EIA/JESD22-A115)	
	Human Body Model	Class 3A (per EIA/JEDEC standard JESD22-A114)	
IC Latch-Up Test		Class , Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	V
V_{HO}	High-Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	V
V_{LO}	Low-Side Output Voltage	-0.3	V_{CC} + 0.3	V
I_{OMAX}	Maximum Allowable Output Current (Either Output) Due to External Power Transistor Miller Effect	-500	500	mA
I_{RT}	RT Pin Current	-5	5	mA
V_{CT}	CT Pin Voltage	-0.3	5.5	V
V_{DC}	VDC Pin Voltage	-0.3	V_{cc} + 0.3	V
I_{CPH}	CPH Pin Current	-5	5	mA
I_{RPH}	RPH Pin Current	-5	5	mA
I_{RUN}	RUN Pin Current	-5	5	mA
I_{DT}	Deadtime Pin Current	-5	5	mA
V_{CS}	Current Sense Pin Voltage	-0.3	5.5	V
I_{CS}	Current Sense Pin Current	-5	5	mA
I_{OC}	Over-Current Threshold Pin Current	-5	5	mA
I_{SD}	Shutdown Pin Current	-5	5	mA
I_{CC}	Supply Current†	-20	20	mA
dV/dt	Allowable Offset Voltage Slew Rate	-50	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25ºC$ (16-Pin DIP)	---	1.60	W
P_D	Package Power Dissipation @ $T_A \leq +25ºC$ (16-Pin SOIC)	---	1.25	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (16-Pin DIP)	---	75	ºC/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (16-Pin SOIC)	---	100	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	---	300	

† This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High Side Floating Supply Voltage	V_{BSUV+}	V_{CLAMP}	V
V_S	Steady State High Side Floating Supply Offset Voltage	-3.0	600	V
V_{CC}	Supply Voltage	V_{CCUV+}	V_{CLAMP}	V
I_{CC}	Supply Current	†	10	mA
V_{DC}	VDC Pin Voltage	0	V_{CC}	V
C_T	CT Pin Capacitance	220	---	pF
R_{DT}	Deadtime Resistance	1.0	---	kΩ
R_{OC}	Over-Current (CS+) Threshold Programming Resistance	---	50	kΩ
I_{RT}	R_T Pin Current ††	-500	-50	µA
I_{RPH}	R_{PH} Pin Current ††	0	450	µA
I_{RUN}	RUN Pin Current ††	0	450	µA
I_{SD}	Shutdown Pin Current	-1	1	mA
I_{CS}	Current Sense Pin Current	-1	1	mA
T_J	Junction Temperature	-40	125	ºC

† Enough current should be supplied into the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage.

†† Due to the fact that the RT input is a voltage-controlled current source, the total RT pin current is sum of all of the parallel current sources connected to that pin. For optimum oscillator current mirror performance, this total current should be kept between 50µA and 500µA. During the preheat mode, the total current flowing out of the RT pin consists of the RPH pin current plus the current due to the RT resistor. During the run mode, the total RT pin current consists of the RUN pin current plus the the current due to the RT resistor.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T=16.9kΩ, C_T = 470 pF, R_{PH} and RUN pins no connection, V_{CPH} = 0V, R_{DT} = 6.1 kΩ, R_{OC} = 20.0 kΩ, V_{CS} = 0.5 V, V_{SD} = 0 V, C_L = 1000pF and T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	11.5	12.5	13.5	V	V_{CC} rising from 0V
V_{UVHYS}	V_{CC} Supply Undervoltage Lockout Hysteresis	---	2.0	---		
I_{QCCUV}	UVLO Mode Quiescent Current	---	150	300	µA	V_{CC} = V_{CCUV+} - 100mV
I_{QCCFLT}	Fault-Mode Quiescent Current	---	400	600		SD = 5V, CS = 2V, or Tj > T_{SD}
I_{QCC}	Quiescent VCC Supply Current		2	4.3	mA	CT connected to COM
I_{QCC40k}	VCC Supply Current, f = 40kHz	4.0	5.5	7.0		
V_{CLAMP}	V_{CC} Zener Clamp Voltage	---	15.6	---	V	I_{CC} = 5mA
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} Supply Current	---	50	100	uA	V_{HO} = V_S
I_{QBS1}	Quiescent V_{BS} Supply Current	---	72	140		V_{HO} = V_B
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	---	9.0	---	V	V_{BS} rising from 0V
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	---	8.0	---		V_{BS} falling from 14V
I_{LK}	Offset Supply Leakage Current	---	---	50	µA	V_B = V_S = 600V
Oscillator I/O Characteristics						
f_{OSC}	Oscillator Frequency	43.7	46	48.3	kHz	
d	Oscillator Duty Cycle		50		%	
V_{CT+}	Upper C_T Ramp Voltage Threshold	---	4.0	---	V	
V_{CT-}	Lower C_T Ramp Voltage Threshold	---	2.0	---		
V_{CTFLT}	Fault-Mode C_T Pin Voltage	---	0	---	mV	SD = 5V, CS = 2V, or Tj > T_{SD}
V_{RT}	RT Pin Voltage	---	2.0	---	V	
V_{RTFLT}	Fault-Mode R_T Pin Voltage	---	0	---	mV	SD = 5V, CS = 2V, or Tj > T_{SD}
tdlo	LO Output Deadtime	---	2.3	---	µsec	
tdho	HO Output Deadtime	---	2.3	---	µsec	
Preheat Characteristics						
I_{CPH}	CPH Pin Charging Current			0.98	µA	V_{CPH} = 0V
V_{CPHIGN}	CPH Pin Ignition Mode Threshold Voltage	3.7	4.0	4.3	V	
V_{CPHRUN}	CPH Pin Run Mode Threshold Voltage	4.6	5.0	5.4		
V_{CPHFLT}	Fault-Mode CPH Pin Voltage	---	0	---	mV	SD = 5V, CS = 2V, or Tj > T_{SD}

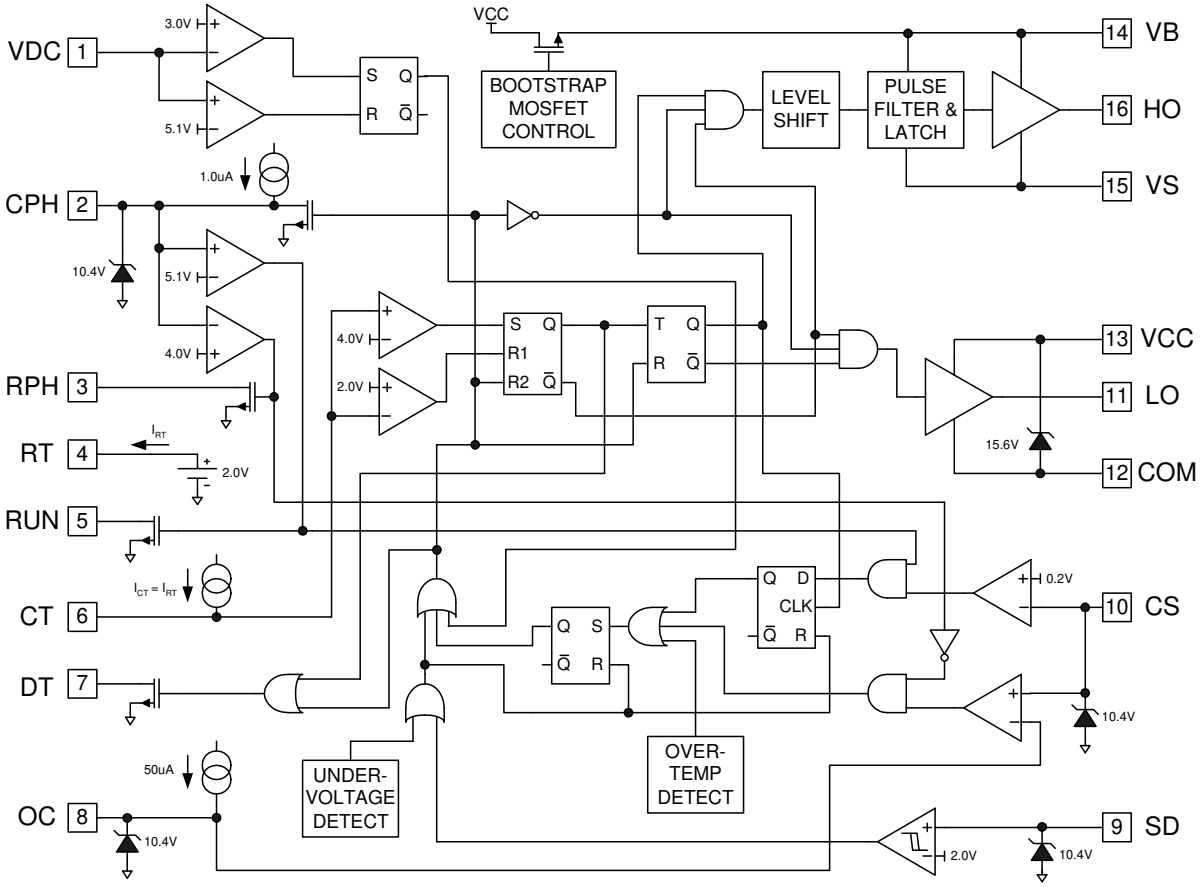
Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T=16.9kΩ, C_T = 470 pF, R_{PH} and RUN pins no connection, V_{CPH} = 0V, R_{DT} = 6.1 kΩ, R_{OC} = 20.0 kΩ, V_{CS} = 0.5 V, V_{SD} = 0 V, C_L = 1000pF and T_A = 25 °C unless otherwise specified.

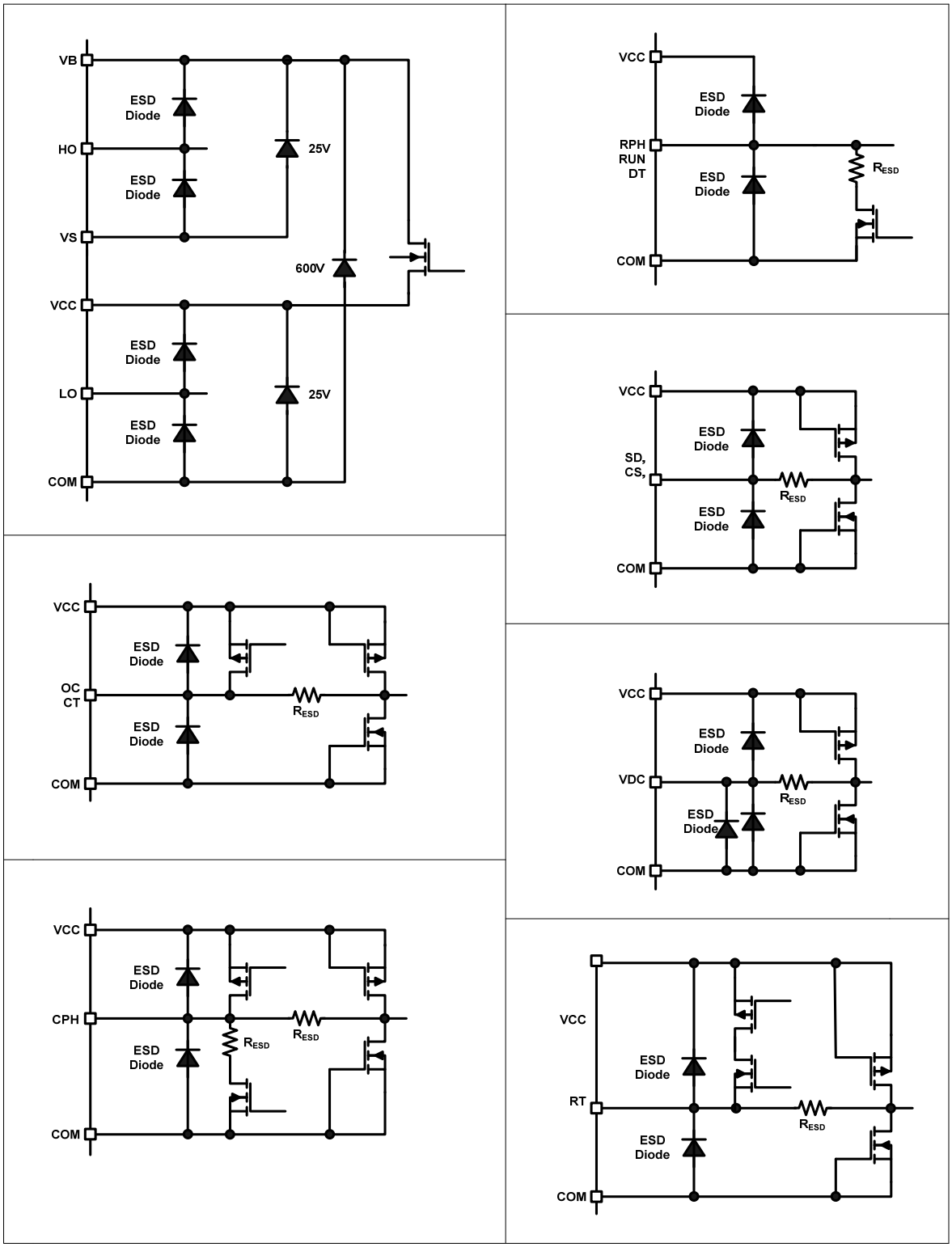
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
RPH Characteristics						
I_{RPHLK}	Open Circuit RPH Pin Leakage Current	---	---	0.1	µA	V_{RPH} = 5V, V_{PH} = 6V
V_{RPHFLT}	Fault-Mode RPH Pin Voltage	---	---	50	mV	SD = 5V, CS = 2V, or Tj > T_{SD}
RUN Characteristics						
I_{RUNLK}	Open Circuit RUN Pin Leakage Current	---	---	0.1	µA	V_{RUN} = 5V
V_{RUNFLT}	Fault-Mode RUN Pin Voltage	---	0	---	mV	SD = 5V, CS = 2V, or Tj > T_{SD}
Protection Circuitry Characteristics						
V_{SD+}	Rising Shutdown Pin Threshold Voltage	2.0	2.2	2.4	V	
V_{SDHYS}	Shutdown Pin Threshold Hysteresis	270	395	520	mV	
V_{CS+}	Over-Current Sense Threshold Voltage	0.99	1.1	1.21	V	
V_{CS-}	Under-Current Sense Threshold Voltage	0.15	0.2	0.26	V	
t_{cs}	Over-Current Sense Propagation Delay		250	400	nsec	Delay from CS to LO
V_{DC+}	Low V_{BUS}/Rectified Line Input Upper Threshold	5.0	5.2	5.6	V	
V_{DC-}	Low V_{BUS}/Rectified Line Input Lower Threshold	2.8	3.1	3.4	V	
T_{SD}	Thermal Shutdown Junction Temperature	---	160	---	ºC	†
Gate Driver Output Characteristics						
V_{OL}	Low-Level Output Voltage		0	100	mV	I_O = 0
V_{OH}	High-Level Output Voltage		0	100		V_{BIAS} - V_O , I_O = 0
t_r	Turn-On Rise Time		120	220	nsec	
t_f	Turn-Off Fall Time		50	220		
I_{O+}	Output source current	---	180	---	mA	
I_{O-}	Output sink current	---	260	---		

† When the IC senses an overtemperature condition (T_j > 175ºC), the IC is latched off. In order to reset this Fault Latch, the SD pin must be cycled high and then low, or the V_{CC} supply to the IC must be cycled below the falling undervoltage lockout threshold (V_{CCUV-}).

Functional Block Diagram



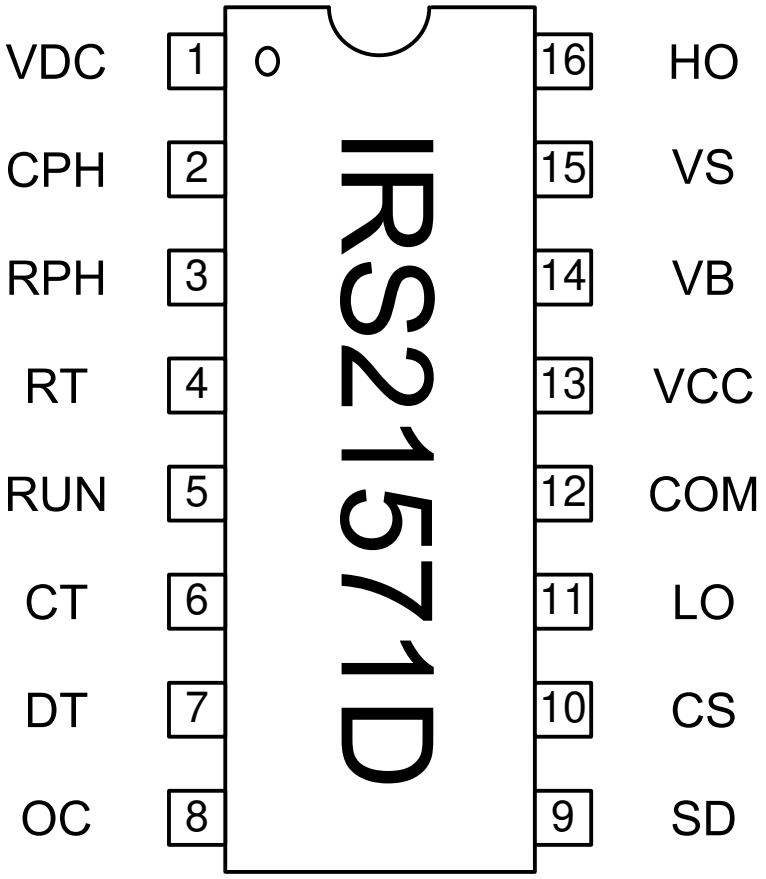
Input/Output Pin Equivalent Circuit Diagrams



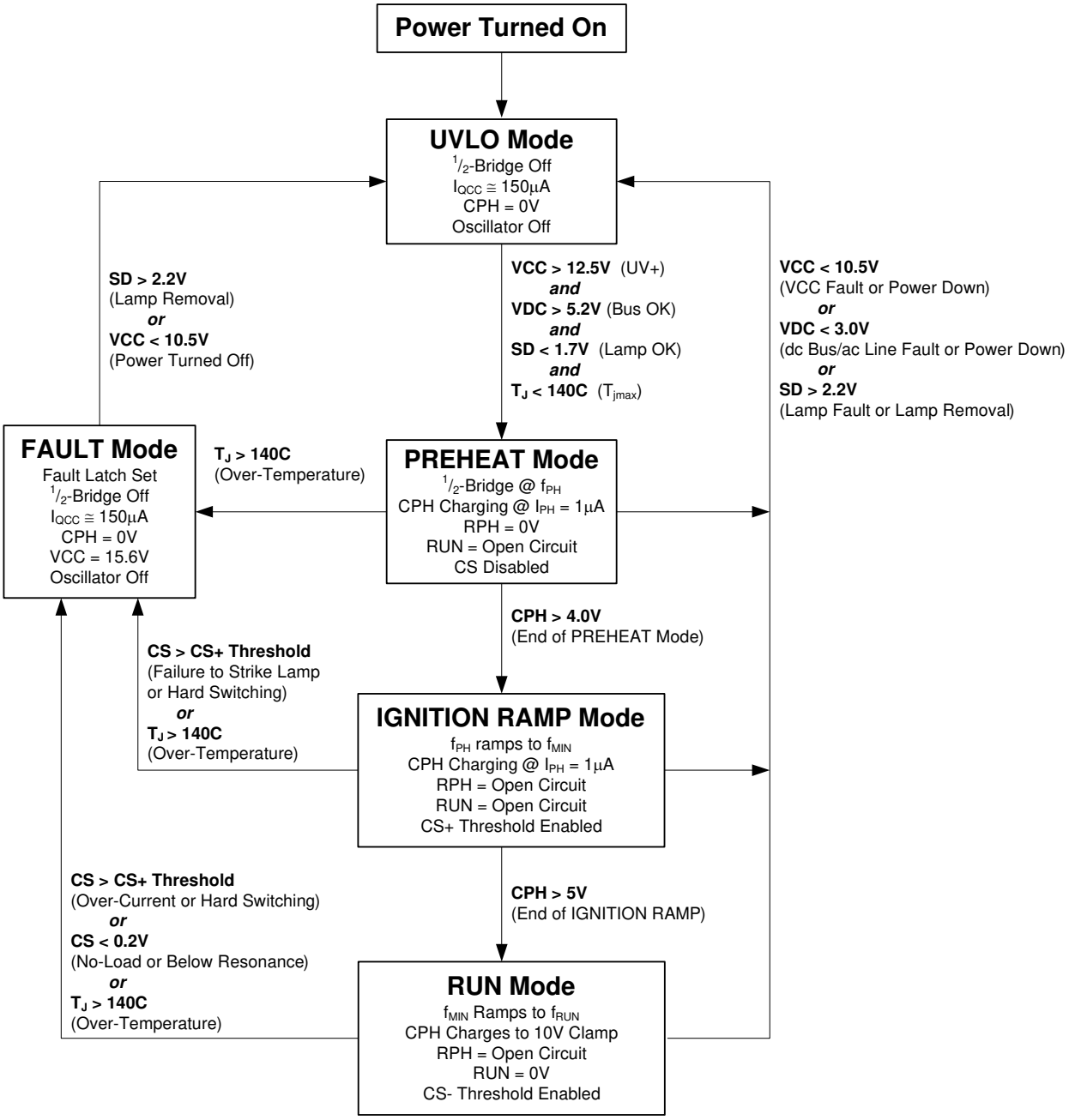
Lead Definitions

Symbol	Description
VDC	DC Bus Sensing Input
CPH	Preheat Timing Capacitor
RPH	Preheat Frequency Resistor & Ignition Capacitor
RT	Oscillator Timing Resistor
RUN	Run Frequency Resistor
CT	Oscillator Timing Capacitor
DT	Deadtime Programming
OC	Over-current (CS+) Threshold Programming
SD	Shutdown Input
CS	Current Sensing Input
LO	Low-Side Gate Driver Output
COM	IC Power & Signal Ground
VCC	Logic & Low-side Gate Driver Floating Supply
VB	High-Side Gate Driver Floating Supply
VS	High Voltage Floating Return
HO	High-Side Gate Driver Outpur

Lead Assignments



State Diagram



Application Information and Additional Details

Supply Bypassing and PCB Layout Rules

Component selection and placement on the pc board is extremely important when using power control ICs. V_{CC} should be bypassed to COM as close to the IC terminals as possible with a low ESR/ESL capacitor, as shown in Figure 1 below.

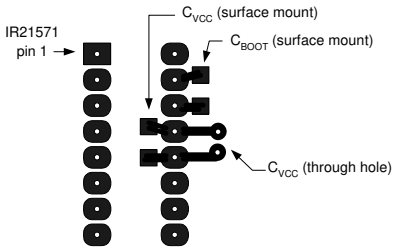


Figure 1: Supply bypassing PCB layout example

A rule of thumb for the value of this bypass capacitor is to keep its minimum value at least 2500 times the value of the total input capacitance (Ciss) of the power transistors being driven. This decoupling capacitor can be split between a higher valued electrolytic type and a lower valued ceramic type connected in parallel, although a good quality electrolytic (e.g., 10μF) placed immediately adjacent to the VCC and COM terminals will work well.

In a typical application circuit, the supply voltage to the IC is normally derived by means of a high value startup resistor (1/4W) from the rectified line voltage, in combination with a charge pump from the output of the half-bridge. With this type of supply arrangement, the internal 15.6V zener clamp diode from VCC to COM will determine the steady state IC supply voltage.

Connecting the IC Ground (COM) to the Power Ground

Both the low power control circuitry and low side gate driver output stage grounds return to this pin within the IC. The COM pin should be connected to the bottom terminal of the current sense resistor in the source of the low side power MOSFET using an individual pc board trace, as shown in Figure 2. In addition, the ground return path of the timing components and V_{CC} decoupling capacitor should be connected directly to the IC COM pin, and not via separate traces or jumpers to other ground traces on the board.

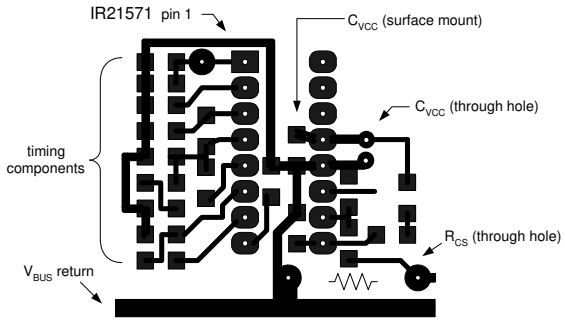


Figure 2: COM pin connection PCB layout example

These connection techniques prevent high current ground loops from interfering with sensitive timing component operation, and allows the entire control circuit to reject common-mode noise due to output switching.

The Control Sequence and Timing Component Selection

The IRS21571D uses the following control sequence (Figure 3) to drive rapid start fluorescent lamps.

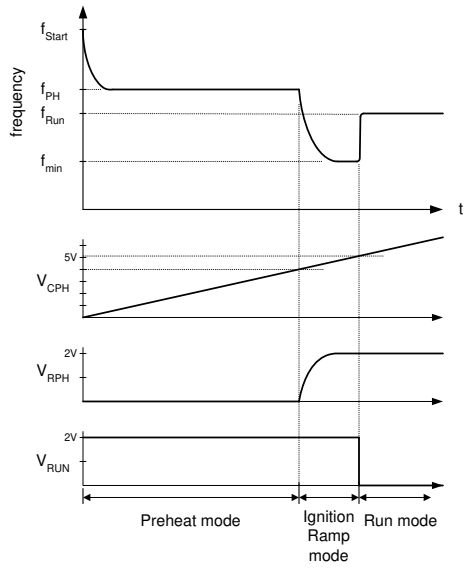


Figure 3: IRS21571D Control sequence

The control sequence used in the IRS21571D allows the **Run Mode** operating frequency of the ballast to be higher than the ignition frequency (i.e., $f_{start} > f_{ph} > f_{run} > f_{ign}$). This control sequence is recommended for lamp types where the ignition frequency is too close to the run frequency to ensure proper lamp striking for all production resonant LC component tolerances (please note that it is possible to use the IRS21571D in systems where $f_{start} > f_{ph} > f_{ign} > f_{run}$, simply by leaving the RUN pin open).

Six pins in the IC are used to control the **Startup, Preheat, Ignition Ramp,** and **Run** modes of operation, and to allow ballast and lamp engineers the flexibility to optimize their designs for virtually any lamp type.

The heart of this controller is an oscillator which resembles those found in many popular PWM voltage regulator ICs. In its simplest form, this oscillator consists of a timing resistor and capacitor connected to ground. The voltage across the timing capacitor C_T is a sawtooth, where the rising portion of the ramp is determined by the current in the R_T pin, and the falling portion of the ramp is determined by an external deadtime resistor R_{DT}. The oscillograph in Figure 4 illustrates the relationship between the oscillator capacitor waveform and the gate driver outputs.

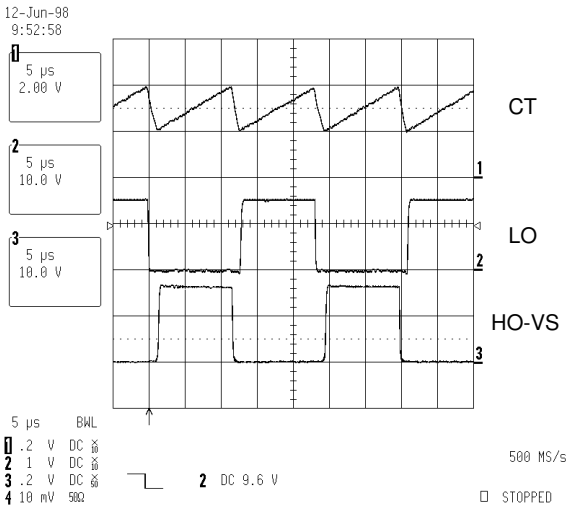


Figure 4

The deadtime can be programmed by means of the external R_{DT} resistor, given a certain range of C_T capacitor values, using the graph shown in Figure 5.

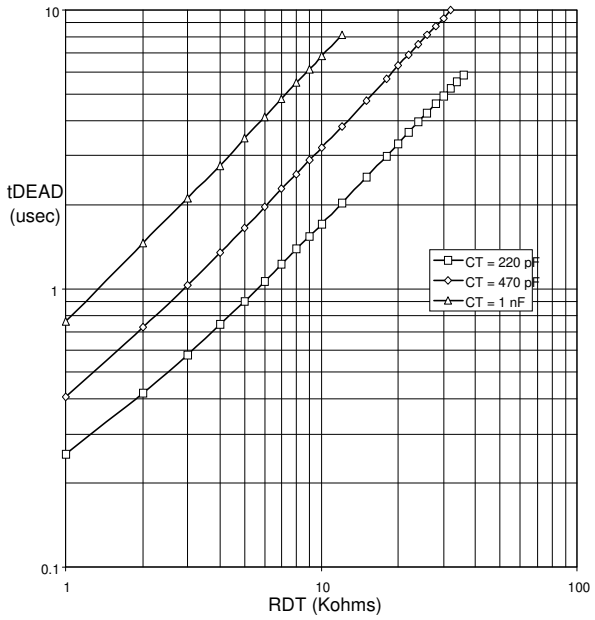


Figure 5: Deadtime versus R_{DT}

The R_T input is a voltage-controlled current source, where the voltage is regulated to be approximately 2.0V. In order to maintain proper linearity between the R_T pin current and the C_T capacitor charging current, the value of the R_T pin current should be kept between 50µA and 500µA. The R_T pin can also be used as a feedback point for closed loop control.

During the **Startup Mode**, the operating frequency is determined by the parallel combination of R_{PH} and R_T , combined with the values of C_T and R_{DT} , and the voltage at the R_T pin, as shown in Figure 6. The voltage at the R_T pin starts at an initial value above 2V, causing the initial start frequency to be higher than the preheat frequency. This frequency is high enough to ensure that the instantaneous voltage across the lamp during the first few cycles of operation does not exceed the strike potential of the lamp. As the voltage at the R_T pin decreases to the final value of 2V, the output frequency ramps down to the preheat frequency.

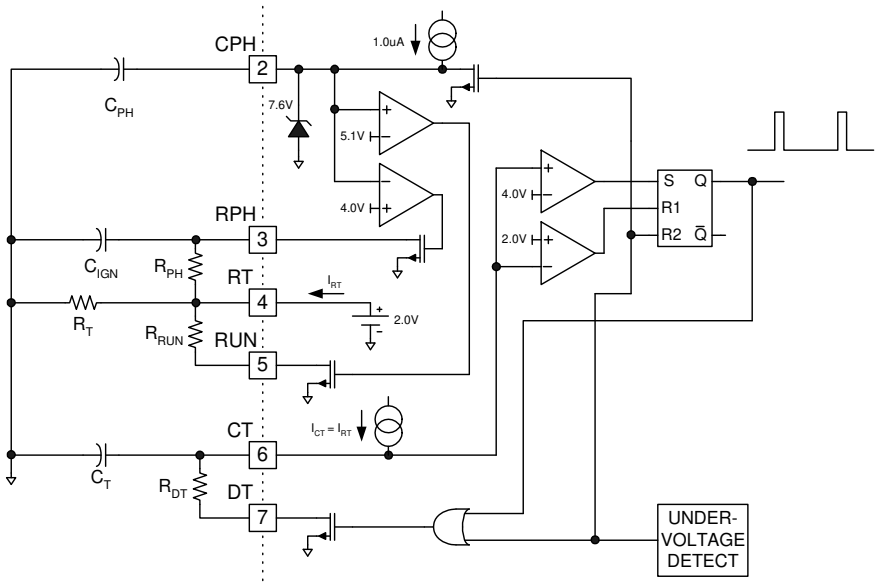


Figure 6: Oscillator section block diagram with external component connection

During the **Preheat Mode**, the operating frequency is determined by the parallel combination of R_{PH} and R_T , combined with the value of C_T and R_{DT} . This frequency, along with the **Preheat Time**, is normally chosen to ensure that adequate heating of the lamp filaments occurs. Typically, a 4.5:1 ratio of the hot filament-to-cold filament resistance is desired for maximum lamp life, as shown in Figure 7 below

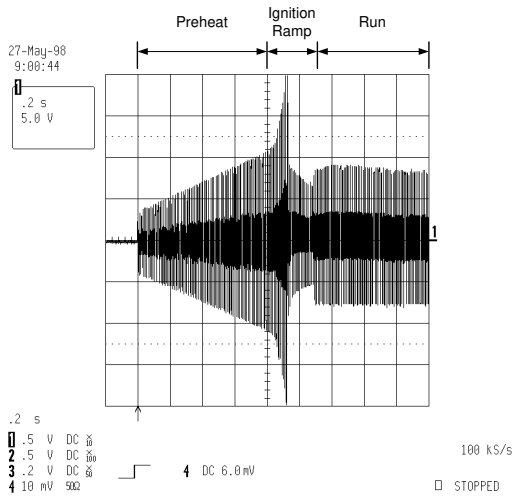


Figure 7: Lamp filament voltage during the preheat, ignition ramp and run modes

The **Preheat Time** is programmed by means of the preheat capacitor, C_{PH}, an internal 1μA current source, and an internal threshold on the CPH pin of 4.0V, according to the following formula:

$$t_{PH} = 4E6 \cdot C_{PH}, \quad \text{or}$$

$$C_{PH} = 250E-9 \cdot t_{PH}$$

At the end of the **Preheat Time,** the internal, open-drain transistor holding the RPH pin to ground turns off, and the voltage on this pin charges exponentially up to the R_T pin potential. During this **Ignition Ramp Mode,** the output frequency exponentially decays to a minimum value. The rate of decay of this frequency is a function of the $R_{PH} * C_{RAMP}$ time constant. Because the **Ignition Ramp Mode** ends when the voltage on the CPH pin reaches 5.15V, the **Ignition Ramp Mode** is always 1/4th as long as the preheat time.

When the CPH pin reaches 5.15V, an open-drain transistor on the RUN pin turns on, and the external R_{RUN} resistor is then in parallel with the R_T resistor. The **Run Mode** operating frequency is therefore a function of the parallel combination of R_{RUN} and R_T, and this means that the operating power of the lamp can be programmed by means of R_{RUN} .

The following graphs, Figures 8 and 9, illustrate the relationship between the effective R_T resistance (i.e., the parallel combination of resistors which programs the C_T capacitor charging current) and the operating frequency.

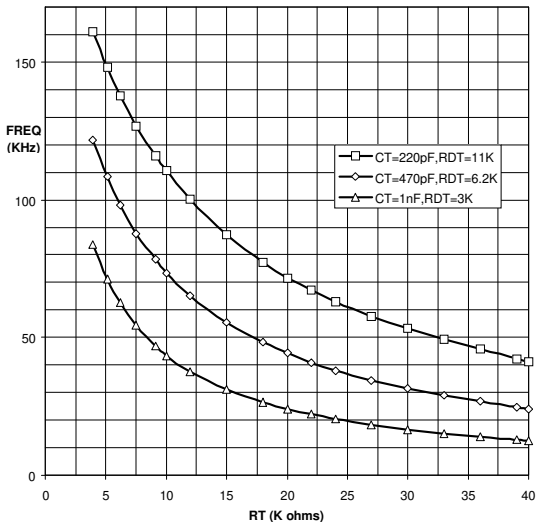


Figure 8: f_{OSC} versus effective R_T (t_{DEAD} = 2.0 usec)

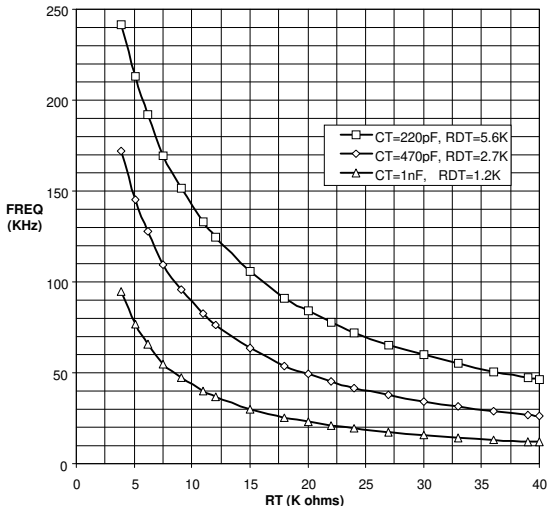


Figure 9: f_{OSC} versus effective R_T (t_{DEAD} = 1.0 usec)

Lamp Protection & Automatic Restart Circuitry Operation

Four pins on the IRS21571D are used for protection, as shown in Figure 10 below. These are VDC (dc bus monitor), SD (unlatched shutdown), CS (latched shutdown) and OC (CS+ threshold programming).

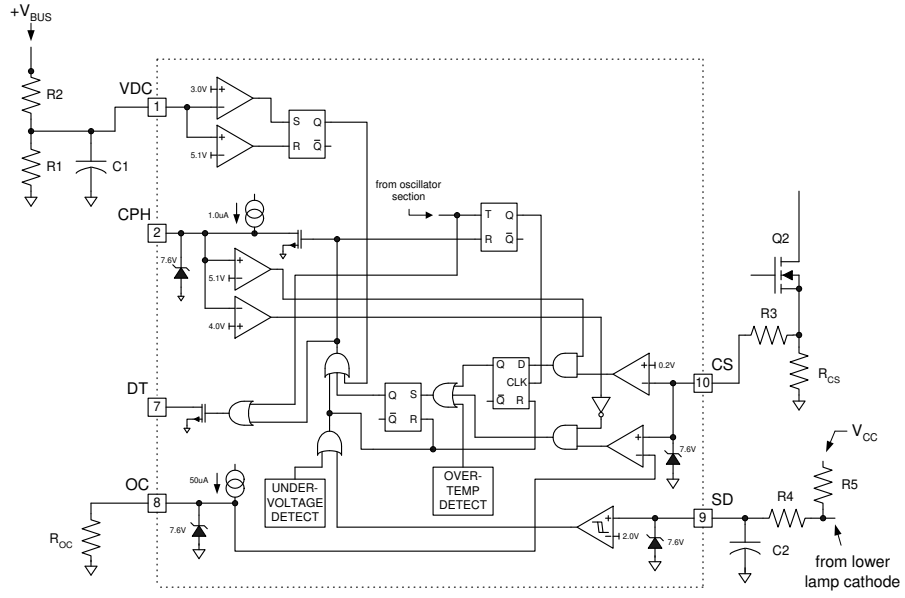


Figure 10: Lamp Protection & Automatic Restart circuitry block diagram with external component connection

Sensing The DC Bus Voltage

The first of these protection pins senses the voltage on the DC bus by means of an external resistor divider and an internal comparator with hysterisis.
When power is first supplied to the IC at system startup, 3 conditions are required before oscillation is initiated: 1.) the voltage on the VCC pin must exceed the rising undervoltage lockout threshold (12.5V), 2.) the voltage at the VDC pin must exceed 5.1V, and 3.) the voltage on the SD pin must be below approximately 1.85V. If a low dc bus condition occurs during normal operation, or if power to the ballast is shut off, the dc bus will collapse prior to the VCC of the chip (assuming the VCC is derived from a charge pump off of the output of the half-bridge). In this case, the voltage on the VDC pin will shut the oscillator off, thereby protecting the power transistors from potentially hazardous hard switching. Approximately 2V of hysterisis has been designed into the internal comparator sensing the VDC pin, in order to account for variations in the dc bus voltage under varying load conditions. When the dc bus recovers, the chip restarts from the beginning of the control sequence, as shown in timing diagram Figure 11 below.

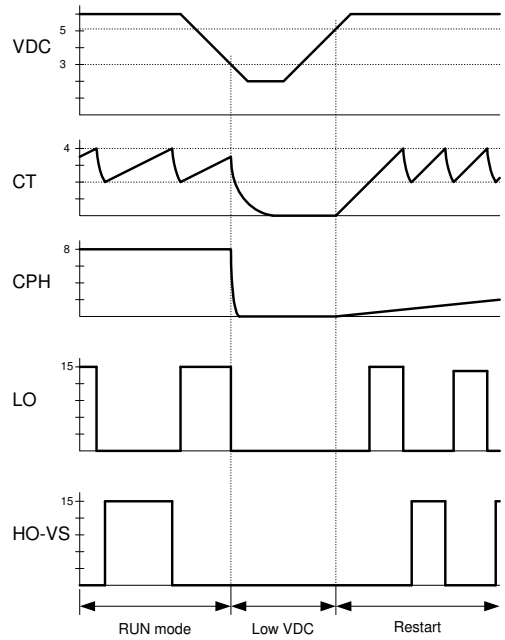


Figure 11: VDC pin fault and auto restart

Lamp Presence Detection and Automatic Restart

The second protection pin, SD, is used for both unlatched shutdown and automatic restart functions. The SD pin would normally be connected to an external circuit which senses the presence of the lamp (or lamps). A example circuit for a single lamp is shown in Figure 12.

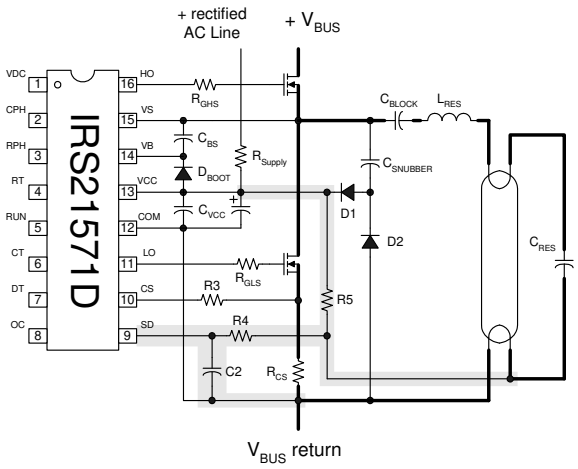


Figure 12: Lamp presence detection circuit connection (shaded area)

When the SD pin exceeds 2.0V (approximately 150mV of hysterisis is included to increase noise immunity), signaling either a lamp fault or lamp removal, the oscillator is disabled, both gate driver outputs are pulled low, and the chip is put into the micropower mode. Since a lamp fault would normally lead to a lamp exchange, when a new lamp is inserted into the fixture, the SD pin would be pulled back to near the ground potential. Under these conditions a reset signal would restart the chip from the beginning of the control sequence, as shown in the timing diagram in Figure 13.

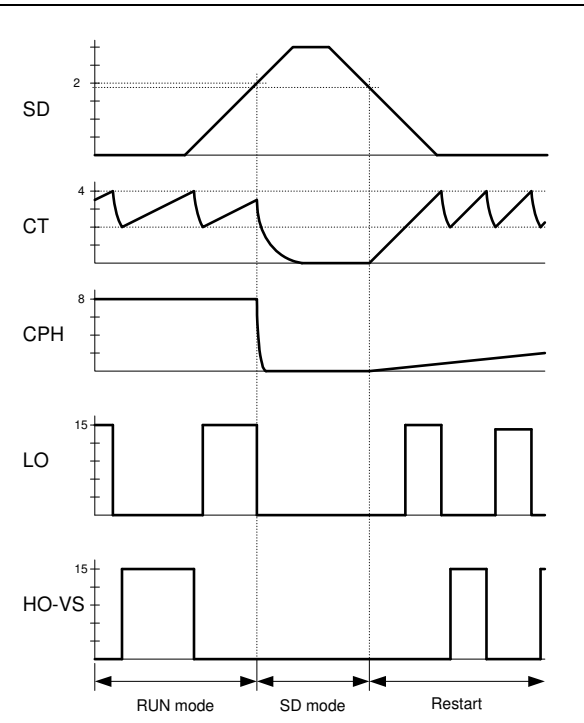


Figure 13: SD pin fault and auto restart

Thus, for a lamp removal and replacement, the ballast automatically restarts the lamp in the proper manner, maximizing lamp life and minimizing stress on the power MOSFETs or IGBTs.

Half-Bridge Current Sensing and Protection

The third pin used for protection is the CS pin, which is normally connected to a resistor in the source of the lower power MOSFET, as shown in Figure 14.

The CS pin is used to sense fault conditions such as failure of a lamp to strike, over-current during normal operation, hard switching, no load, and operation below resonance. If any one of these conditions is sensed, the fault latch is set, the oscillator is disabled, the gate driver outputs go low, and the chip is put into the micropower mode. The CS pin performs its sensing functions on a cycle-by-cycle basis in order to maximize ballast reliability.

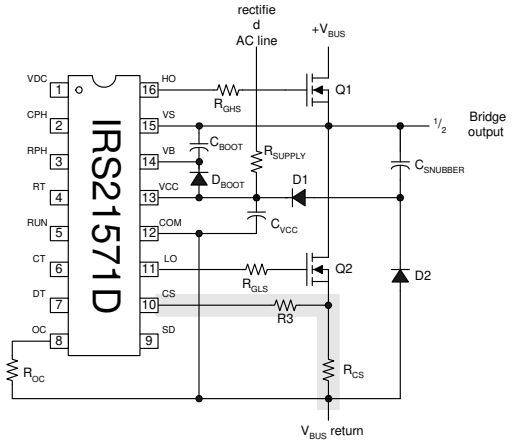


Figure 14: Half-bridge current sensing circuit connection (shaded area)

For the over-current, failure-to-strike, and hard switching fault conditions, an externally programmable, positive-going CS+ threshold is enabled at the end of the preheat time. The level of this positive-going threshold is determined by the value of the resistor ROC. The value of the resistor ROC is determined by the following formula:

$$R_{OC} = \frac{V_{CS+}}{50E-6}, \quad \text{or}$$

$$V_{CS+} = 50E-6 \cdot R_{OC}$$

For the under-current and under-resonance conditions, there is a negative-going CS- threshold of 0.2V which is enabled at the onset of the run mode. The sensing of this CS- threshold is synchronized with the falling edge of the LO output.

Figures 15, 16 and 17 are oscillographs of fault conditions. Figure 15 shows a failure of the lamp to strike, Figure 16 shows a hard switching condition and Figure 17 shows an under-current condition.

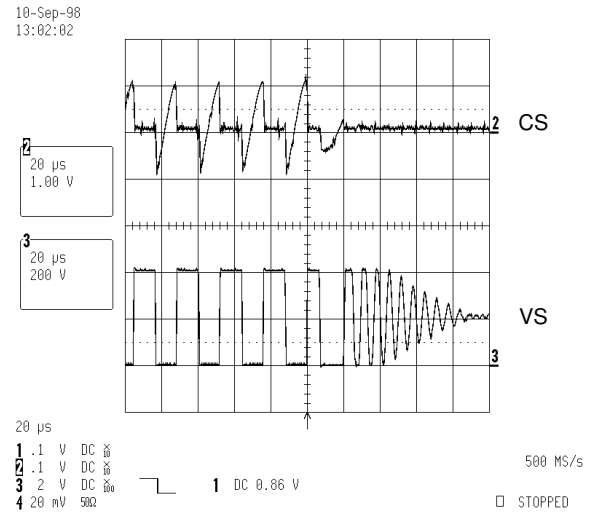


Figure 15: Lamp failure to strike

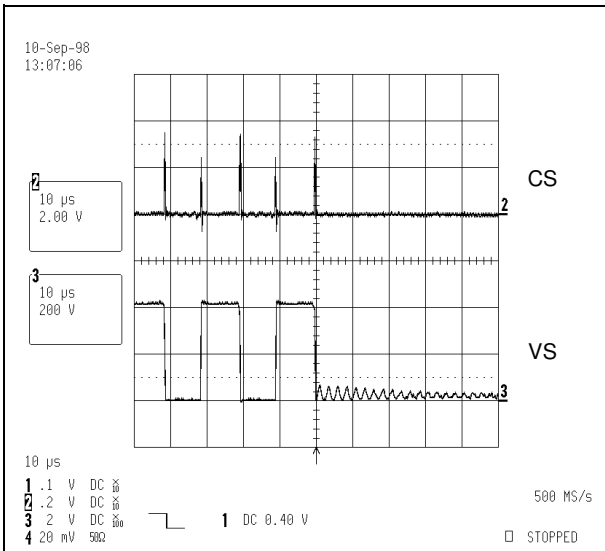


Figure 16: Hard switching condition

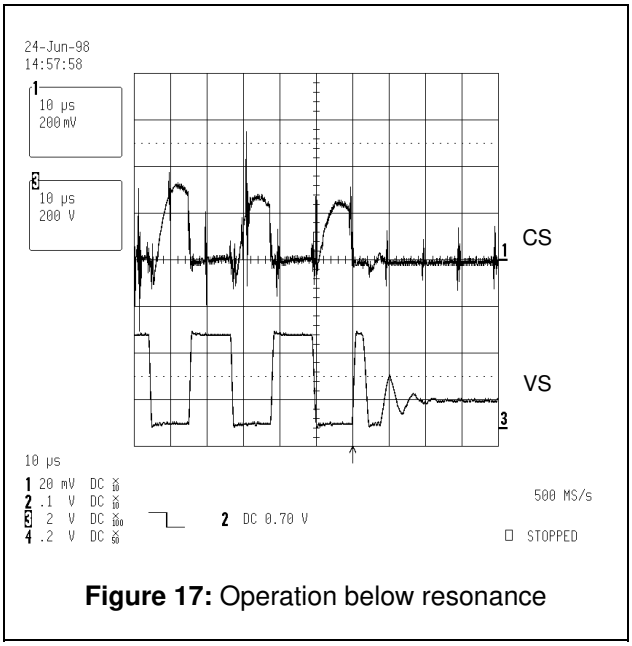


Figure 17: Operation below resonance

Recovery from such a fault condition is accomplished by cycling either SD pin or the VCC pin. When a lamp is removed, the SD pin goes high, the fault latch is reset, and the chip is held off in an unlatched state. Lamp replacement causes the SD pin to go low again, reinitiating the startup sequence. The fault latch can also be reset by the undervoltage lockout signal, if VCC falls below the lower undervoltage threshold.

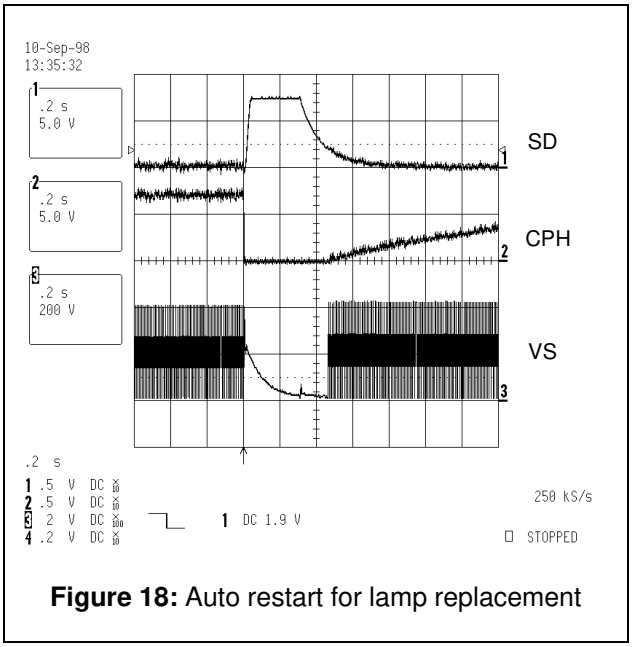


Figure 18: Auto restart for lamp replacement

Package Details: SO16N