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International
IOR Rectifier

Data Sheet No. PD60310

IRS2168D(S)PbF

ADVANCED PFC + BALLAST CONTROL IC

Features

- PFC, ballast control and 600 V half-bridge driver in one IC
- Critical-conduction mode boost-type PFC
- Programmable PFC over-current protection
- Programmable half-bridge over-current protection
- Programmable preheat frequency
- Programmable preheat time
- Programmable ignition ramp
- Programmable run frequency
- Closed-loop ignition current regulation
- RoHs compliant
- Fixed internal 1.6 µs HO and LO deadtime
- Voltage-controlled oscillator (VCO)
- End-of-life window comparator pin
- Internal 65-event current sense up/down fault counter
- DC bus undervoltage reset
- Lamp removal/auto-restart shutdown pin
- Internal bootstrap MOSFET
- Internal 15.6 V Zener clamp diode on V_{cc}
- Micropower startup (250 µA)
- Latch immunity and ESD protection

Description

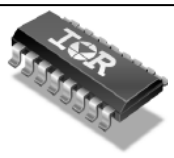
The IRS2168D is a fully integrated, fully protected 600 V ballast control IC designed to drive all types of fluorescent lamps. The IRS2168D is based on the popular IR2166 control IC with additional improvements to increase ballast performance. The PFC circuitry operates in critical conduction mode and provides high PF, low THD and DC bus regulation. The IRS2168D features include programmable preheat and run frequencies, programmable preheat time, programmable PFC over-current protection, closed-loop half-bridge ignition current regulation, and programmable end-of-life protection. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, end-of-life protection, DC bus undervoltage reset as well as an automatic restart function, have been included in the design.

System Features

- One-chip ballast control solution
- Wide range PFC for universal input and multi-lamp ballasts
- Ultra low THD
- Closed-loop ignition regulation for reliable lamp ignition
- End-of-Life window comparator with internal OTA
- Lamp removal/auto-restart function
- Fault counter for robust noise immunity
- Brown-out protection and reset
- Internal bootstrap MOSFET

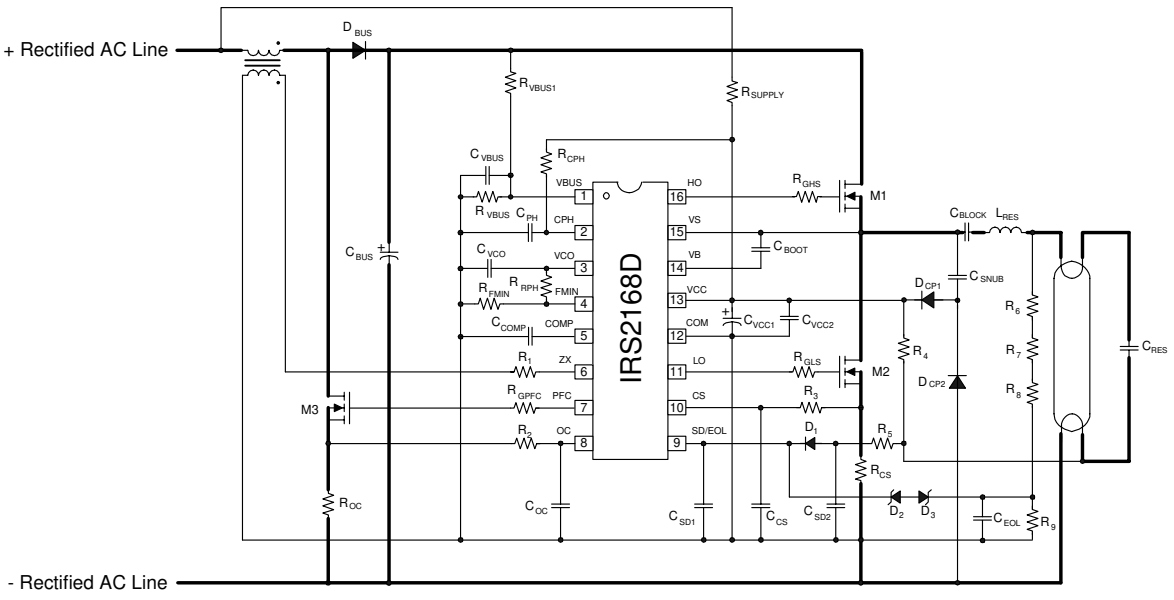
Packages

16-Lead PDIP
IRS2168DPbF



16-Lead SOIC
IRS2168DSPbF

Application Diagram (Typical Only)



* Please note that this datasheet contains advanced information that could change before the product is released to production.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defned positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	V_B pin high-side floating supply voltage		-0.3	625	V
V_S	V_S pin high-side floating supply offset voltage		V_B – 25	V_B + 0.3	
V_{HO}	HO pin high-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	LO pin low-side output voltage		-0.3	V_{CC} + 0.3	
V_{PFC}	PFC gate driver output voltage				
$I_{O,MAX}$	Maximum allowable output current (HO, LO, PFC) due to external power transistor miller effect		-500	500	mA
I_{CC}	V_{CC} current (see Note 1)		-25	25	
V_{BUS}	VBUS pin voltage		-0.3	V_{CC} + 0.3	V
V_{CPH}	CPH pin voltage				
V_{COMP}	COMP pin voltage				
V_{ZX}	ZX pin voltage				
V_{OC}	OC pin voltage				
$V_{SD/EOL}$	SD/EOL pin voltage				
V_{CS}	CS pin voltage				
V_{VCO}	VCO pin voltage		-0.3	6	V
I_{CPH}	CPH pin current		-5	5	mA
I_{VCO}	VCO pin current				
I_{FMIN}	FMIN pin current				
I_{COMP}	COMP pin current				
I_{ZX}	ZX pin current				
I_{OC}	OC pin current				
$I_{SD/EOL}$	SD/EOL pin current				
I_{CS}	CS pin current				
dV/dt	Allowable V_S pin offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ ºC	(16-Pin DIP)	---	1.8	W
	$PD = (T_{JMAX}-T_A)/R_{\theta JA}$	(16-Pin SOIC)	---	1.4	
$R_{\theta JA}$	Thermal resistance, junction to ambient	(16-Pin DIP)	---	70	ºC/W
		(16-Pin SOIC)	---	86	
T_J	Junction temperature		-55	150	ºC
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note 1: This IC contains a Zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6 V. This supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B-V_S	High-side floating supply voltage	V_{BSUV+}	V_{CLAMP}	V
V_S	Steady state high-side floating supply offset voltage	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	V_{CC} supply current	Note 2	10	mA
$I_{SD/EOL}$	SD/EOL pin current	-1	1	
I_{CS}	CS pin current			
I_{OC}	OC pin current			
I_{ZX}	ZX pin current			
V_{VCO}	VCO pin voltage	0	5	V
R_{FMIN}	FMIN pin programming resistor	10	300	kΩ
T_J	Junction temperature	-25	125	ºC

Note 2: Enough current should be supplied into the V_{CC} pin to keep the internal 15.6 V Zener clamp diode on this pin regulated at its voltage, V_{CLAMP}.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS}=14 V +/- 0.25 V, C_{LO} = C_{HO} = C_{PFC} = 1000 pF, R_{FMIN} = 42.2 kΩ, R_{PH} = N/C, V_{CPH} = V_{VCO} = 0 V, $V_{SD/EOL}$ = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0 V, T_A=25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	11.5	12.5	13.5	V	V_{CC} rising from 0 V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	9.5	10.5	11.5		V_{CC} falling from 14 V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	1.5	2.0	3.0		
I_{QCCUV}	UVLO mode V_{CC} quiescent current	---	220	320	µA	V_{CC} = 8 V
I_{QCCFLT}	V_{CC} quiescent current in fault mode	---	0.4	---	mA	MODE=FAULT
I_{CCRUN}	Run mode V_{CC} supply current	---	5.5	7.2		MODE = RUN V_{BUS}=4 V CSD/EOL=1 nF PFC off time = 5 µs
V_{CLAMP}	V_{CC} Zener clamp voltage	14.6	15.6	16.6	V	I_{CC} = 10 mA
Floating Supply Characteristics						
I_{BS}	V_{BS} supply current	---	0.9	1.3	mA	MODE=PREHEAT
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.0	9.0	10.0	V	V_{BS} rising from 0 V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.0	9.0		V_{BS} falling from 14 V
I_{LKVS}	V_S offset supply leakage current	---	---	50	µA	V_B = V_S = 600 V

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS}=14 V +/- 0.25 V, C_{LO} = C_{HO} = C_{PFC} = 1000 pF, R_{FMIN} = 42.2 kΩ, R_{PH} = N/C, V_{CPH} = V_{VCO} = 0 V, $V_{SD/EOL}$ = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0 V, T_A=25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
PFC Error Amplifier Characteristics						
$I_{COMP,\ SOURCE}$	COMP pin OTA error amplifier output current Sourcing	20	30	40	µA	MODE = RUN V_{VBUS} = 3.5 V V_{COMP}=4.0 V
$I_{COMP,\ SINK}$	COMP pin OTA error amplifier output current Sinking	-40	-30	-20		MODE = RUN V_{VBUS} = 4.5 V V_{COMP}=4.0 V
V_{COMPOH}	OTA error amplifier output voltage swing (high state)	12.0	12.5	13.0	V	V_{BUS}=3.5 V I_{COMP}=I_{COMP}SOURCE-5 µA
V_{COMPOL}	OTA error amplifier output voltage swing (low state)	0.2	0.4	0.5		V_{BUS}=5.0 V I_{COMP}=I_{COMP}SINK+5 µA
$V_{COMPFLT}$	OTA error amplifier output voltage in fault mode	---	0	---		V_{BUS}=4.0 V
PFC Control Characteristics						
$V_{VBUSREG}$	V_{BUS} internal reference voltage	3.9	4.0	4.1	V	V_{COMP} = 4.0 V
V_{VBUSOV}	V_{BUS} overvoltage comparator threshold	4.1	4.3	4.5		
$V_{VBUSOV-}$	V_{BUS} overvoltage fault reset threshold	4.0	4.15	4.3		
V_{ZX}	ZX pin threshold voltage	1.8	2.0	2.2		
V_{ZXHYS}	ZX pin comparator hysterisis	100	300	500	mV	
$V_{ZXclamp}$	ZX pin clamp voltage (high state)	5.5	6.5	7.5	V	I_{ZX} = 1 mA
t_{BLANK}	OC pin current-sensing blank time	---	300	---	ns	V_{BUS}=4.0 V V_{COMP}=4.0 V
t_{WD}	PFC watch-dog pulse interval	150	400	500	µs	ZX = 0, V_{COMP} = 4.0 V
PFC Protection Circuitry Characteristics						
$V_{VBUSUV-}$	V_{BUS} pin undervoltage reset threshold	2.7	3.0	3.3	V	
V_{OCTH+}	OC pin over-current sense threshold	1.1	1.2	1.3		V_{BUS}=V_{COMP}=4.0 V

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS}=14 V +/- 0.25 V, C_{LO} = C_{HO} = C_{PFC} = 1000 pF, R_{FMIN} = 42.2 kΩ, R_{PH} = N/C, V_{CPH} = V_{VCO} = 0 V, $V_{SD/EOL}$ = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0 V, T_A=25 °C unless otherwise specified.

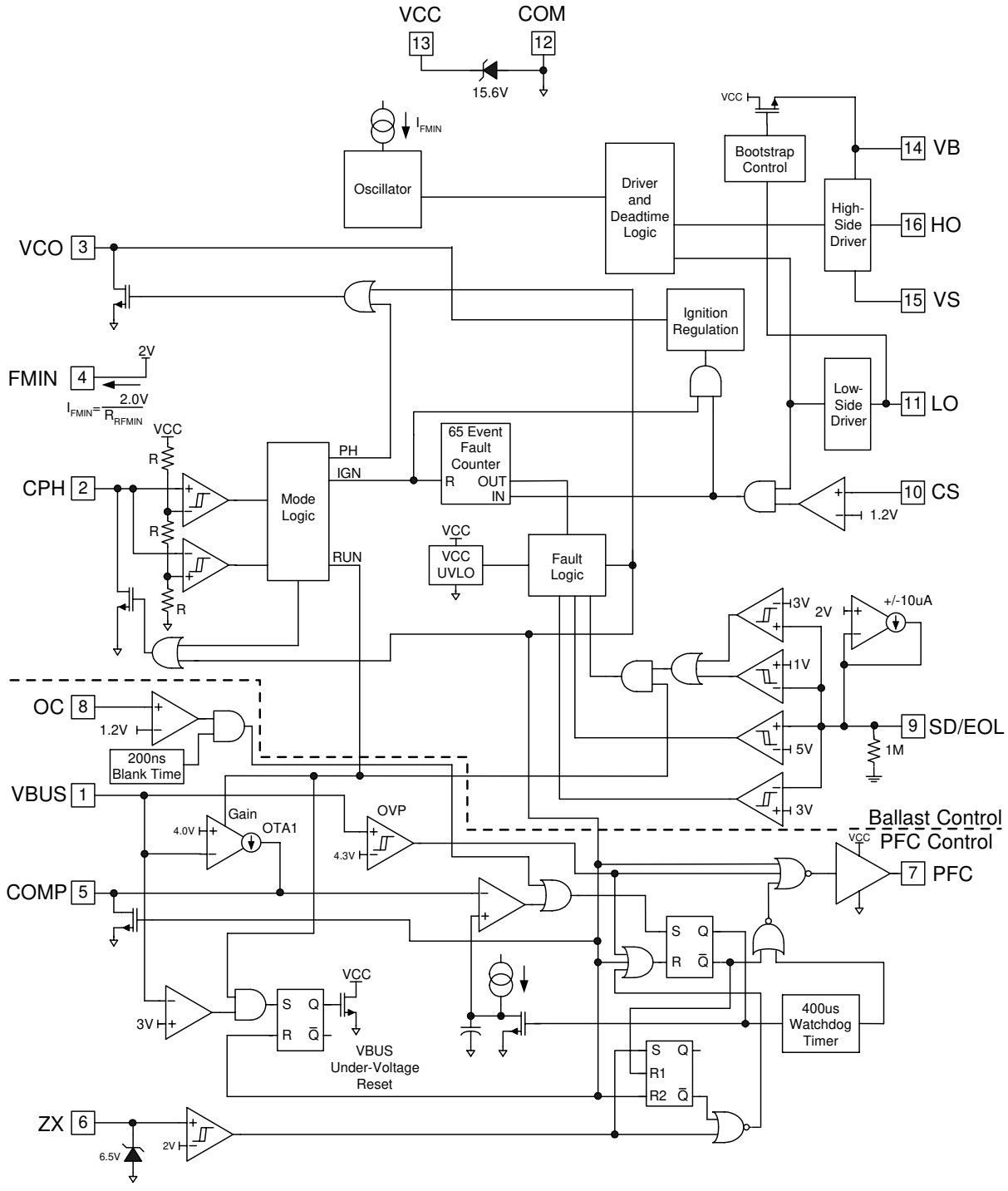
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Ballast Control Oscillator Characteristics						
$f_{OSC, RUN}$	Half-bridge oscillator run frequency	42.5	44.5	46.5	kHz	MODE = RUN
$f_{OSC, PH}$	Half-bridge oscillator preheat frequency	81	85	89		RPH = 42.2 kΩ, MODE = PREHEAT
D	Oscillator duty cycle	---	50	---	%	
$t_{d, LO}$	LO output deadtime	1.1	1.6	2.1	µs	
$t_{d, HO}$	HO output deadtime	1.1	1.6	2.1		
V_{FMIN}	F_{MIN} pin voltage	1.9	2.0	2.1	V	V_{CC} = 14.0 V
Ballast Control Preheat, Ignition and Run Mode Characteristics						
$V_{CPHEOP+}$	CPH pin end of preheat rising threshold voltage	8.8	9.3	9.8	V	
$V_{CPHSOI-}$	CPH pin start of ignition falling threshold voltage	4.6	4.9	5.2		
V_{VCOPH}	VCO pin preheat mode voltage	---	0	---		MODE = PREHEAT
V_{VCOIGN}	VCO pin ignition mode voltage	---	(Open Drain)	---		MODE = IGNITION, V_{CS} < V_{CSTH+}
I_{VCOIGN}	VCO pin ignition regulation discharge current	---	0.6	---	mA	MODE = IGNITION, V_{VCO} = 1 V, V_{CS} > V_{CSTH+}
$V_{CPHRUN+}$	CPH pin run mode rising threshold voltage	8.8	9.3	9.8	V	MODE = IGNITION
V_{VCORUN}	VCO pin run mode voltage	---	(Open Drain)	---		MODE = RUN
Ballast Control Protection Circuitry Characteristics						
V_{CSTH+}	CS pin over-current sense threshold	1.1	1.2	1.3	V	
n_{EVENTS}	CS pin fault counter number of events	30	65	100	---	MODE = PREHEAT or RUN
V_{SDTH+}	SD pin rising non-latched shutdown threshold voltage	4.7	5.2	5.7	V	
V_{SDTH-}	SD pin falling reset threshold voltage	2.5	3.0	3.5		
$V_{EOLBIAS}$	EOL pin internal bias voltage	1.9	2.0	2.1		
V_{EOLTH+}	EOL pin rising latched shutdown threshold voltage	2.85	3.0	3.15		MODE = RUN
V_{EOLTH-}	EOL pin falling latched shutdown threshold voltage	0.9	1.0	1.1		MODE = RUN
$I_{EOL, SOURCE}$	EOL pin OTA output sourcing current	---	10	---	µA	MODE = PREHEAT V_{EOL} = 1.5 V
$I_{EOL, SINK}$	EOL pin OTA output sinking current	---	-10	---		MODE = PREHEAT V_{EOL} = 2.5 V
V_{CPHFLT}	CPH pin fault mode voltage	---	0	---	V	MODE = FAULT
V_{VCOFLT}	VCO pin fault mode voltage					
$V_{FMINFLT}$	FMIN pin fault mode voltage					

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS}=14 V +/- 0.25 V, C_{LO} = C_{HO} = C_{PFC} = 1000 pF, R_{FMIN} = 42.2 kΩ, R_{PH} = N/C, V_{CPH} = V_{VCO} = 0 V, $V_{SD/EOL}$ = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0 V, T_A=25 °C unless otherwise specified.

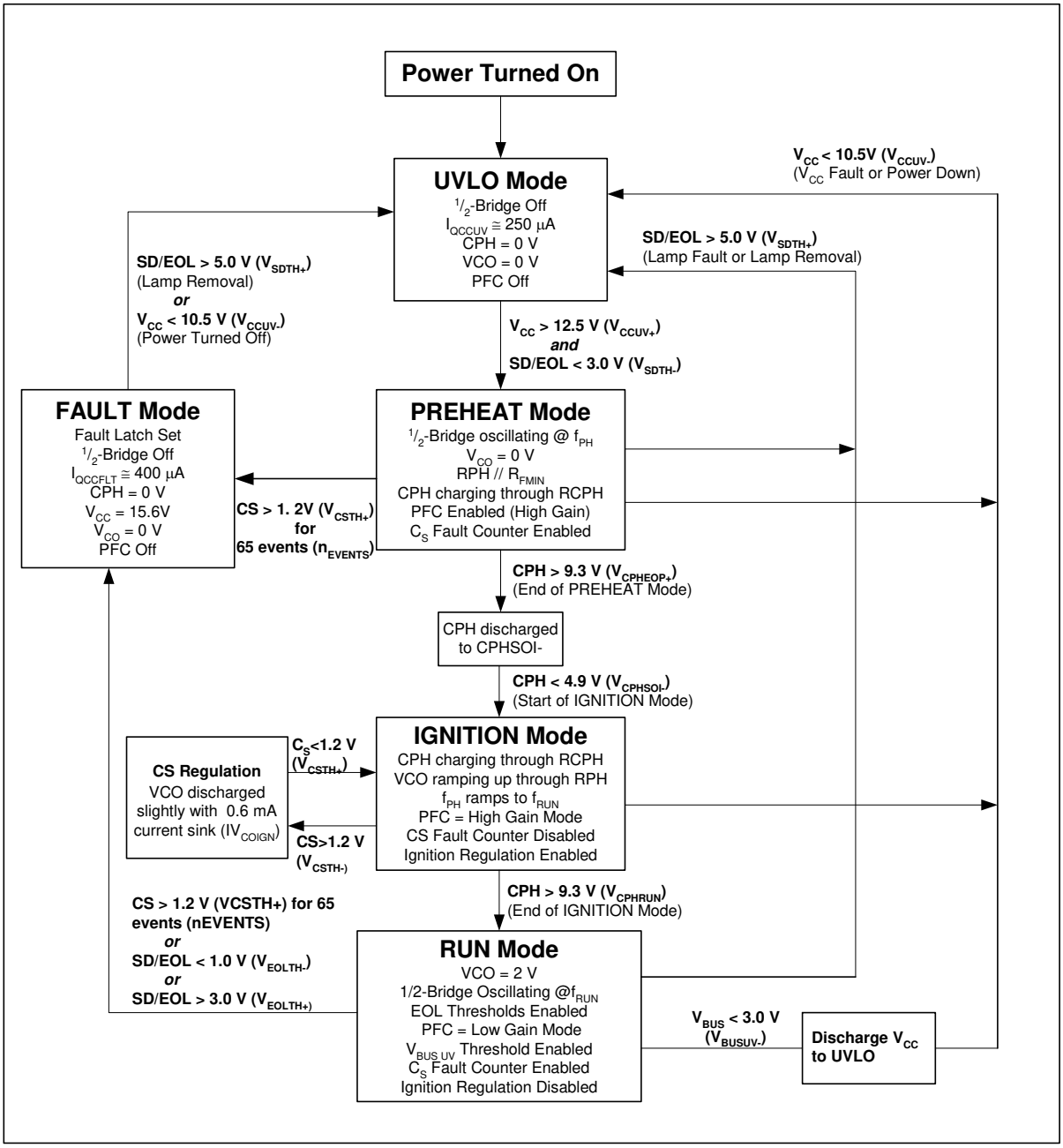
Gate Driver Output Characteristics (HO, LO and PFC pins)						
V_{OL}	Low-level output voltage	---	COM	---	V	
V_{OH}	High-level output voltage	---	V_{CC}	---		
t_r	Turn-on rise time	---	120	220	ns	
t_f	Turn-off fall time	---	50	100		
I_{0+}	Source current	---	180	---	mA	
I_{0-}	Sink current	---	260	---		
Bootstrap FET Characteristics						
$V_{B/ON}$	V_B when the bootstrap FET is on	13.0	13.4	---	V	
$I_{B/CAP}$	V_B source current when FET is on	40	55	---	mA	C_{BS}=0.1 µF
$I_{B/10V}$	V_B source current when FET is on	9	12	---		V_B=10 V

Schematic Block Diagram



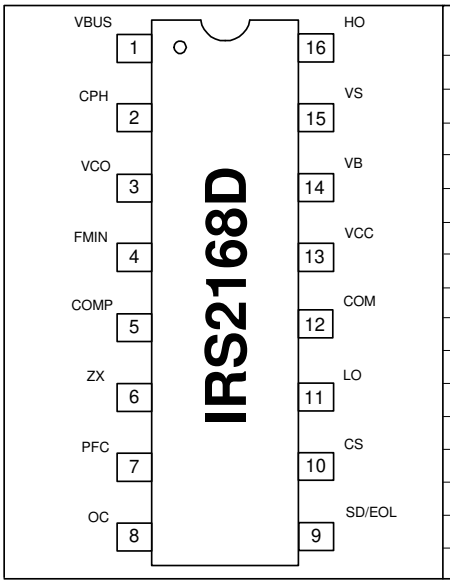
Please Note: All values shown in block diagram are typical values only.

State Diagram



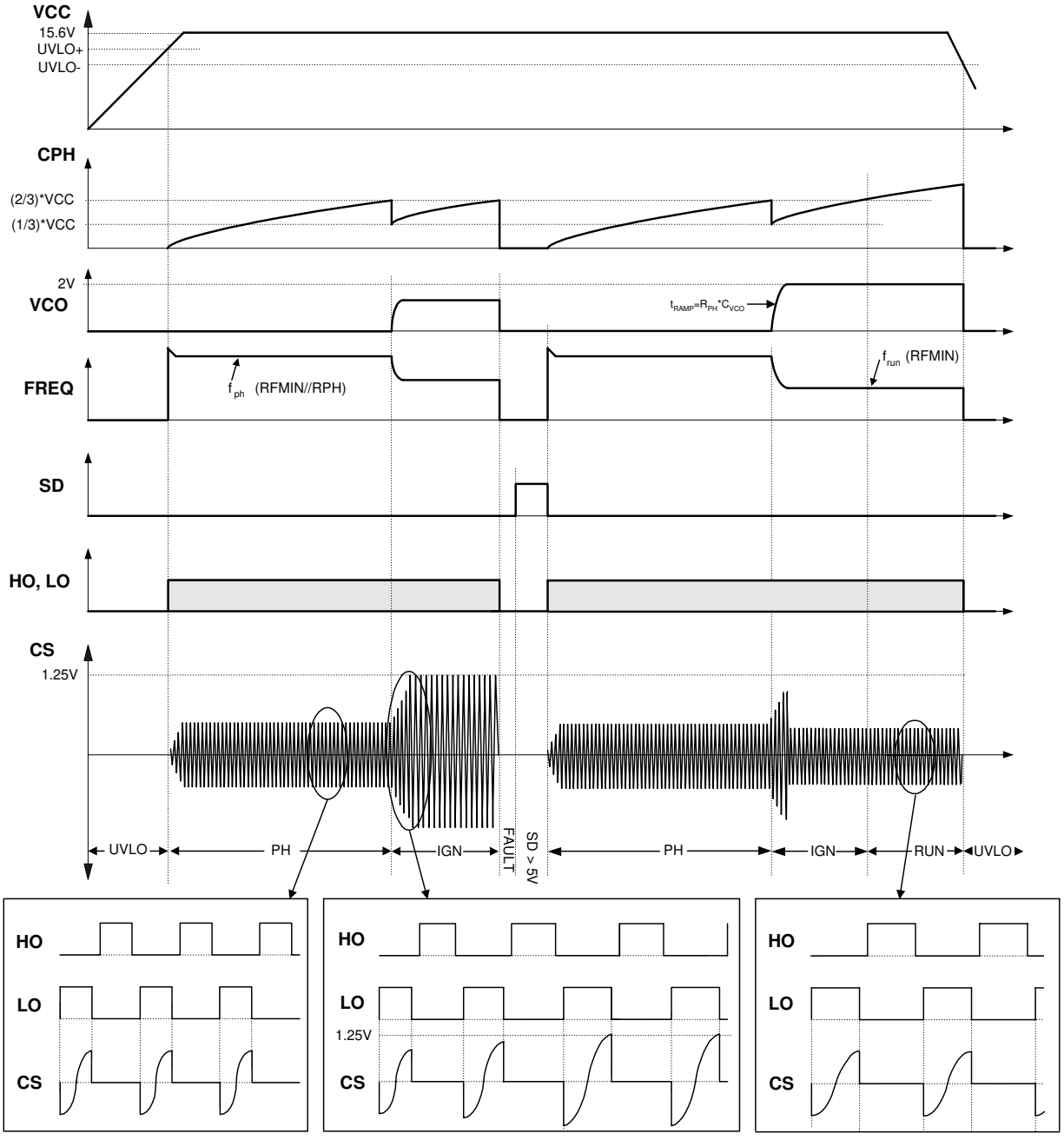
All values are typical.
Please refer to application diagram on page 1.

Lead Assignments & Definitions



Pin #	Symbol	Description
1	VBUS	DC bus sensing input
2	CPH	Preheat timing input
3	VCO	Voltage controlled oscillator/ignition ramp input
4	FMIN	Oscillator minimum frequency setting
5	COMP	PFC error amplifier compensation
6	ZX	PFC zero-crossing detection
7	PFC	PFC gate driver output
8	OC	PFC current sensing input
9	SD/EOL	Shutdown/end of life sensing input
10	CS	Half-Bridge current sensing input
11	LO	Low-side gate driver output
12	COM	IC power & signal ground
13	VCC	Logic & low-side gate driver supply
14	VB	High-side gate driver floating supply
15	VS	High voltage floating return
16	HO	High-side gate driver output

Timing Diagrams Ballast Section



I. Ballast Section Functional Description

Undervoltage Lockout Mode (UVLO)

The undervoltage lockout mode (UVLO) is defined as the state the IC is in when V_{CC} is below the turn-on threshold of the IC. To identify the different modes of the IC, refer to the State Diagram shown on page 3 of this document. The IRS2168D undervoltage lockout is designed to maintain an ultra low supply current of 250 µA (I_{QCCUV}), and to guarantee the IC is fully functional before the high- and low-side output drivers are activated. Figure 1 shows an efficient supply voltage using the micro-power start-up current of the IRS2168D together with a snubber charge pump from the half-bridge output (R_{VCC}, C_{VCC1}, C_{VCC2}, C_{SNUB}, D_{CP1} and D_{CP2}).

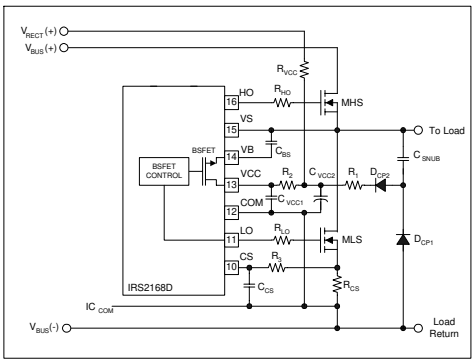


Figure 1: Start-up and supply circuitry

The V_{CC} capacitors (C_{VCC1} and C_{VCC2}) are charged by the current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to set the desired AC line input voltage turn-on threshold for the ballast. When the voltage at V_{CC} exceeds the IC start-up threshold (V_{CCUV+}) and the SD pin is below 3.0 V (V_{SDTH}-), the IC turns on and LO begins to oscillate. The capacitors at V_{CC} begin to discharge due to the increase in IC operating current (Fig. 2). The high-side supply voltage, V_B-V_S, begins to increase as capacitor C_{BS} is charged through the internal bootstrap MOSFET during the LO on-time of each LO switching cycle. When the V_B-V_S voltage exceeds the high-side start-up threshold (V_{BSUV+}), HO then begins to oscillate. This may take several cycles of LO to charge V_B-V_S above V_{BSUV+} due to R_{DSon} of the internal bootstrap MOSFET.

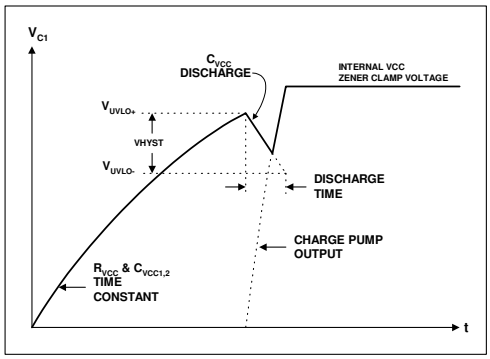


Figure 2: V_{CC} supply voltage

When LO and HO are both oscillating, the external MOSFETs (MHS and MLS) are turned on and off with a 50% duty cycle and a non-overlapping deadtime of 1.6 µs (t_d). The half-bridge output (pin V_S) begins to switch between the DC bus voltage and COM. During the deadtime between the turn-off of LO and the turn-on of HO, the half-bridge output voltage transitions from COM to the DC bus voltage at a dV/dt rate determined by the snubber capacitor (C_{SNUB}). As the snubber capacitor charges, current will flow through the charge pump diode (D_{CP2}) to V_{CC}. After several switching cycles of the half-bridge output, the charge pump and the internal 15.6 V Zener clamp of the IC take over as the supply voltage. Capacitor C_{VCC2} supplies the IC current during the V_{CC} discharge time and should be large enough such that V_{CC} does not decrease below UVLO- before the charge pump takes over. Capacitor C_{VCC1} is required for noise filtering and must be placed as close as possible and directly between V_{CC} and COM, and should not be lower than 0.1 µF Resistors R_1 and R_2 are recommended for limiting high currents that can flow to V_{CC} from the charge pump during hard-switching of the half-bridge or during lamp ignition. The internal bootstrap MOSFET and supply capacitor (C_{BS}) comprise the supply voltage for the high side driver circuitry. During UVLO mode, the high- and low-side driver outputs HO and LO are both low, the internal oscillator is disabled, and pin CPH is connected internally to COM for resetting the preheat time.

Preheat Mode (PH)

The IRS2168D enters preheat mode when V_{CC} exceeds the UVLO positive-going threshold (V_{CCUV+}). The internal MOSFET that connects pin CPH to COM is turned off and an external resistor (Fig. 3) begins to charge the external preheat timing capacitor (C_{PH}). LO and HO begin to oscillate at a higher soft-start frequency and ramp down quickly to the preheat frequency. The VCO pin is connected to COM through an internal

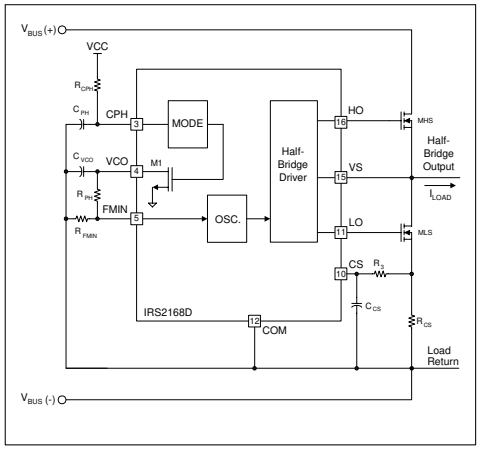


Figure 3: Preheat circuitry

MOSFET M1 so the preheat frequency is determined by the equivalent resistance at the FMIN pin formed by the parallel combination of resistors R_{FMIN} and R_{PH}. The frequency remains at the preheat frequency until the voltage on pin C_{PH} exceeds approvixmately $2/3*V_{CC}$ ($V_{CPHEOP+}$) and the IC enters Ignition Mode. During preheat mode, the over-current protection on pin CS and the 65-cycle (n_{EVENTS}) consecutive over-current fault counter are both enabled. The PFC circuit is working in high-gain mode (see PFC section) and keeps the DC bus voltage regulated at a constant level.

Ignition Mode (IGN)

The IRS2168D ignition mode is defined by the second time C_{PH} charges from $1/3*V_{CC}$ ($V_{CPHSOI-}$) to $2/3*V_{CC}$ ($V_{CPHRUN+}$). When the voltage on pin CPH exceeds $2/3*V_{CC}$ ($V_{CPHRUN+}$) for the first time, pin CPH is discharged quickly through an internal MOSFET down to $1/3*V_{CC}$ ($V_{CPHSOI-}$) (see Figs. 4 and 5). The internal MOSFET turns off and the voltage on pin C_{PH} begins to increase again. The internal MOSFET M1 at pin V_{CO} turn off and resistor R_{PH} is disconnected from COM. The equivalent resistance at the FMIN pin increases from the parallel combination (R_{PH}//R_{FMIN}) to R_{FMIN} at a rate programmed by the external capacitor at pin VCO (C_{VCO}) and resistor R_{PH}. This causes the operating frequency to ramp down smoothly from the preheat frequency through the ignition frequency to the final run frequency. During this ignition ramp, the frequency sweeps through the resonance frequency of the lamp output stage to ignite the lamp.

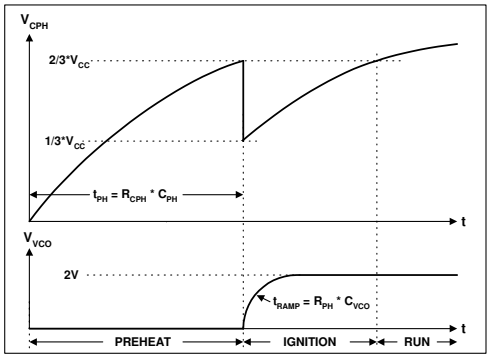


Figure 4: C_{PH} and VCO timing diagram

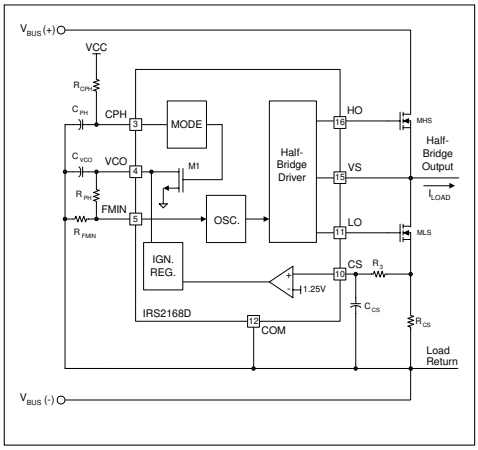


Figure 5: Ignition circuitry

The over-current threshold on pin CS will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor R_{CS}. This resistor programs the maximum peak ignition current (and therefore peak

ignition voltage) of the ballast output stage. Should this voltage exceed the internal threshold of 1.2 V (V_{CSTH+}), the ignition regulation circuit controls the voltage on the VCO pin to increase the frequency slightly (see Fig. 6). This cycle-by-cycle feedback from the C_S pin to the VCO pin will adjust the frequency each cycle to limit the amplitude of the current for the entire duration of ignition mode.

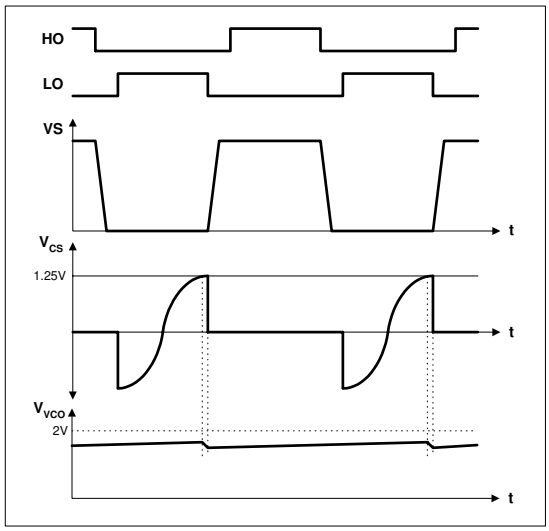


Figure 6: Ignition regulation timing diagram

When C_{PH} exceeds 2/3*V_{CC} ($V_{CPHRUN+}$) for the second time, the IC enters run mode and the fault counter becomes enabled. The ignition regulation disabled in run mode but the IC will enter fault mode after 65 (n_{EVENTS}) consecutive over-current faults and gate driver outputs HO, LO and PFC will be latched low.

The output voltage of the ballast will increase during the ignition ramp t_{RAMP} because the frequency ramp down from the preheat frequency to the ignition frequency and will be constant during ignition because the ignition regulation circuit will regulate the amplitude of the current for the entire duration of the ignition time t_{IGN} (Figs. 7 and 8).

During ignition mode, the PFC circuit is working in high-gain mode and keeps the DC bus voltage regulated at a constant level. The high-gain mode is necessary to prevent the DC bus from decreasing during lamp ignition or ignition regulation. Also during ignition mode, the SD/EOL fault is disabled.

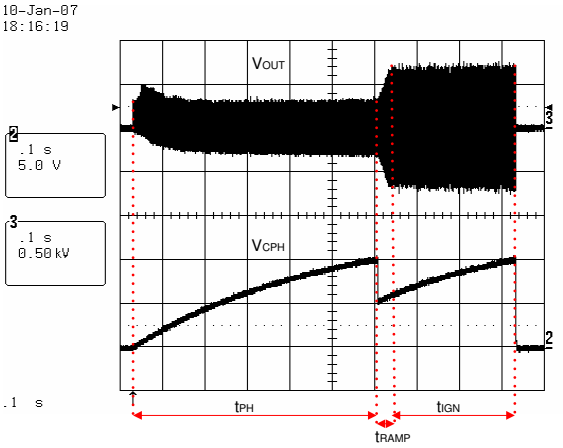


Figure 7: Ballast output voltage and CPH pin during preheat and ignition with deactivated lamp, time span 100ms

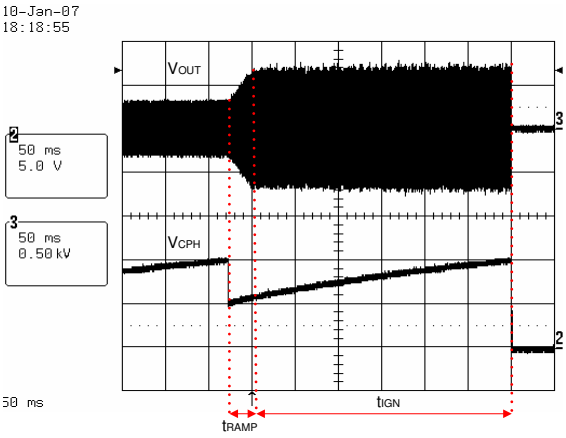


Figure 8: Ballast output voltage and CPH pin during preheat and ignition with deactivated lamp, time span 50ms

Run Mode (RUN)

Once V_{CC} has exceeded 2/3*V_{CC} ($V_{CPHRUN+}$) for the second time, the IC enters run mode. CPH continues to charge up to V_{CC}. The operating frequency is at the minimum frequency (after the ignition ramp) and is programmed by the external resistor (R_{FMIN}) at the FMIN pin. Should hard-switching occur at the half-bridge at any time (open-filament, lamp removal, etc.), the voltage across the current sensing resistor (R_{CS}) will exceed the internal threshold of 1.2 V (V_{CSTH+}) and the fault counter will begin counting (see Fig. 5). Should the number of consecutive over-current faults exceed 65 (n_{EVENTS}), the IC will enter fault mode and the HO, LO and PFC gate driver outputs will be latched low. During run mode, the end-of-life (EOL) window comparator and the DC bus undervoltage reset are both enabled.

DC Bus Undervoltage Reset

Should the DC bus decrease too low during a brown-out line condition or over-load condition, the resonant output stage to the lamp can shift near or below resonance. This can produce hard switching at the half- bridge that can damage the half-bridge switches, or, the DC bus can decrease too far and the lamp can extinguish. To protect against this, the V_{BUS} pin includes a 3.0 V undervoltage reset threshold V_{BUSUV-}. When the IC is in run mode and the voltage at the V_{BUS} pin decreases below 3.0 V (V_{BUSUV-}), V_{CC} will be discharged through an internal MOSFET down to the V_{CCUV-} threshold and all gate driver outputs will be latched low. For proper ballast design, the designer should set the over-current limit of the PFC section such that the DC bus does not drop until the AC line input voltage falls below the minimum rated input voltage of the ballast (see PFC section). When the PFC over-current limit is correctly set, the DC bus voltage will start to decrease when over-current is reached during low-line conditions. The voltage measured at the V_{BUS} pin will decrease below the internal 3.0 V threshold V_{BUSUV-} and the ballast will turn off cleanly. The pull-up resistor to V_{CC} (R_{VCC}) will then turn the ballast on again when the AC input line voltage increases high enough again where V_{CC} exceeds V_{CCUV+}. R_{VCC} should be set to turn the ballast on at the minimum specified ballast input voltage and the PFC over-current should be set somewhere below this level. This hysteresis will result in clean turn-on and turn-off of the ballast.

SD/EOL and CS Fault Mode

Should the voltage at the SD/EOL pin exceed 3.0 V (V_{EOLTH+}) or decrease below 1.0 V (V_{EOLTH-}) during run mode, an end-of-life (EOL) fault condition has occurred and the IC enters fault mode. LO, HO and PFC gate driver outputs are all latched off in the 'low' state. CPH is discharged to COM for resetting the preheat time and VCO is discharged to COM for resetting the frequency. To exit fault mode, V_{CC} can be decreased below V_{CCUV-} (ballast power off) or the SD pin can be increased above 5.0 V (V_{SDTH+}) (lamp removal). Either of these will force the IC to enter UVLO mode (see State Diagram, page 3). Once V_{CC} is above V_{CCUV+} (ballast power on) and SD is pulled above 5.0 V (V_{SDTH+}) and back below 3.0 V (V_{SDTH-}) (lamp re-insertion), the IC will enter preheat mode and begin oscillating again.

The current sense function will force the IC to enter fault mode only after the voltage at the CS pin has been greater than 1.2 V (V_{CSTH+}) for 65 (n_{EVENTS}) consecutive cycles of LO. The voltage at the CS pin is AND-ed with LO (see Fig. 9) so it will work with pulses that occur during the LO on-time or DC. If the over-current faults are not consecutive, then the internal fault counter will count back down each cycle when there is no fault. Should an over-current fault occur only for a few cycles and then not occur again, the counter will eventually reset to zero. The over-current fault counter is enabled during preheat and run modes and disabled during ignition mode.

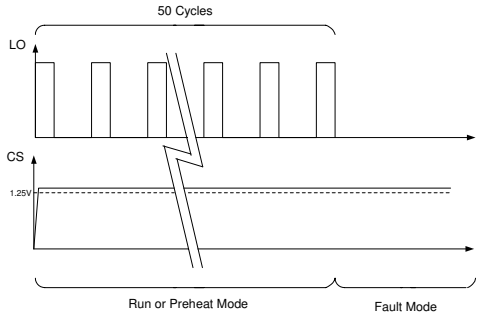


Figure 9: Fault counter timing diagram

II. PFC Section Functional Description

In most electronic ballasts it is necessary to have the circuit act as a pure resistive load to the AC input line voltage. The degree to which the circuit matches a pure resistor is measured by the phase shift between the input voltage and input current and how well the shape of the input current waveform matches the shape of the sinusoidal input voltage. The cosine of the phase angle between the input voltage and input current is defined as the power factor (PF), and how well the shape of the input current waveform matches the shape of the input voltage is determined by the total harmonic distortion (THD). A power factor of 1.0 (maximum) corresponds to zero phase shift and a THD of 0% and represents a pure sinusoidal waveform (no distortion). For this reason it is desirable to have a high PF and a low THD. To achieve this, the IRS2168D includes an active power factor correction (PFC) circuit.

The control method implemented in the IRS2168D is for a boost-type converter (Fig. 10) running in critical-conduction mode (CCM). This means that during each switching cycle of the PFC MOSFET, the circuit waits until the inductor current discharges to zero before turning the PFC MOSFET on again. The PFC MOSFET is turned on and off at a much higher frequency (>10 kHz) than the line input frequency (50 to 60 Hz).

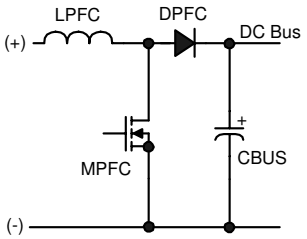


Figure 10: Boost converter circuit

When the switch M_{PFC} is turned on, the inductor L_{PFC} is connected between the rectified line input (+) and (-) causing the current in L_{PFC} to charge up linearly. When M_{PFC} is turned off, L_{PFC} is connected between the rectified line input (+) and the DC bus capacitor C_{BUS} (through diode D_{PFC}) and the stored current in L_{PFC} flows into C_{BUS}. M_{PFC} is turned on and off at a high frequency and the voltage on C_{BUS} charges up to a specified voltage. The feedback loop of the IRS2168D regulates this voltage to a fixed value by continuously monitoring the DC bus voltage and adjusting the on-time of M_{PFC} accordingly. For an increasing DC bus the on-time is decreased, and for a decreasing DC bus the on-time is increased. This negative feedback control is performed with a slow loop speed and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage for high power factor and low THD. The on-time of M_{PFC} therefore appears to be fixed (with an additional modulation to be discussed later) over several cycles of the line voltage. With a fixed on-time, and an off-time determined by the inductor current discharging to zero, the result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Fig. 11).

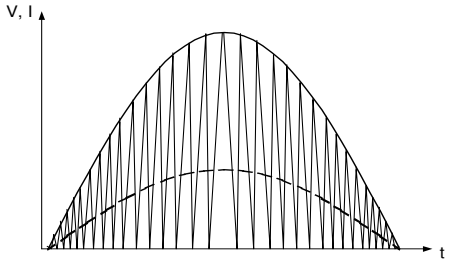


Figure 11: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage

When the line input voltage is low (near the zero crossing), the inductor current will charge up to a small amount and the discharge time will be fast resulting in a high switching frequency. When the input line voltage is high (near the peak), the inductor current will charge up to a higher amount and the discharge time will be longer giving a lower switching frequency.

The PFC control circuit of the IRS2168D (Fig. 12) includes five control pins: V_{BUS}, COMP, ZX, PFC and OC. The V_{BUS} pin measures the DC bus voltage via an external resistor voltage divider. The COMP pin programs the on-time of M_{PFC} and the speed of the feedback loop with an external capacitor. The ZX pin detects when the inductor current discharges to zero each switching cycle using a secondary winding from the P_{FC} inductor. The P_{FC} pin is the low-side gate driver output for the external MOSFET, M_{PFC}. The OC pin senses the current flowing through M_{PFC} and performs cycle-by-cycle over-current protection.

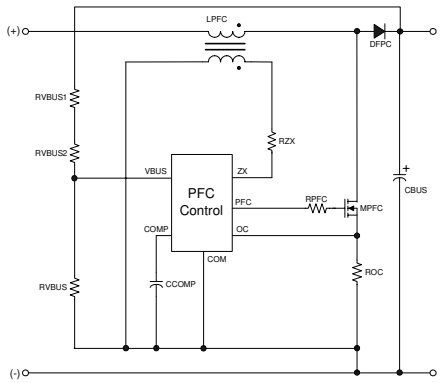


Figure 12: IRS2168D simplified PFC control circuit

The V_{BUS} pin is regulated against a fixed internal 4.0 V reference voltage for regulating the DC bus voltage (Fig. 13). The feedback loop is performed by an operational transconductance amplifier (OTA) that sinks or sources a current to the external capacitor at the COMP pin. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor (C1, Figure 13) and therefore programs the on-time of M_{PFC}. During preheat and ignition modes of the ballast section, the gain of the OTA is set to a high level to raise the DC bus level quickly and to minimize the transient on the DC bus that can occur during ignition. During run mode, the gain is then decreased to a lower level necessary for a slower

loop speed for achieving high power factor and low THD.

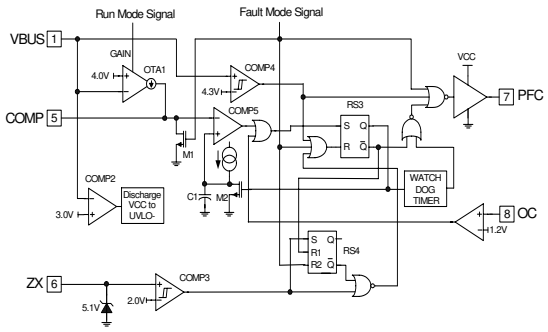


Figure 13: IRS2168D detailed PFC control circuit

The off-time of M_{PFC} is determined by the time it takes the L_{PFC} current to discharge to zero. The zero current level is detected by a secondary winding on LPFC that is connected to the ZX pin through an external current limiting resistor R_{ZX}. A positive-going edge exceeding the internal 2 V threshold (V_{ZXTH+}) signals the beginning of the off-time. A negative-going edge on the ZX pin falling below 1.7 V (V_{ZXTH+} - V_{ZXHYS}) will occur when the L_{PFC} current discharges to zero which signals the end of the off-time and M_{PFC} is turned on again (Fig. 14). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the ballast section (Fault Mode), an over-voltage or undervoltage condition on the DC bus, or, the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, M_{PFC} will remain off until the watch-dog timer forces a turn-on of M_{PFC} for an on-time duration programmed by the voltage on the COMP pin. The watch-dog pulses occur every 400 µs (t_{WD}) indefinitely until a correct positive- and negative-going signal is detected on the ZX pin and normal PFC operation is resumed. Should the OC pin exceed the 1.2 V (V_{OCTH+}) over-current threshold during the on-time, the PFC output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the PFC output on again.

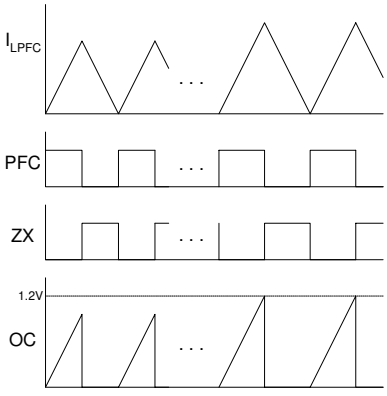


Figure 14: Inductor current, PFC pin, ZX pin and OC pin timing diagram

On-time Modulation Circuit

A fixed on-time of M_{PFC} over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage for high power factor but the total harmonic distortion (THD), as well as the individual higher harmonics, of the current can still be too high. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve low harmonics that are acceptable to international standard organizations and general market requirements, an additional on-time modulation circuit has been added to the PFC control. This circuit dynamically increases the on-time of M_{PFC} as the line input voltage nears the zero-crossings (Fig. 15). This causes the peak L_{PFC} current, and therefore the smoothed line input current, to increase slightly higher near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the THD and higher harmonics to low levels.

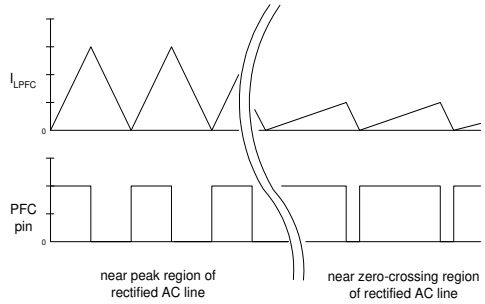


Figure 15: On-time modulation circuit timing diagram

DC Bus Over-voltage Protection

Should over-voltage occur on the DC bus and the VBUS pin exceeds the internal 4.3 V threshold (V_{BUSOV+}), the PFC output is disabled (set to a logic 'low'). When the DC bus decreases again and the V_{BUS} pin decreases below the internal 4.15 V threshold (V_{BUSOV-}), a watch-dog pulse is forced on the PFC pin and normal PFC operation is resumed.

DC Bus Undervoltage Reset

When the input line voltage decreases, the on-time of M_{PFC} increases to keep the DC bus constant. The on-time will continue to increase as the line voltage continues to decrease until the OC pin exceeds the internal 1.2 V over-current threshold (V_{OCTH+}). At this time, the on-time can no longer increase and the PFC can no longer supply enough current to keep the DC bus fixed for the given load power. This will cause the DC bus to begin to decrease. The decreasing DC bus will cause the V_{BUS} pin to decrease below the internal 3.0 V threshold (V_{BUSUV-}) (Fig. 12).

When this occurs, V_{CC} is discharged internally to UVLO. The IRS2168D enters UVLO mode and both the PFC and ballast sections are disabled. The start-up supply resistor to V_{CC}, together with the micro-power start-up current, should be set such that the ballast turns on at an AC line input voltage above the level at which the DC bus begins to drop. The current-sensing resistor at the OC pin sets the maximum PFC current and therefore sets the maximum on-time of M_{PFC}. This prevents saturation of the PFC inductor and programs the minimum low-line input voltage for the ballast. The micro-power supply resistor to V_{CC} and the current-sensing resistor at the OC pin program the on and off input line voltage thresholds for the ballast. With these thresholds correctly set, the ballast will turn off due to the 3.0 V undervoltage threshold (V_{BUSUV-}) on the V_{BUS} pin, and on again at a higher voltage (hysterisis) due to the supply resistor to V_{CC}.

III. Ballast Design Equations

Note: The results from the following design equations can differ slightly from actual measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

Step 1: Program Run Frequency

The run frequency is programmed with the timing resistor R_{FMIN} at the FMIN pin. Use graph in Fig. 16 (R_{FMIN} vs. Frequency) to select R_{FMIN} value for desired run frequency.

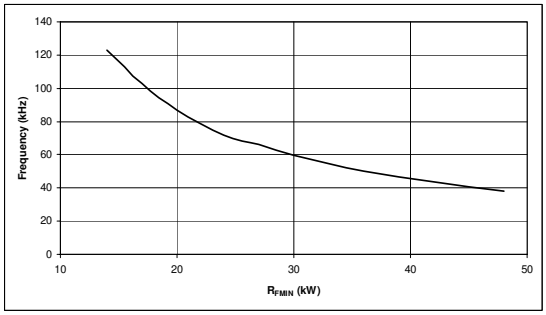


Figure 16: f_{OSC} vs R_{FMIN}

Step 2: Program Preheat Frequency

The preheat frequency is programmed with timing resistors R_{FMIN} and R_{PH}. The timing resistors are connected in parallel for the duration of the preheat time. Use graph in Fig. 14 (R_{FMIN} vs. Frequency) to select R_{EQUIV} value for desired preheat frequency. Then R_{PH} is given as:

$$R_{PH} = \frac{R_{FMIN} \cdot R_{EQUIV}}{R_{FMIN} - R_{EQUIV}} \qquad [\Omega] \quad (1)$$

Step 3: Program Preheat Time and Ignition Time

The preheat time is defined by the time it takes for the external capacitor on pin C_{PH} to charge up to $V_{CPHEOP+}$. An external resistor (R_{CPH}) connected to V_{CC} charges capacitor C_{PH}. The preheat time is therefore given as:

$$t_{PH} \approx R_{CPH} \cdot C_{PH} \qquad [s] \quad (2)$$

or

$$C_{PH} \approx \frac{t_{PH}}{R_{CPH}} \qquad [F] \quad (3)$$

The ignition time is defined by the time it takes for the external capacitor on pin C_{PH} to charge up the second time from $V_{CPHSOI-}$ to V_{CPHRUN}. The ignition time is therefore given as:

$$t_{IGN} \approx 0.4 \cdot t_{PH} \qquad [s] \quad (4)$$

Step 4: Program Ignition Ramp Time

The ignition ramp time is defined by the time it takes for the external capacitor on pin VCO to charge up to 2 V. The external timing resistor (R_{PH}) connected to F_{MIN} charges capacitor C_{VCO}. The ignition ramp time is therefore given as:

$$t_{RAMP} = R_{PH} \cdot C_{VCO} \qquad [s] \quad (5)$$

or

$$C_{VCO} \approx \frac{t_{RAMP}}{R_{PH}} \qquad [F] \quad (6)$$

Step 5: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor R_{CS} and an internal threshold of 1.2 V (V_{CSTH+}). This threshold determines the over-current limit of the ballast, which will be reached when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} \approx \frac{1.2}{R_{CS}} \qquad [A] \text{ (peak)} \quad (7)$$

or

$$R_{CS} \approx \frac{1.2}{I_{IGN}} \qquad [\Omega] \quad (8)$$

IV. PFC Design Equations

Step1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(8e-6)\cdot(VBUS - VAC_{RMS}\sqrt{2})\cdot VAC_{RMS}\cdot\eta}{2\cdot\sqrt{2}\cdot P_{OUT}} \quad [H] \quad (1)$$

where,

$VBUS$ = DC bus voltage
VAC_{RMS} = Nominal rms AC input voltage
η = PFC efficiency (typically 0.95)
P_{OUT} = Ballast output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2\cdot\sqrt{2}\cdot P_{OUT}}{VAC_{MIN}\cdot\eta} \quad [A] \text{ (peak)} \quad (2)$$

where,

VAC_{MIN} = Minimum rms AC input voltage

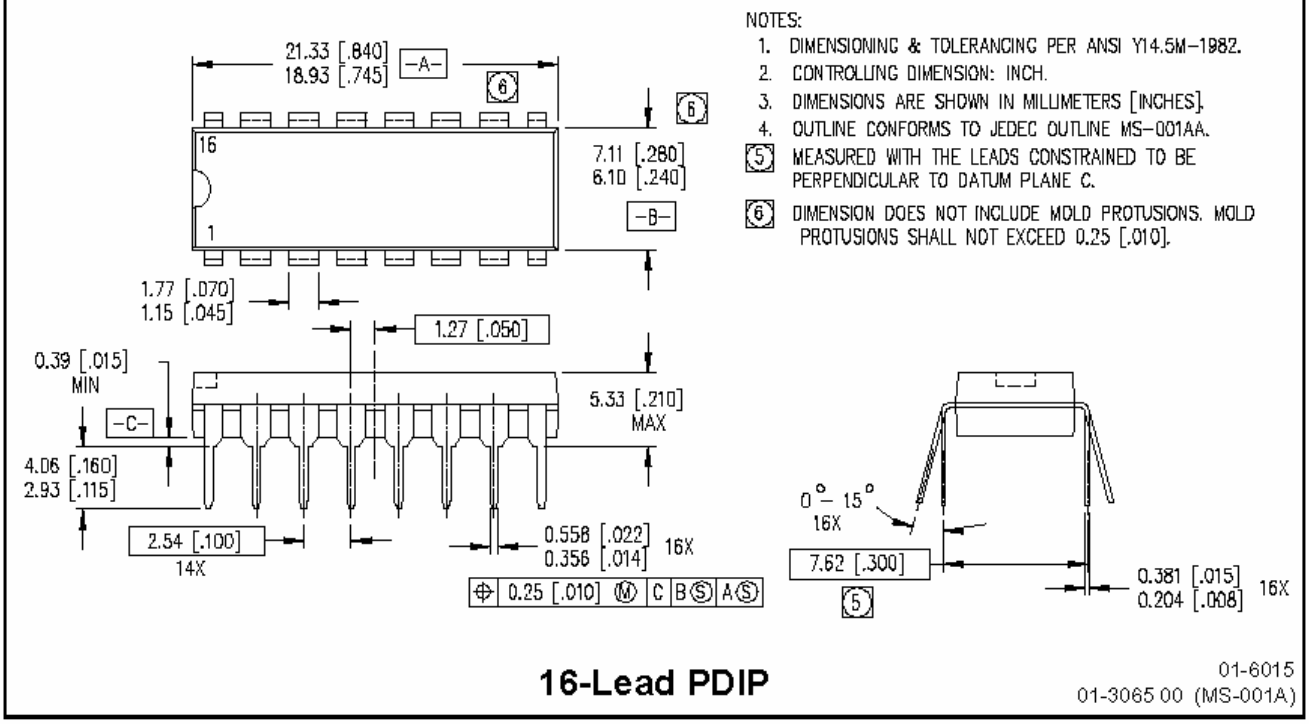
Note: The PFC inductor must not saturate at i_{PK} over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

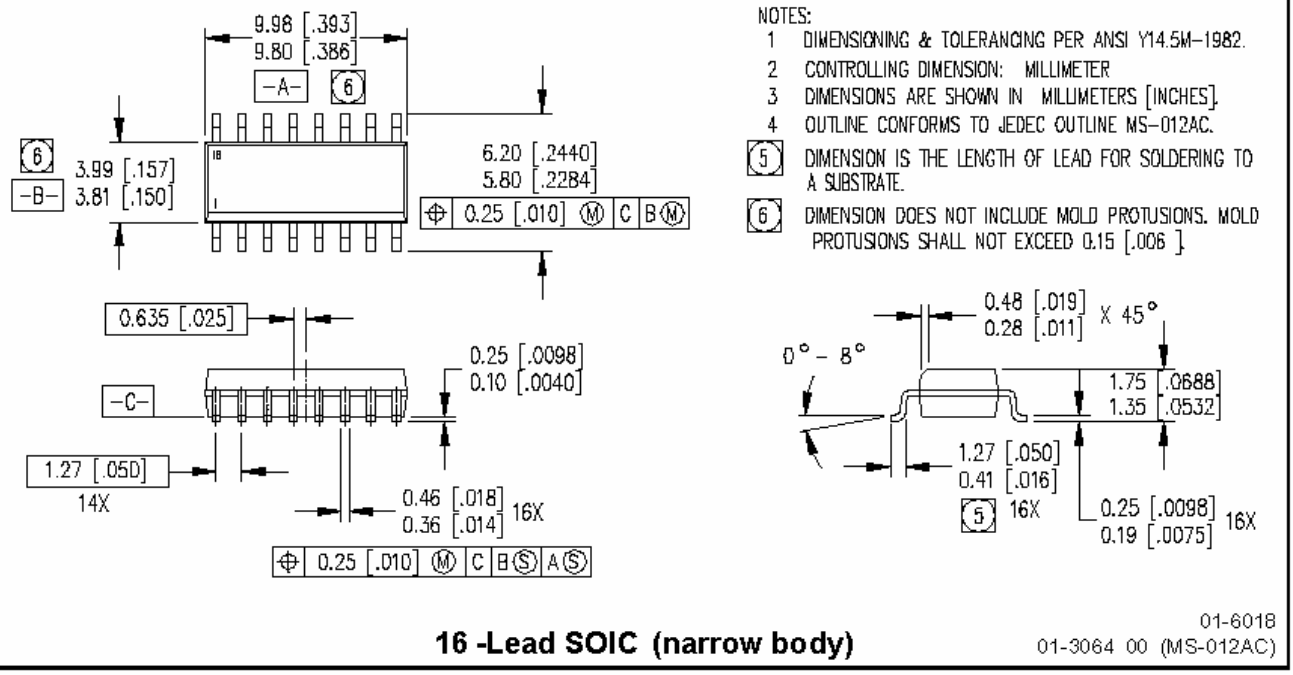
Step 3: Calculate PFC over-current resistor ROC value:

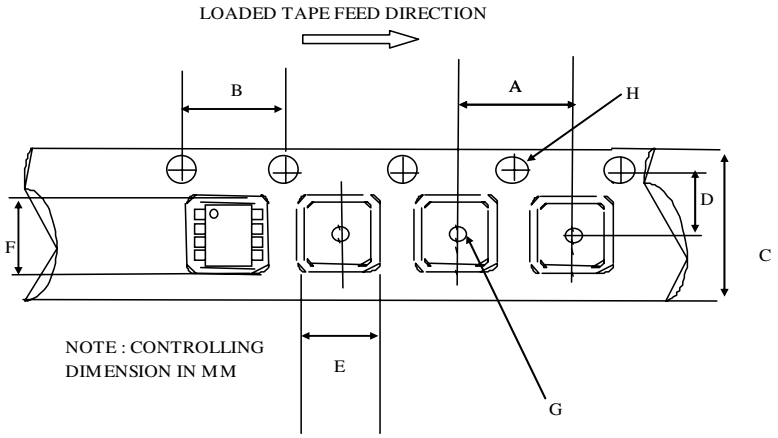
$$R_{OC} = \frac{1.2}{i_{PK}} \quad [\Omega] \quad (3)$$

Step 4: Calculate start-up resistor R_{VCC} value:

$$R_{VCC} = \frac{VAC_{MIN\_PK} + 10}{IQCCUV} \quad [\Omega] \quad (4)$$

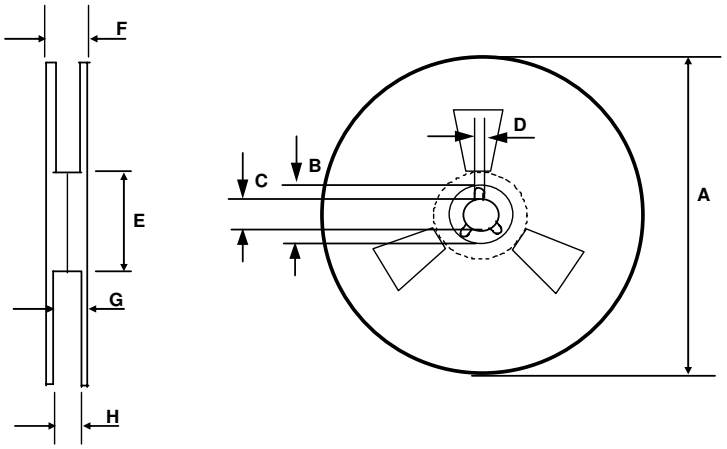

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].
21.33 [.840]
18.93 [.745]
-A-
16
1
7.11 [.280]
6.10 [.240]
-B-
1.77 [.070]
1.15 [.045]
1.27 [.050]
0.39 [.015]
MIN
-C-
5.33 [.210]
MAX
4.06 [.160]
2.93 [.115]
2.54 [.100]
14X
0.558 [.022]
0.356 [.014]
16X
0.25 [.010] M C B S A S
0° - 15°
16X
7.62 [.300]
0.381 [.015]
0.204 [.008]
16X
16-Lead PDIP
01-6015
01-3065 00 (MS-001A)


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].
9.98 [.393]
9.80 [.386]
-A-
6
6
-B-
3.99 [.157]
3.81 [.150]
6.20 [.2440]
5.80 [.2284]
0.25 [.010] M C B M
0.635 [.025]
0.25 [.0098]
0.10 [.0040]
-C-
1.27 [.050]
14X
0.46 [.018]
0.36 [.014]
16X
0.25 [.010] M C B S A S
0.48 [.019]
0.28 [.011]
X 45°
0° - 8°
1.75 [.0688]
1.35 [.0532]
1.27 [.050]
0.41 [.016]
5 16X
0.25 [.0098]
0.19 [.0075]
16X
16 -Lead SOIC (narrow body)
01-6018
01-3064 00 (MS-012AC)



CARRIER TAPE DIMENSION FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
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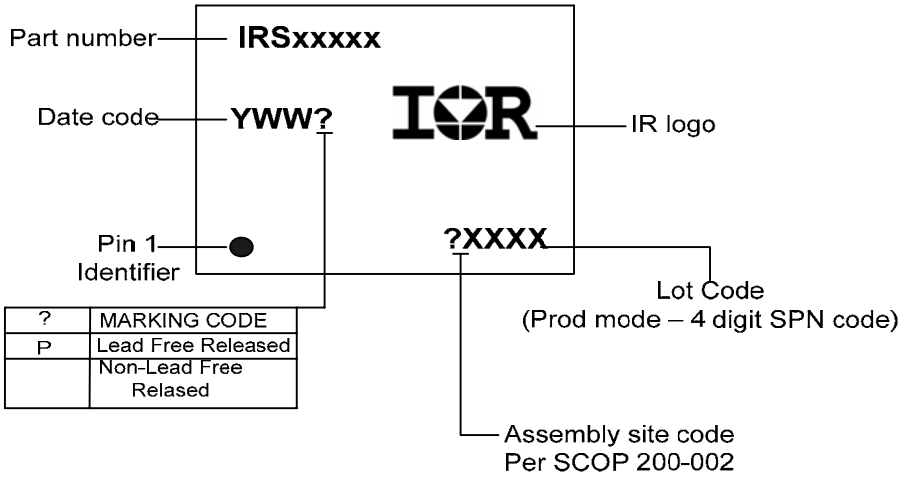
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

16-Lead PDIP IRS2168DPbF
16-Lead SOIC IRS2168DSPbF
16-Lead SOIC Tape & Reel IRS2168DSTRPbF

The SOIC-16 is MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com <http://www.irf.com>
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252-7105
Data and specifications subject to change without notice. 1/26/2007