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International
IOR Rectifier

January 16, 2009
Datasheet No. - PD97375

IRS21956S

Floating Input, High and Low(Dual mode) Side Driver

Features

- Low side programmable ramp gate drive
- Low side generic gate drive integrated using the same low side output pin
- High side generic gate driver
- Under voltage lockout for VDD, VCC & VBS
- Floating 5V input logic compatible
- Tolerant to negative transient voltage on Vs
- Shoot through prevention
- RoHS compliant

Product Summary

Topology	PDP
V_{OFFSET}	≤ 600 V
LO SR_+	4.5V/us
I_{o+} & I_{o-} (typical)	0.5A & 0.5A
t_{ON} & t_{OFF} (typical)	300ns & 280ns

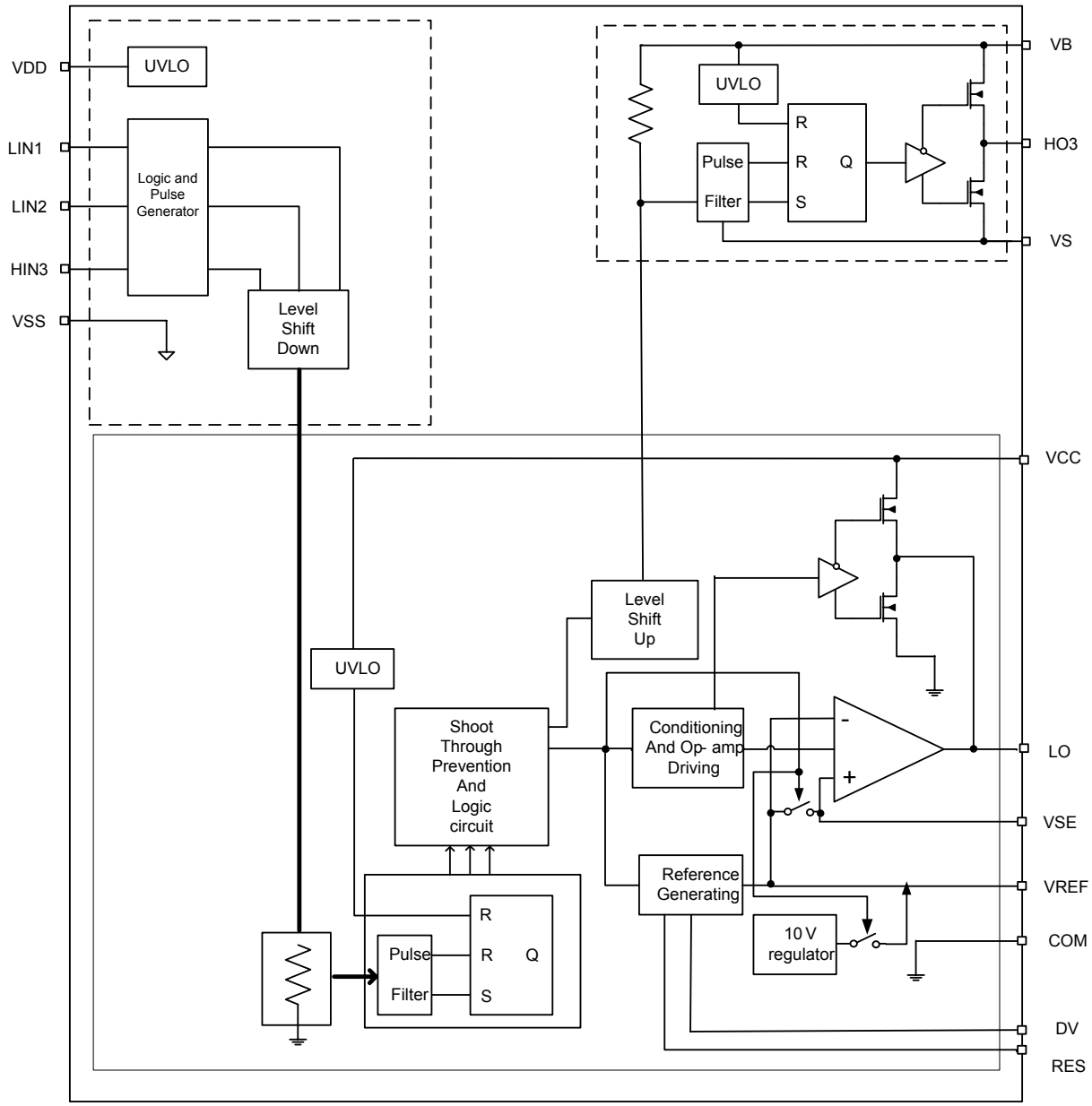
Package Options

20-Lead SOIC

Description

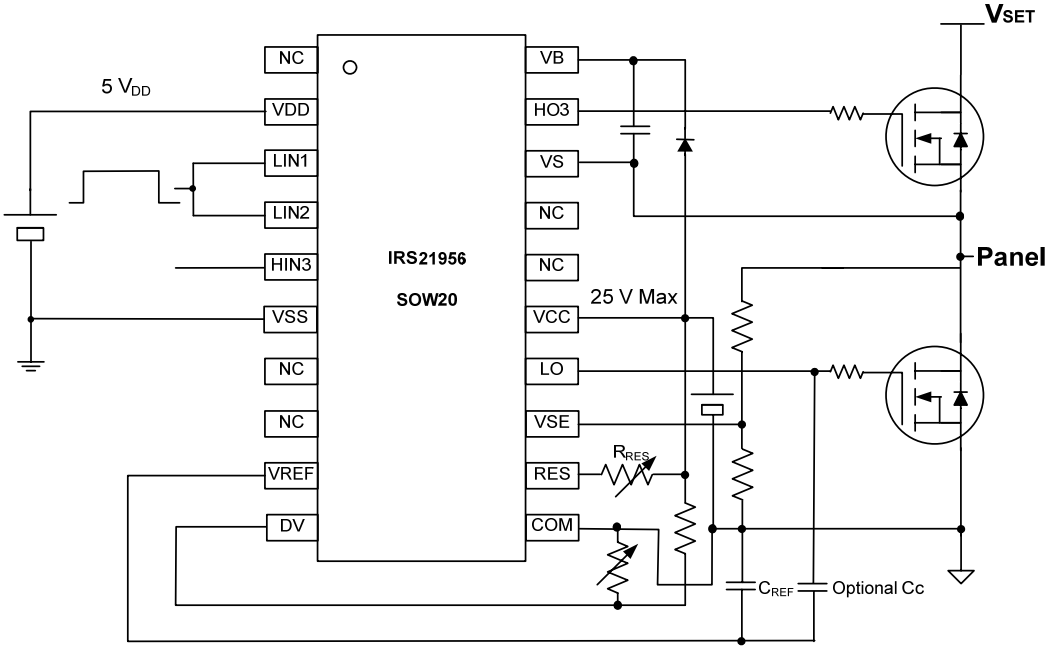
The IRS21956 is high voltage and programmable ramp slope control gate driver for MOSFET and IGBT with single low side dual mode driver, high side driver and floating 5V input. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The floating logic input is compatible with standard 5V CMOS or LSTTL output. The output driver features a programmable slope control by external R/C and input signals. The floating channels can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 600 volts above the COM ground.

Simplified Block Diagram

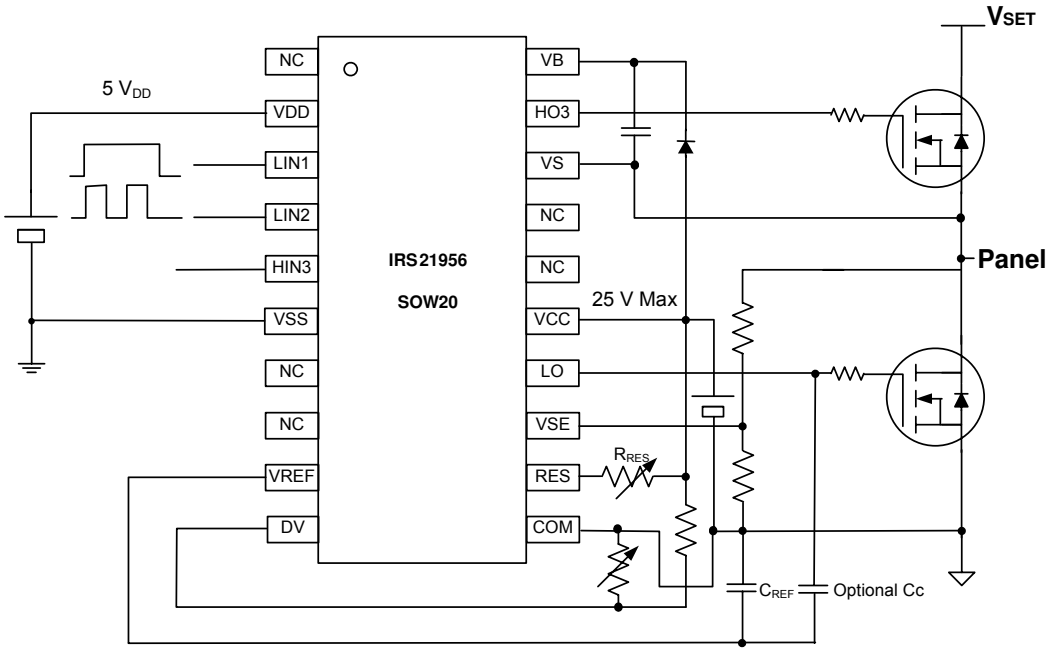


Typical Connection Diagram

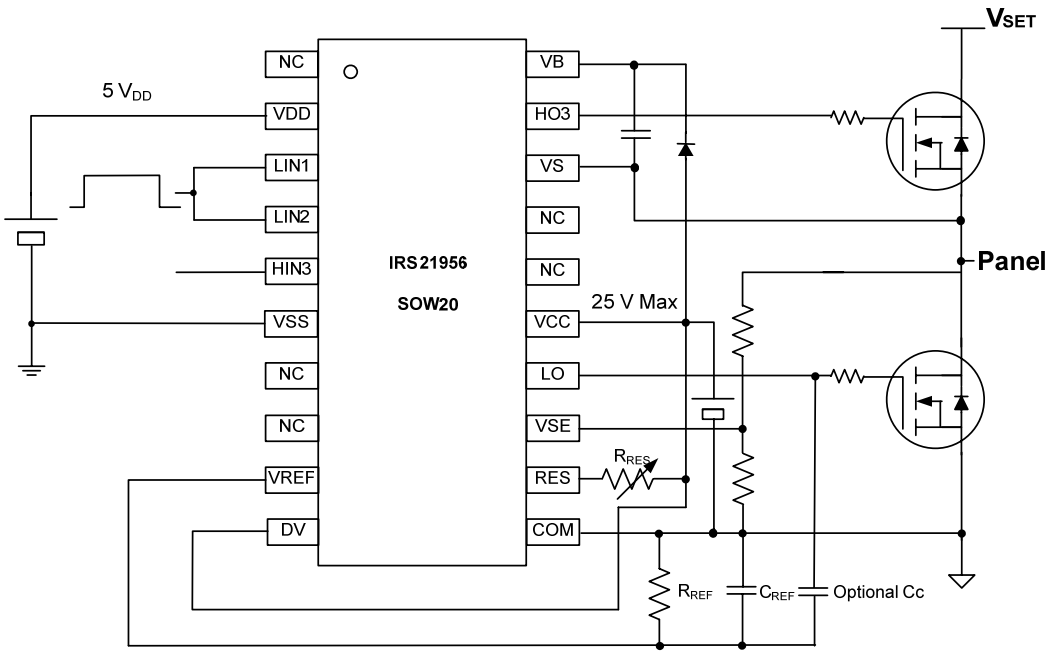
A) Linear Ramp driver's connection diagram



B) Stepwise linear Ramp driver's connection diagram



C) Exponential Ramp driver's connection diagram



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC20W	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
V_{DD}	Floating Input Supply Voltage	-0.3	625	V
V_{SS}	Floating Input Supply Return Voltage	V_{DD} -25	V_{DD} +0.3	V
V_{IN}	Logic input voltage (LIN1,LIN2,HIN3)	V_{SS} -0.3	V_{DD} +0.3	V
V_{CC}	Low side supply voltage	-0.3	25	V
V_{DV}, V_{VREF}	Low side inputs voltage	COM-0.3	V_{CC}+0.3	V
V_{VSE}, V_{RES}	Low side inputs voltage	COM-0.3	V_{CC}+0.3	V
V_{LO}	Low side gate drive output voltage	COM-0.3	V_{CC}+0.3	V
V_B	High side floating well supply voltage	-0.3	625	V
V_S	High side floating well supply return voltage	V_B-25	V_B+0.3	V
V_{HO}	Floating gate drive output voltage	V_S-0.3	V_B+0.3	V
dV_{SS}/dt	Allowable V_{SS} offset supply transient relative to COM	-	50	V/ns
dV_S/dt	Allowable V_S offset supply transient relative to COM	-	50	V/ns
P_D	Package Power Dissipation @ T_A<=+25ºC	-	1.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	120	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	ºC
T_L	Lead temperature (Soldering, 10 seconds)	-	300	ºC

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM.

The offset rating are tested with supplies of (V_{CC}-COM) = (V_B-V_S)=15V.

Symbol	Definition	Min	Max	Units
V_{DD}	Floating Input Supply voltage	V_{SS}+4.5	V_{SS}+6	V
V_{SS}	Floating Input Supply offset voltage	-0.3	600	V
V_{IN}	LIN1, LIN2, HIN3 input voltage	V_{SS}	V_{DD}	V
V_{CC}	Low side supply voltage	10	20	V
V_{LO}	Low side gate drive output voltage	COM	V_{CC}	V
V_{RES}	RES input voltage	COM	V_{CC}	V
V_{DV}	DV input voltage	COM	V_{CC}	V
$V_{VREF, VSE}$	VREF and VSE input voltage	COM	V_{CC}-3	V
V_B	High side floating well supply voltage	V_S+10	V_S+20	V
V_S	High side floating well supply offset voltage	Note2††	600	V
V_{HO}	Floating gate drive output voltage	V_S	V_B	V
T_A	Ambient Temperature	-40	125	ºC

† V_S and V_B voltages will be tolerant to short negative transient spikes. These will be defined and specified in the future.

†† Logic operation for Vs of -5 to 600V. Logic state held for Vs of -5V to $-V_{BS}$. (Please refer to Design Tip DT97-3 for more details).

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S)=15V. T_A = 25ºC. The V_{IN}, $V_{IN\,TH}$ and I_{IN} parameters are referenced to V_{SS}. The V_O and I_O parameters are referenced to respective VS, COM and are applicable to the respective output leads HO3, LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S. The V_{DDUV} parameters are referenced to V_{SS}.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{DDUV+}	V_{DD} supply undervoltage positive going threshold		4.0		V	
V_{DDUV-}	V_{DD} supply undervoltage negative going threshold		3.9			
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.8	8.7	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.0	8.8		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.8	8.7	9.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.2	8.0	8.8		
I_{LK1}	High side floating well offset supply leakage current	---	---	50	uA	V_B = V_S = 600V
I_{LK2}	High side floating well offset supply leakage current	---	---	50		V_{DD} = V_{SS} = 300V
I_{QDD}	Quiescent VDD supply current	---	145	250	uA	IN1, 2, 3 = 0Vor 5V
I_{QBS}	Quiescent VBS supply current	---	65	120	uA	HIN3 = 5V or 0V
I_{QCC}	Quiescent VCC supply current	---	1	1.5	mA	LIN1, 2 = 0V, RES=130kohm
		---	5	7	mA	LIN1, 2 = 5V, RES=130kohm
V_{IH}	Logic “1” input voltage	3.5	---	---	V	
V_{IL}	Logic “0” input voltage	---	---	0.8		
I_{IN+}	Logic “1” input bias current	---	5	---	uA	V_{IN}= 5V
I_{IN-}	Logic “0” input bias current	---	0	---		V_{IN}= 0V
$I_{o+\_HO3, LO}$	Output high short circuit pulsed current	---	0.5	---	A	V_O=15V,V_{IN}=5V, PW<=10us
$I_{o-\_HO3, LO}$	Output low short circuit pulsed current	---	0.5	---		V_O=0V,V_{IN}=0V, PW<=10us
$V_{OL\_HO3, LO}$	Low level output voltage	---	35	150	mV	Io=2mA
$V_{OH\_HO3, LO}$	High level output voltage, Vbias-Vo	---	15	80		Io=2mA
DV exp+	Positive DV input threshold for exponential ramp	---	10	---	V	C_{REF} =1nF, V_{SE} open R_{RES} =130K

DV / Linear (Stepwise) Mode

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VREF, hold	DV reference voltage	0.4	0.5	0.6	V	DV=500mV, C_{REF} =1nF, V_{SE} open R_{RES} =130K,
		2.82	3	3.18		DV=3V, C_{REF} =1nF, V_{SE} open R_{RES} =130K,

Dynamic Electrical Characteristics

(V_{CC}-COM)= (V_B-V_S)=15V. TA = 25ºC. C_L = 1000pF unless otherwise specified. All parameters are reference to COM.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Internal Operational Amplifier Characteristics						
$t_{ref\_ln\_ramp}$	Linear ramp reference 10% to 90%	130	190	250	µs	C_{REF} =1nF, V_{SE} open R_{RES} =130K, V_{DV} =COM
Gm	OTA transconductance	---	12	---	mS	CL_LO=1nF, V_{DV} =V_{CC}, R_{RES} =130K, dc bias 5V
$G_{open\ loop}$	Open loop gain	45	60	---	dB	Cc =1nF, V_{DV} =V_{CC}, R_{RES} =130K
BW_{SS}	Small signal bandwidth	---	3.5	---	MHz	Cc =1nF V_{DV} =V_{CC}, R_{RES} =130K
V_{OS}	Input offset voltage	---	20	---	mV	V_{DV} =V_{CC}, R_{RES} =130K
LO_{SR+}	Output positive slew rate	---	4.5	---	V/µs	CL_LO=1nF, V_{DV} =V_{CC}, R_{RES} =130K
CMRR	Common mode rejection ratio	55	65	---	dB	V_{DV} =V_{CC}, R_{RES} =130K
PSRR	Power supply rejection ratio	55	65	---	dB	V_{DV} =V_{CC}, R_{RES} =130K
Propagation Delay Characteristics						
t_{on}	Turn-on delay (HO3, LO)	---	300	400	ns	Gate Drive Mode C_L =1nF
t_{off}	Turn-off delay (HO3, LO)	---	280	380		
t_r	Turn-on rise from 10% to 90%	---	25	60		
t_f	Turn-off fall from 90% to 10%	---	15	40		
MT	Delay matching, HO3 & LO turn-on/off			50		

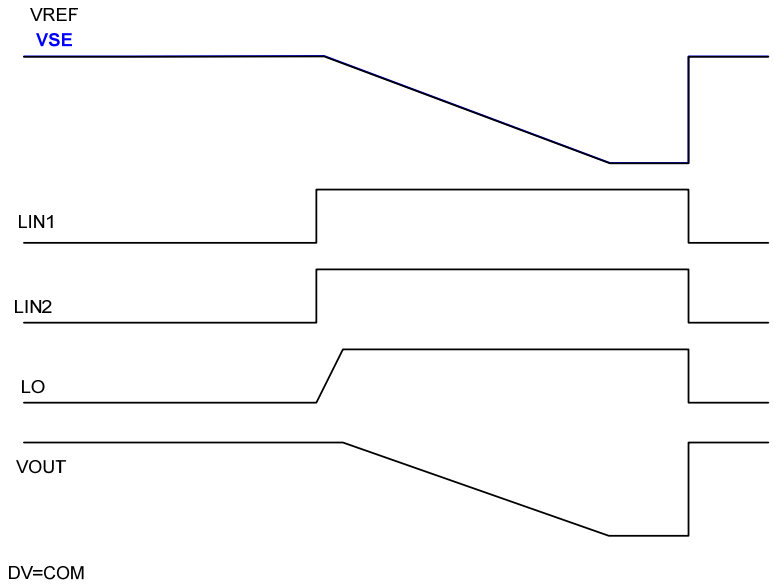


Figure 1A1 Input/Output Timing Diagram: Linear Ramp

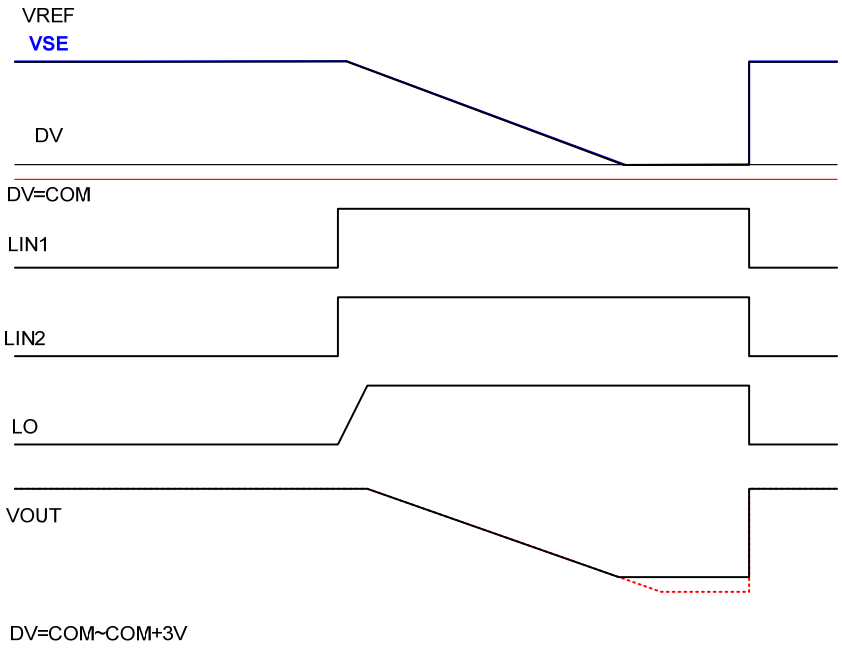


Figure 1A2 Input/Output Timing Diagram: Linear Ramp with voltage difference

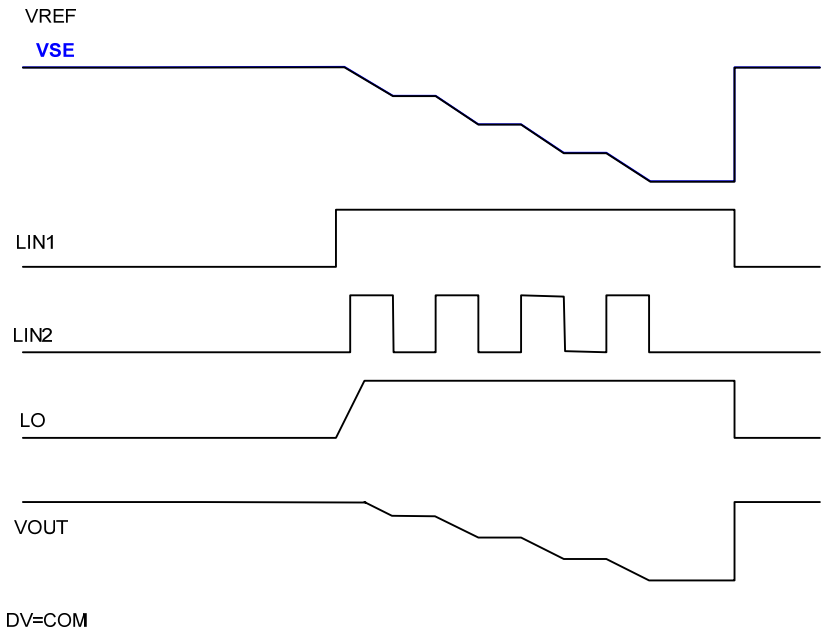


Figure 1B Input/Output Timing Diagram: Stepwise linear Ramp

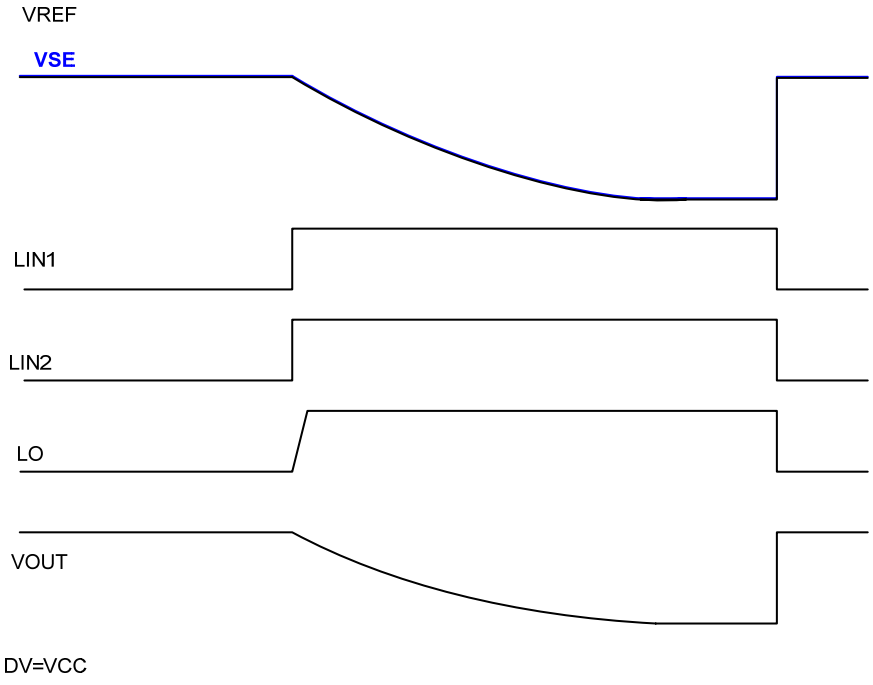


Figure 1C Input/Output Timing Diagram: Exponential Ramp

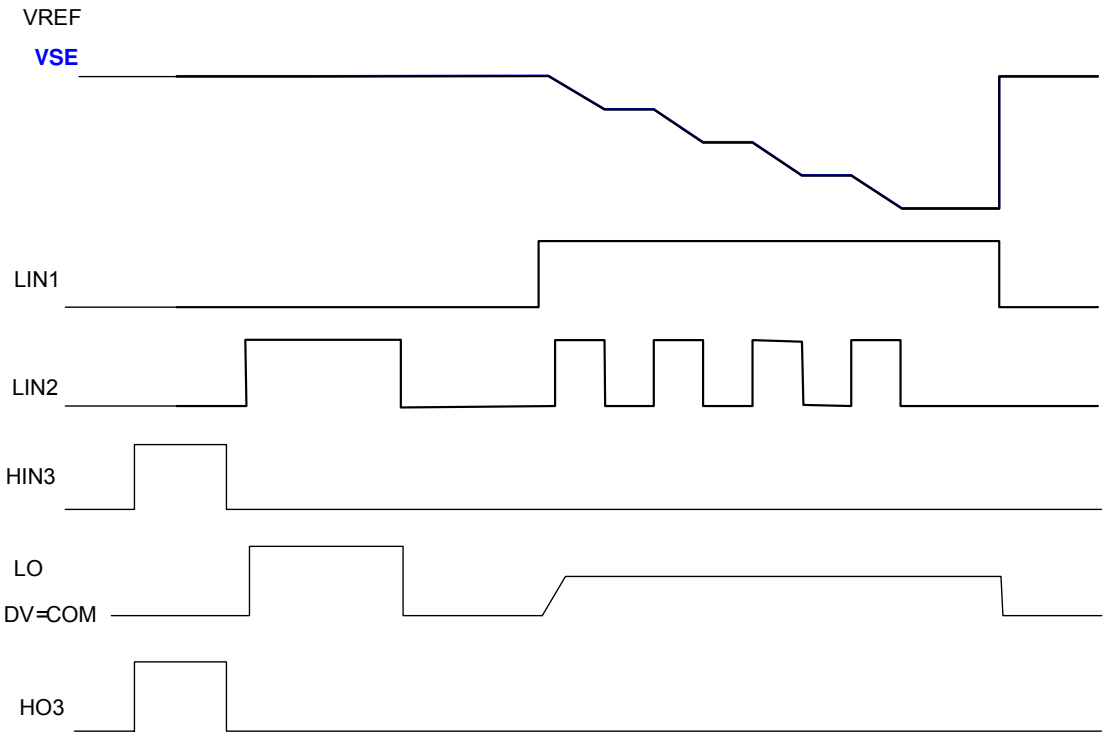


Figure 1D Input/Output Timing Diagram : LO/HO3 outputs

Logic Truth Table

LIN1	LIN2	HIN3	HO3	OTA of LO	Gate driver of LO
0	0	0	0	High impedance (HIZ)	0
0	0	1	1	High impedance (HIZ)	0
0	1	0	0	High impedance (HIZ)	1
0	1	1	0	High impedance (HIZ)	0
1	1	0	0	Linear/Exp ramp depend on DV pin	High impedance (HIZ)
1	1	1	0	High impedance (HIZ)	0
1	Step(0/1)	0	0	Stepwise linear if DV pin is COM	High impedance (HIZ)
1	Step(0/1)	1	0	High impedance (HIZ)	0

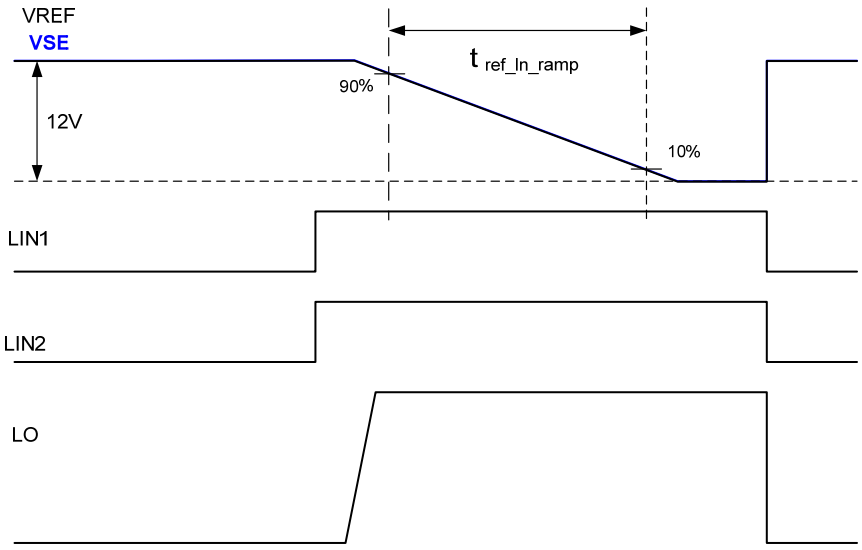


Figure 2 Timing Definitions of V_{REF}

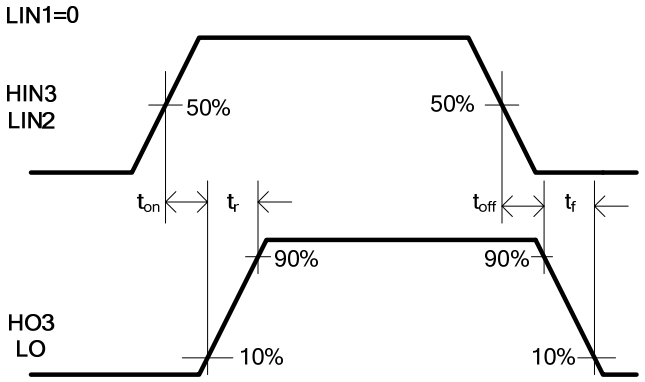


Figure 3 Switching Time Waveform Definitions of LO and HO3

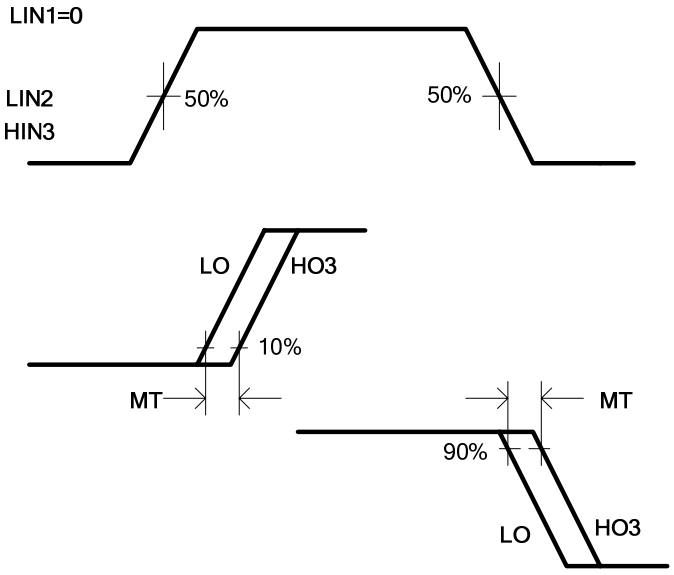
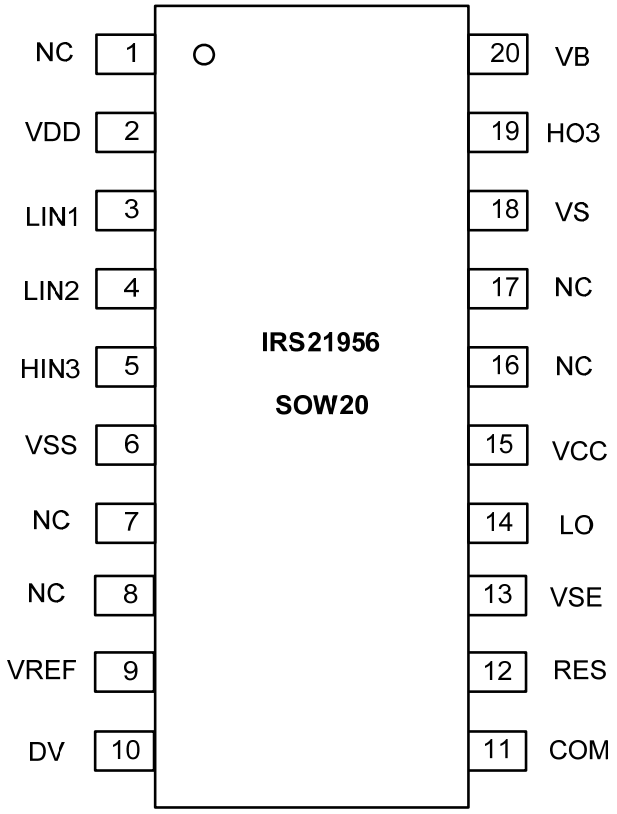
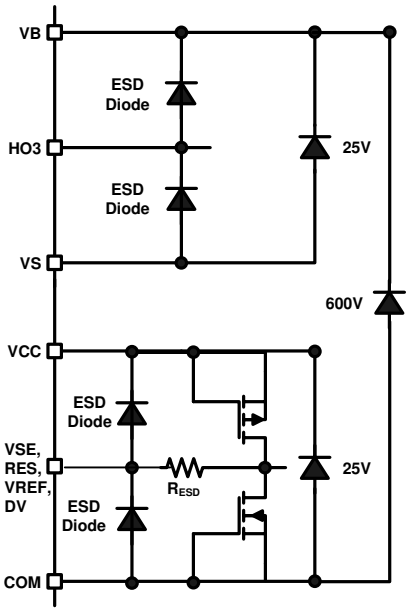
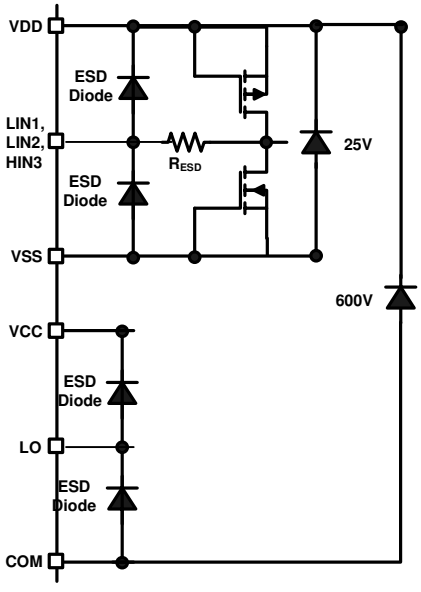


Figure 4 Delay Matching Waveform Definitions

Input/Output Pin Equivalent Circuit Diagram



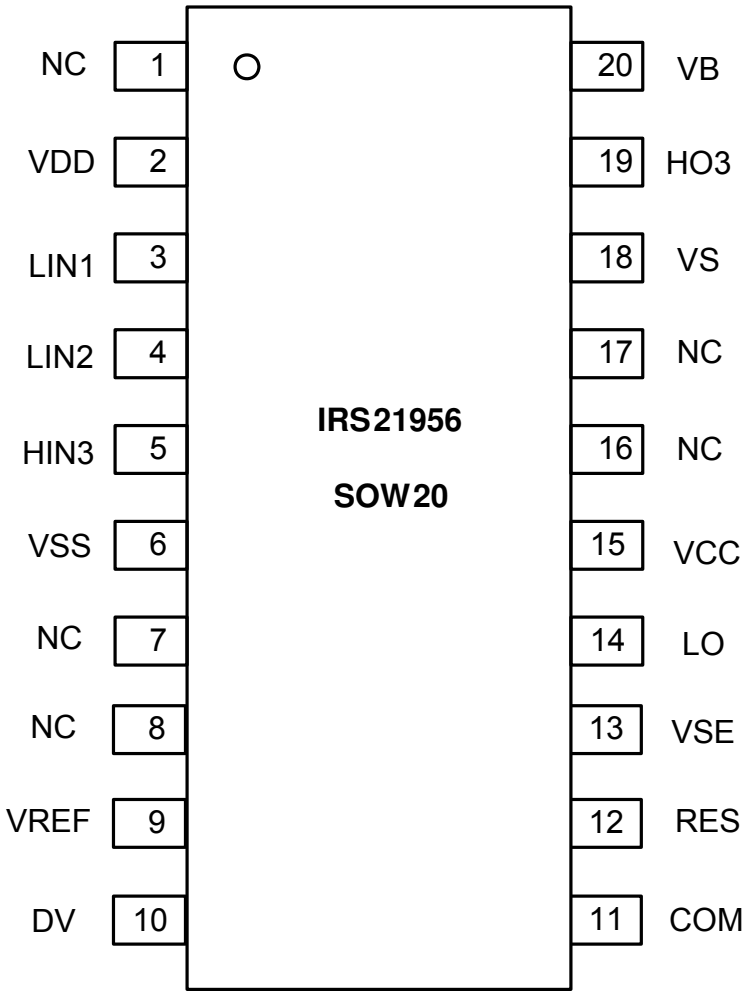




Lead Definitions

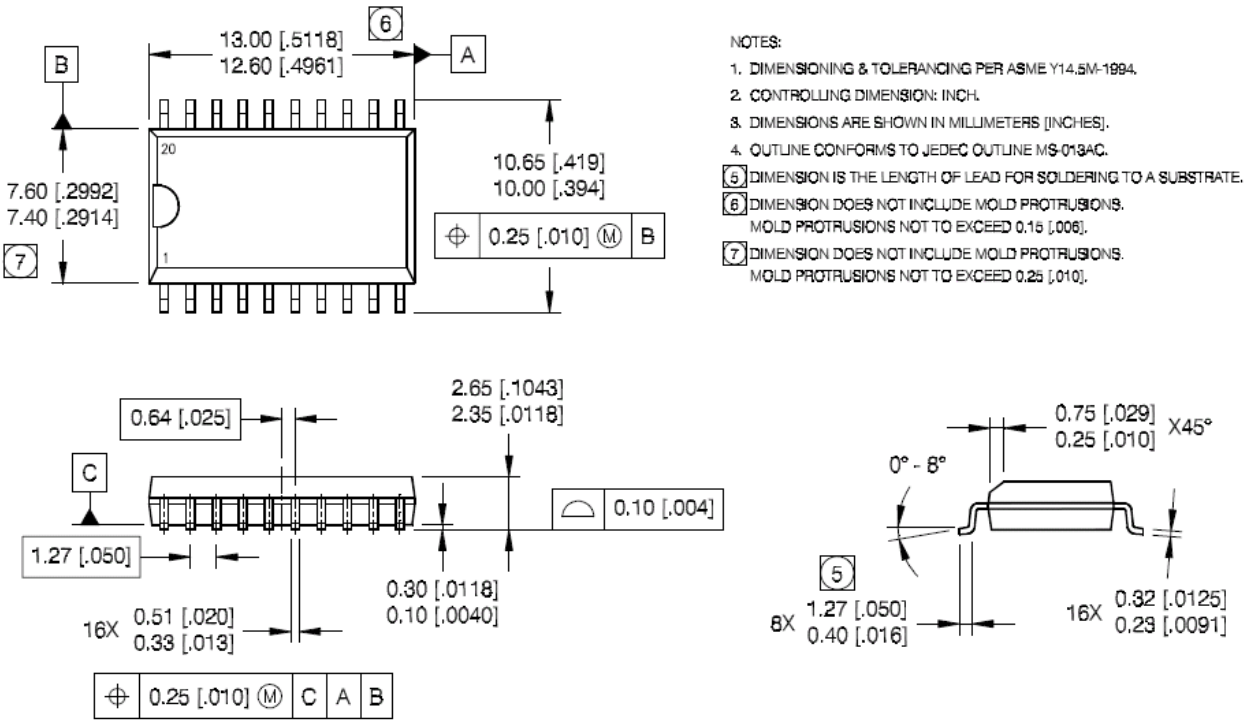
PIN#	Symbol	Description
1	NC	No Connection
2	VDD	Floating input supply voltage
3	LIN1	Logic input for LO ramp control
4	LIN2	Logic input for low side gate driver outputs, in phase
5	HIN3	Logic input for high side gate driver output
6	VSS	Floating input supply return
7	NC	No Connection
8	NC	No Connection
9	VREF	External programmable R/C input for ramp generation
10	DV	Ramp selection and programmable difference voltage (DV) input
11	COM	Low side supply return
12	RES	Adjustable current source resistor input
13	VSE	Voltage sense input
14	LO	Low side gate driver output
15	VCC	Low side supply voltage
16	NC	No Connection
17	NC	No Connection
18	VS	High side gate drive floating supply return
19	HO3	High side gate driver output
20	VB	High side gate drive floating supply

Lead Assignments



Package 20 pin SOW

Package Information



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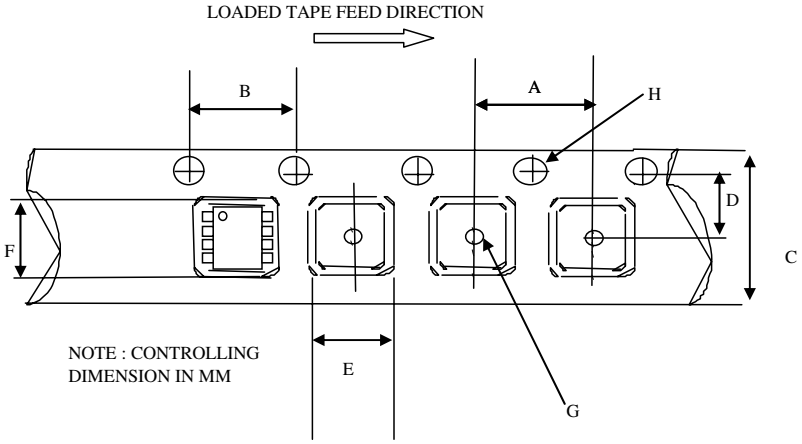
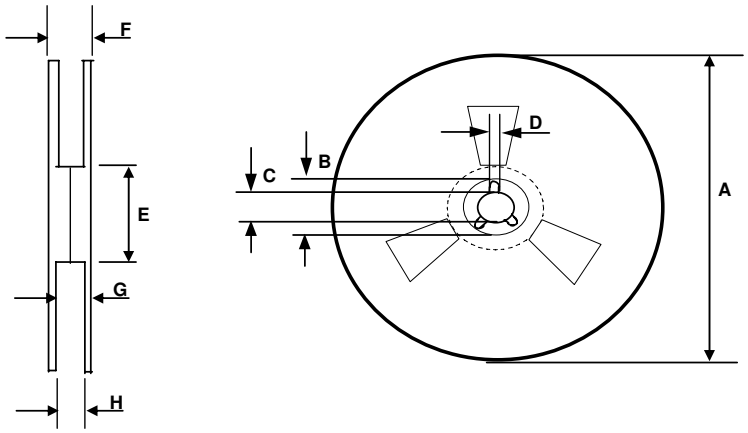


CARRIER TAPE DIMENSION FOR 20SOICW

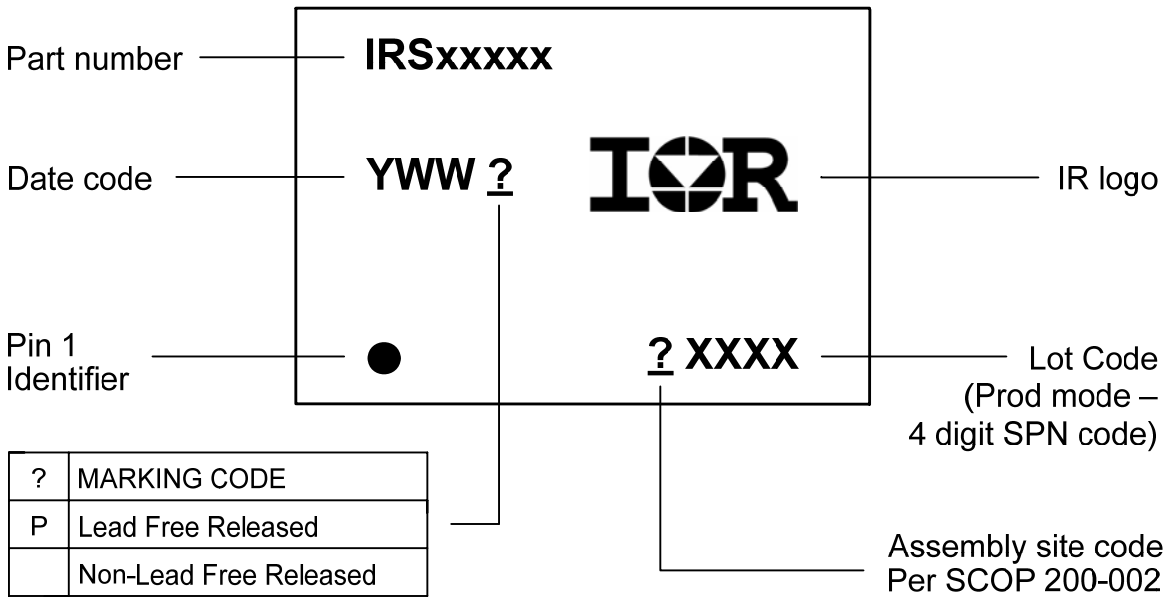
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	13.20	13.40	0.520	0.528
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 20SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS21956	SOIC20W	Tube/Bulk	38	IRS21956SPBF
		Tape and Reel	1000	IRS21956STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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