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International
IOR Rectifier

April 26, 2011

IRS2336(D)
IRS23364D

HIGH VOLTAGE 3 PHASE GATE DRIVER IC

Features

- Drives up to six IGBT/MOSFET power devices
- Gate drive supplies up to 20 V per channel
- Integrated bootstrap functionality (IRS2336(4)D)
- Over-current protection
- Over-temperature shutdown input
- Advanced input filter
- Integrated deadtime protection
- Shoot-through (cross-conduction) protection
- Undervoltage lockout for V_{CC} & V_{BS}
- Enable/disable input and fault reporting
- Adjustable fault clear timing
- Separate logic and power grounds
- 3.3 V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Matched propagation delays for all channels
- -40°C to 125°C operating range
- RoHS compliant
- Lead-Free

Product Summary

Topology		3 Phase
V_{OFFSET}		≤ 600 V
V_{OUT}	IRS2336(D)	10 V – 20 V
	IRS23364D	11.5 V – 20 V
I_{o+} & I_{o-} (typical)		200 mA & 350 mA
t_{ON} & t_{OFF} (typical)		530 ns & 530 ns
Deadtime (typical)		275 ns

Package Options

28-Lead PDIP

28-Lead SOIC Wide Body

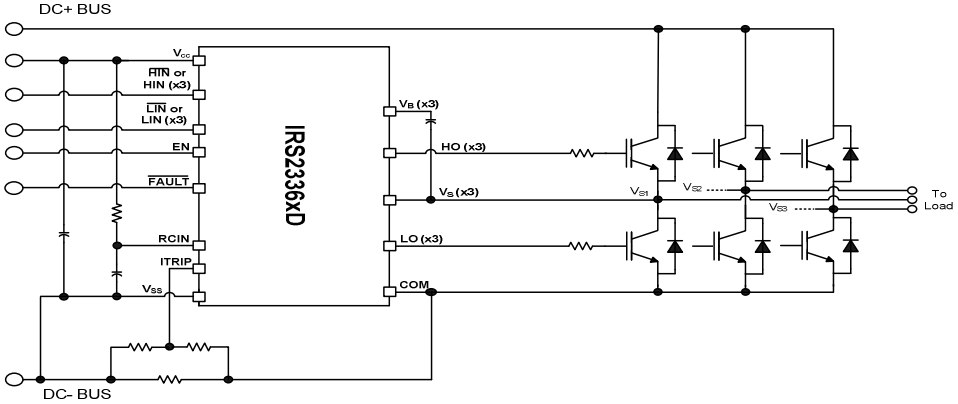
48-Lead MLPQ7X7
(without 14 leads)

44-Lead PLCC
(without 12 leads)

Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Typical Connection Diagram



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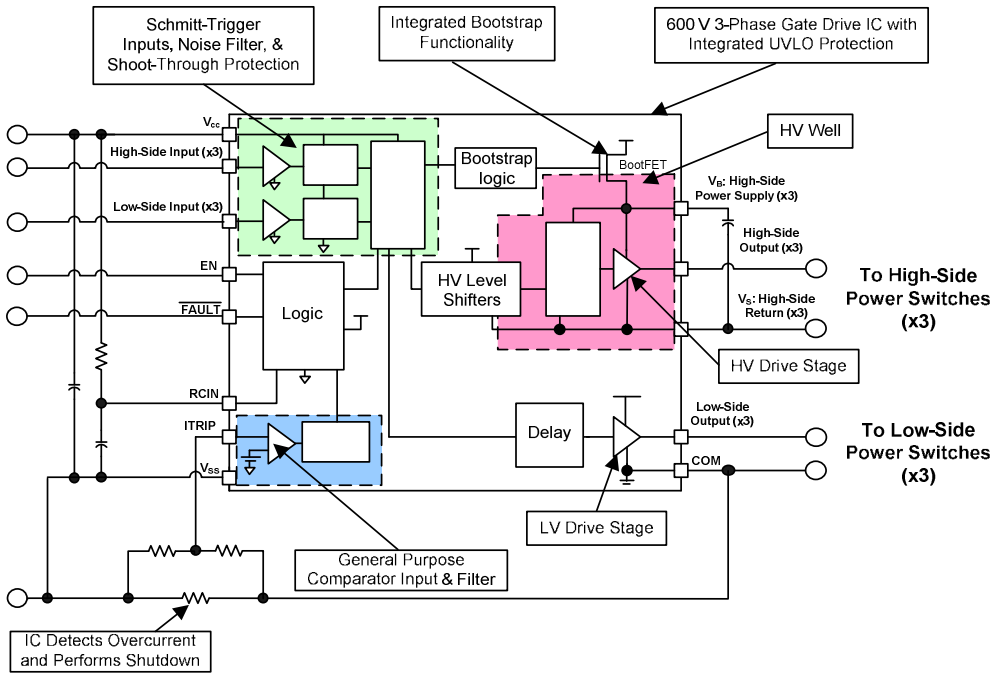
Description

The IRS2336xD are high voltage, high speed, power MOSFET and IGBT gate drivers with three high-side and three low-side referenced output channels for 3-phase applications. This IC is designed to be used with low-cost bootstrap power supplies; the bootstrap diode functionality has been integrated into this device to reduce the component count and the PCB size. Proprietary HVIC and latch immune CMOS technologies have been implemented in a rugged monolithic structure. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3 V logic). A current trip function which terminates all six outputs can be derived from an external current sense resistor. Enable functionality is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that a fault (e.g., over-current, over-temperature, or undervoltage shutdown event) has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Shoot-through protection circuitry and a minimum deadtime circuitry have been integrated into this IC. Propagation delays are matched to simplify the HVIC's use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high-side configuration, which operate up to 600 V.

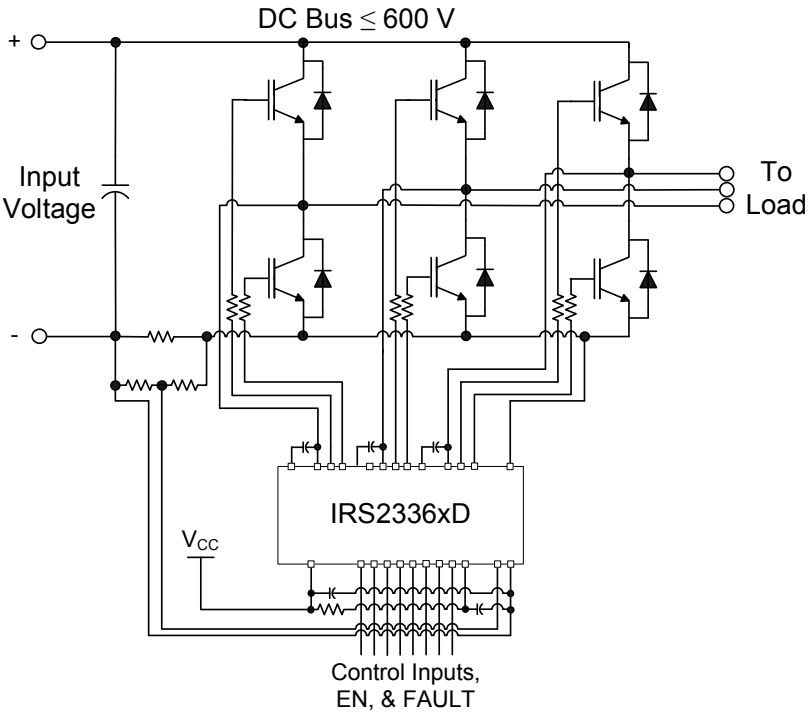
Feature Comparison: IRS2336xD Family

Part Number	Input Logic	UVLO	$V_{IT,TH}$	t_{ON}, t_{OFF}	V_{OUT}
IRS2336(D)	HIN/N, LIN/N	8.9 V/ 8.2 V	0.46 V	530 ns, 530 ns	10 V – 20 V
IRS23364D	HIN, LIN	11.1 V/ 10.9 V	0.46 V	530 ns, 530 ns	11.5 V – 20 V

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC28W	MSL3†††, 260°C (per IPC/JEDEC J-STD-020)
		MLPQ7X7	
		PLCC44	MSL3†††, 245°C (per IPC/JEDEC J-STD-020)
		PDIP28	Not applicable (non-surface mount package style)
ESD	Human Body Model	Class 1C (per JEDEC standard JESD22-A114)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
	Charged Device Model ††††	Class IV (per JEDEC standard JESD22-C101)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† Charged Device Model classification is based on SOIC28W package.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20 V), and V_B & V_S (20 V).

Symbol	Definition		Min	Max	Units
V_{CC}	Low side supply voltage		-0.3	20†	V
V_{IN}	Logic input voltage (HIN, LIN, ITRIP, EN)	IRS2336(D)	V_{SS}-0.3	V_{SS}+5.2	
		IRS23364D	V_{SS}-0.3	V_{CC}+0.3	
V_{RCIN}	RCIN input voltage		V_{SS}-0.3	V_{CC}+0.3	
V_B	High-side floating well supply voltage		-0.3	620†	
V_S	High-side floating well supply return voltage		V_B-20†	V_B+0.3	
V_{HO}	Floating gate drive output voltage		V_S-0.3	V_B+0.3	
V_{LO}	Low-side output voltage		COM-0.3	V_{CC}+0.3	
V_{FLT}	Fault output voltage		V_{SS}-0.3	V_{CC}+0.3	
COM	Power ground		V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Allowable V_S offset supply transient relative to V_{SS}		—	50	V/ns
PW_{HIN}	High-side input pulse width		500	—	ns
P_D	Package power dissipation @ $T_A \leq +25°C$	28-Lead PDIP	—	1.5	W
		28-Lead SOICW	—	1.6	
		44-Lead PLCC	—	2.0	
		48-Lead MLPQ7X7	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient	28-Lead PDIP	—	83	°C/W
		28-Lead SOICW	—	78	
		44-Lead PLCC	—	63	
		48-Lead MLPQ7X7	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are tested at 25 V. An internal 20 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC}-COM) = (V_B-V_S) = 15 V.

Symbol	Definition		Min	Max	Units
V_{CC}	Low-side supply voltage	IRS2336(D)	10	20	V
		IRS23364D	11.5	20	
V_{IN}	HIN, LIN, & EN input voltage	IRS2336(D)	V_{SS}	V_{SS}+5	
		IRS23364D		V_{CC}	
V_B	High-side floating well supply voltage	IRS2336(D)	V_S+10	V_S+20	
		IRS23364D	V_S+11.5	V_S+20	
V_S	High-side floating well supply offset voltage†		COM-8	600	
V_S(t)	Transient high-side floating supply voltage††		-50	600	
V_{HO}	Floating gate drive output voltage		V_s	V_B	
V_{LO}	Low-side output voltage		COM	V_{CC}	
COM	Power ground		-5	5	
V_{FLT}	FAULT output voltage		V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage		V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage		V_{SS}	V_{SS}+5	
T_A	Ambient temperature		-40	125	ºC

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative V_S of V_{SS} - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	IRS2336(D)	8	8.9	9.8	V	NA
		IRS23364D	10.4	11.1	11.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	IRS2336(D)	7.4	8.2	9		
		IRS23364D	10.2	10.9	11.4		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	IRS2336(D)	0.3	0.7	—		
		IRS23364D	—	0.2	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	IRS2336(D)	8	8.9	9.8		
		IRS23364D	10.4	11.1	11.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	IRS2336(D)	7.4	8.2	9		
		IRS23364D	10.2	10.9	11.4		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	IRS2336(D)	0.3	0.7	—		
		IRS23364D	—	0.2	—		
I_{LK}	High-side floating well offset supply leakage		—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current		—	70	120		All inputs are in the off state
I_{QCC}	Quiescent V_{CC} supply current	IRS2336	—	2	3	mA	
		IR2336(4)D	—	3	4		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O		—	0.90	1.4	V	I_O= 20 mA
V_{OL}	Low level output voltage drop, V_O		—	0.40	0.6	V	
I_{o+}	Output high short circuit pulsed current		120	200	—	mA	V_O=0 V,V_{IN}=0 V, PW ≤ 10 µs
I_{o-}	Output low short circuit pulsed current		250	350	—		V_O=15 V,V_{IN}=5 V, PW ≤ 10 µs
V_{IH}	Logic “0” input voltage		2.5	—	—	V	NA
	Logic “1” input voltage						
V_{IL}	Logic “1” input voltage		—	—	0.8		
	Logic “0” input voltage						
$V_{IN,CLAMP}$	Input voltage clamp (HIN, LIN, ITRIP and EN)	IRS2336(D)	4.8	5.2	5.65		I_{IN} = 100 µA
I_{HIN+}	Input bias current (HO = High)	IRS2336(D)	—	150	200	µA	V_{IN} = 0 V
		IRS23364D	—	120	165		V_{IN} = 4 V
I_{HIN-}	Input bias current (HO = Low)	IRS2336(D)	—	110	150		
		IRS23364D	—	—	1		V_{IN} = 0 V
I_{LIN+}	Input bias current (LO = High)	IRS2336(D)	—	150	200		
		IRS23364D	—	120	165		V_{IN} = 4 V
I_{LIN-}	Input bias current (LO = Low)	IRS2336(D)	—	110	150		
		IRS23364D	—	—	1		V_{IN} = 0 V
$V_{RCIN,TH}$	RCIN positive going threshold		—	8	—	V	NA
$V_{RCIN,HY}$	RCIN hysteresis		—	3	—		
I_{RCIN}	RCIN input bias current		—	—	1	µA	V_{RCIN} = 0 V or 15 V
$R_{ON,RCIN}$	RCIN low on resistance		—	50	100	Ω	I = 1.5 mA

Static Electrical Characteristics (continued)

Symbol	Definition		Min	Typ	Max	Units	Test Conditions
$V_{IT,TH+}$	ITRIP positive going threshold		0.37	0.46	0.55	V	NA
$V_{IT,TH-}$	ITRIP negative going threshold		—	0.4	—		
$V_{IT,HYS}$	ITRIP hysteresis		—	0.07	—		
I_{ITRIP+}	"High" ITRIP input bias current	IRS2336(D)	—	5	20	µA	V_{IN} = 4 V
		IRS23364D	—	5	40		
I_{ITRIP-}	"Low" ITRIP input bias current		—	—	1		V_{IN} = 0 V
$V_{EN,TH+}$	Enable positive going threshold		—	—	2.5	V	NA
$V_{EN,TH-}$	Enable negative going threshold		0.8	—	—		
I_{EN+}	"High" enable input bias current	IRS2336(D)	—	5	20	µA	V_{IN} = 4 V
		IRS23364D	—	120	165		
I_{EN-}	"Low" enable input bias current		—	—	1		V_{IN} = 0 V
$R_{ON,FLT}$	FAULT low on resistance		—	50	100	Ω	I = 1.5 mA
R_{BS}	Internal BS diode Ron	(IRS2336(4)D)	—	200	—		NA

Dynamic Electrical Characteristics

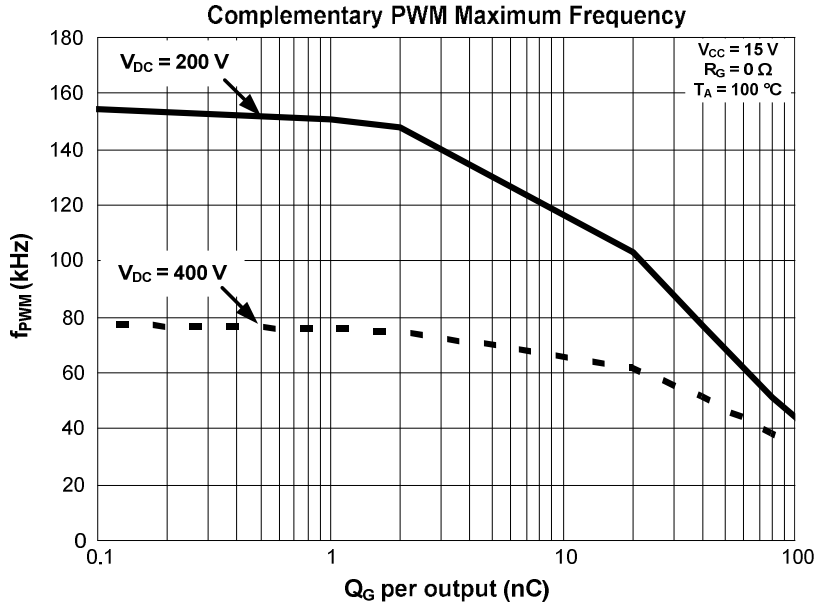
V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{ON}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0 V & 5 V
t_{OFF}	Turn-off propagation delay	400	530	750		
t_R	Turn-on rise time	—	125	190		
t_F	Turn-off fall time	—	50	75		
$t_{FIL,IN}$	Input filter time† (HIN, LIN, ITRIP)	200	350	510		
t_{EN}	Enable low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or 5 V
$t_{FILTER,EN}$	Enable input filter time	100	200	—		NA
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1200	ns	V_{ITRIP} = 5 V
t_{BL}	ITRIP blanking time	—	400	—		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	950		
DT	Deadtime	190	275	420		V_{IN} = 0 V & 5 V without external deadtime
MDT	DT matching††	—	—	60		
MT	Delay matching time (t_{ON}, t_{OFF}) ††	—	—	50		V_{IN} = 0 V & 5 V with external deadtime larger than DT
PM	Pulse width distortion†††	—	—	75		PW input=10 µs

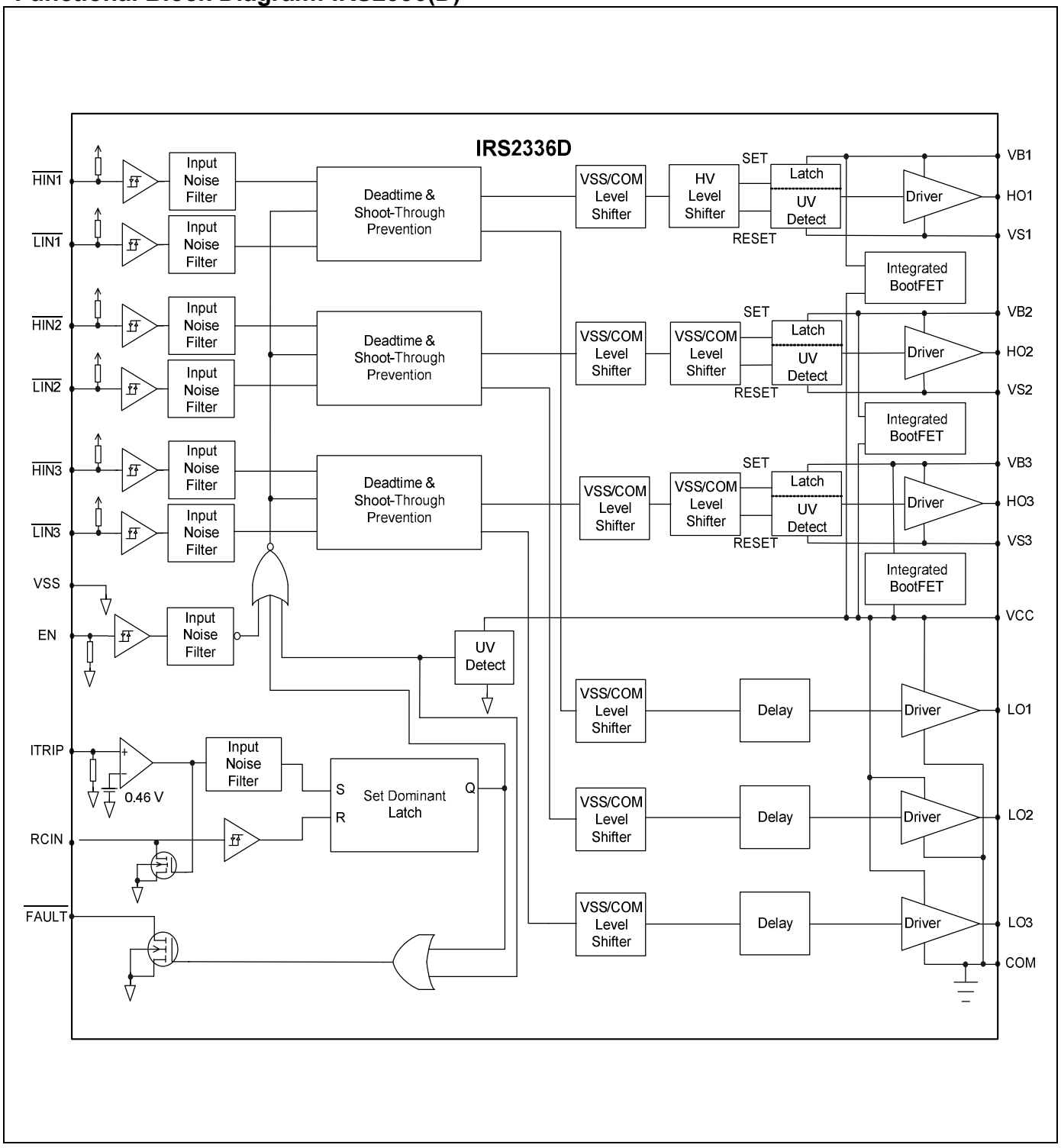
† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.

†† This parameter applies to all of the channels. Please see the application section for more details.

††† PM is defined as PW_{IN} - PW_{OUT}.

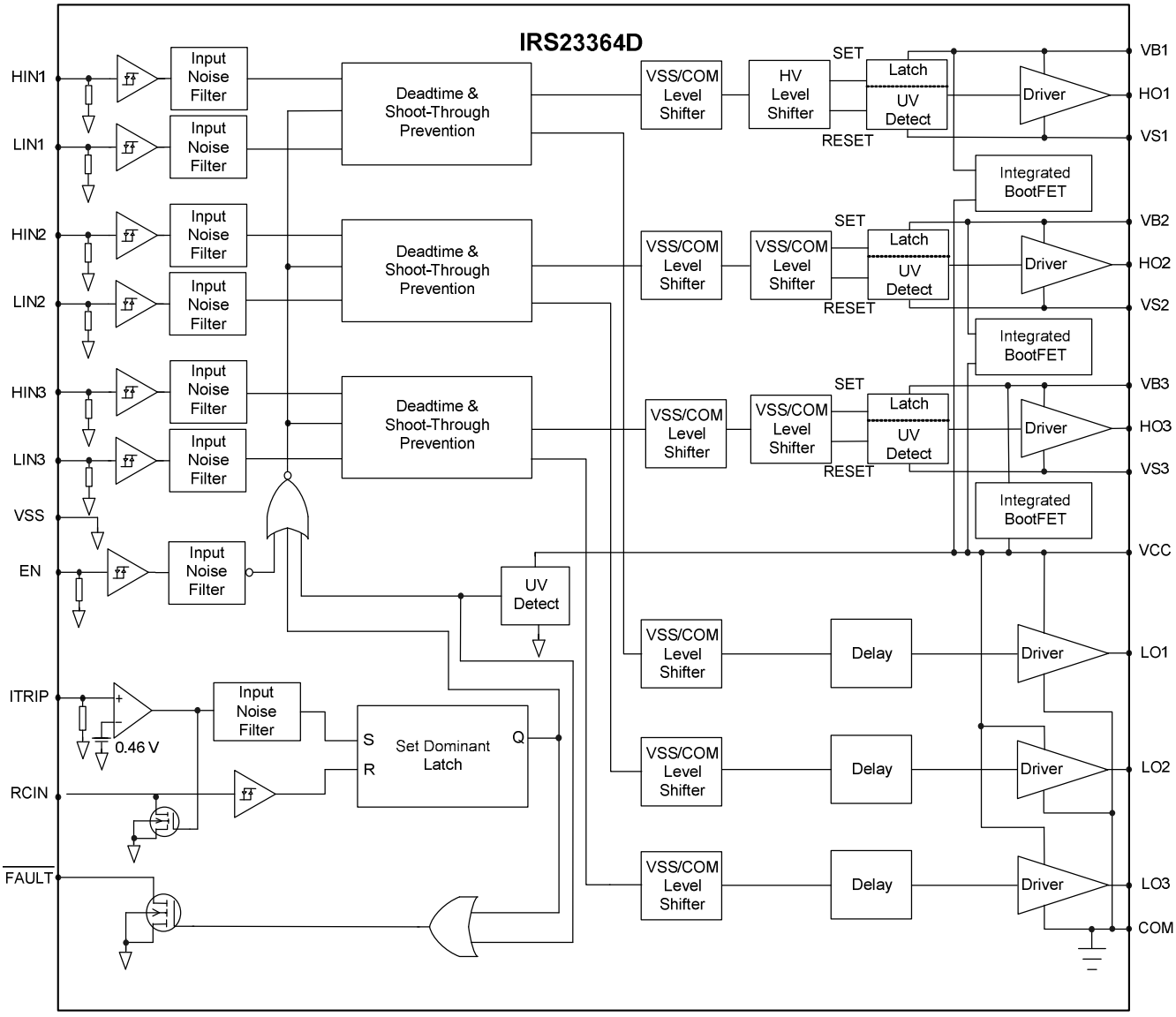


Functional Block Diagram: IRS2336(D)

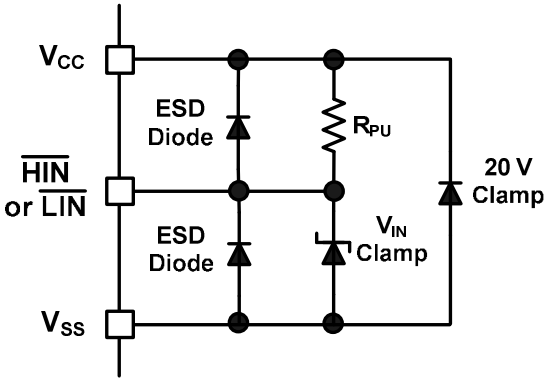


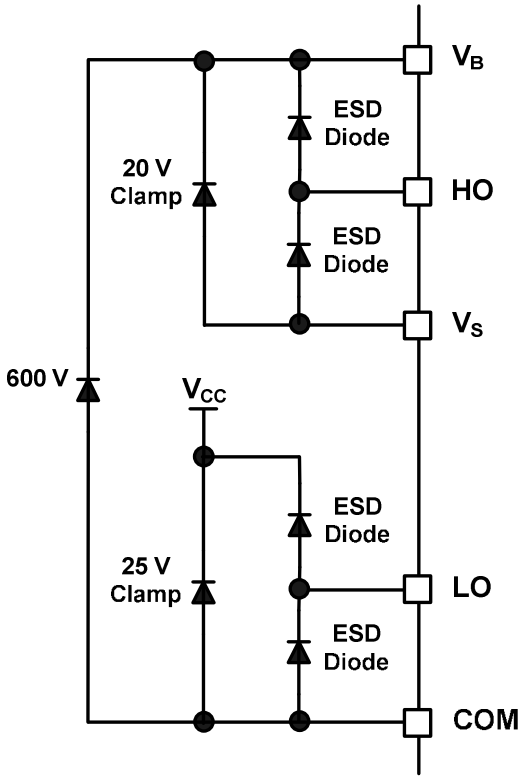
Note: IRS2336 is without the "Integrated BootFET"

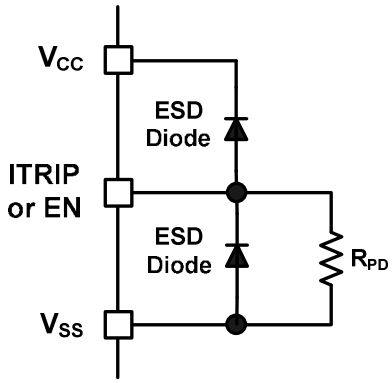
Functional Block Diagram: IRS23364D

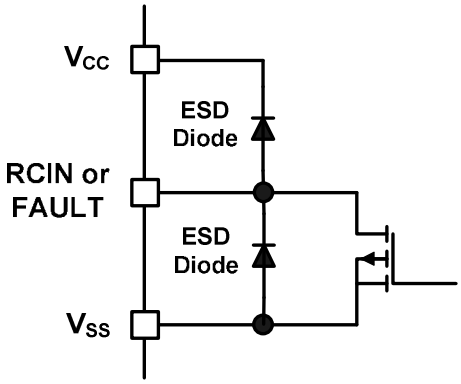


Input/Output Pin Equivalent Circuit Diagrams: IRS2336(D)

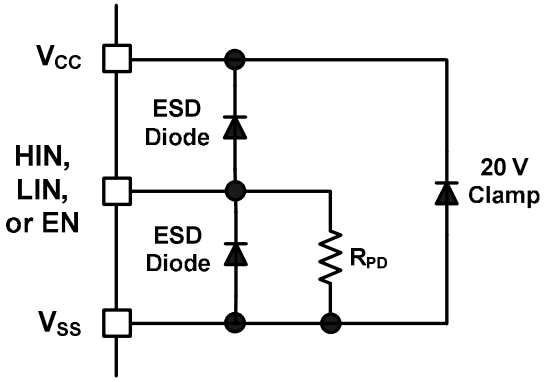


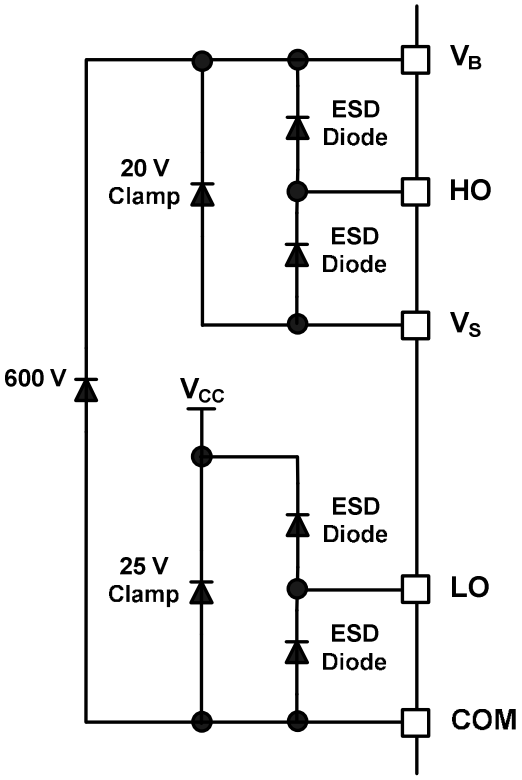


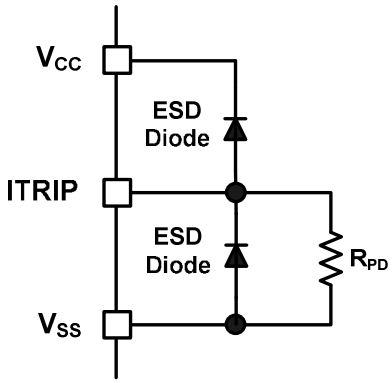


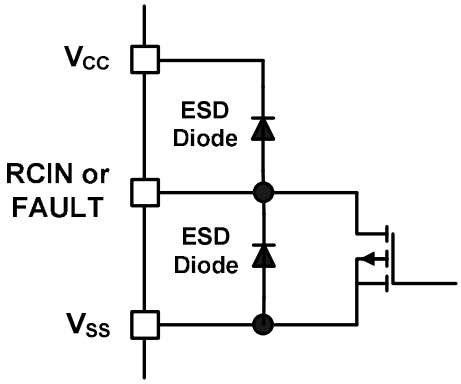


Input/Output Pin Equivalent Circuit Diagrams: IRS23364D









Lead Definitions: IRS2336(D)

Symbol	Description
VCC	Low-side supply voltage
VSS	Logic ground
VB1	High-side gate drive floating supply (phase 1)
VB2	High-side gate drive floating supply (phase 2)
VB3	High-side gate drive floating supply (phase 3)
VS1	High voltage floating supply return (phase 1)
VS2	High voltage floating supply return (phase 2)
VS3	High voltage floating supply return (phase 3)
HIN1/N	Logic inputs for high-side gate driver outputs (phase 1); input is out-of-phase with output
HIN2/N	Logic inputs for high-side gate driver outputs (phase 2); input is out-of-phase with output
HIN3/N	Logic inputs for high-side gate driver outputs (phase 3); input is out-of-phase with output
LIN1/N	Logic inputs for low-side gate driver outputs (phase 1); input is out-of-phase with output
LIN2/N	Logic inputs for low-side gate driver outputs (phase 2); input is out-of-phase with output
LIN3/N	Logic inputs for low-side gate driver outputs (phase 3); input is out-of-phase with output
HO1	High-side driver outputs (phase 1)
HO2	High-side driver outputs (phase 2)
HO3	High-side driver outputs (phase 3)
LO1	Low-side driver outputs (phase 1)
LO2	Low-side driver outputs (phase 2)
LO3	Low-side driver outputs (phase 3)
COM	Low-side gate drive return
FAULT/N	Indicates over-current, over-temperature (ITRIP), or low-side undervoltage lockout has occurred. This pin has negative logic and an open-drain output. The use of over-current and over-temperature protection requires the use of external components.
EN	Logic input to shutdown functionality. Logic functions when EN is high (i.e., positive logic). No effect on FAULT and not latched.
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into an open-drain high-impedance state.

Lead Definitions: IRS23364D

Symbol	Description
VCC	Low-side supply voltage
VSS	Logic ground
VB1	High-side gate drive floating supply (phase 1)
VB2	High-side gate drive floating supply (phase 2)
VB3	High-side gate drive floating supply (phase 3)
VS1	High voltage floating supply return (phase 1)
VS2	High voltage floating supply return (phase 2)
VS3	High voltage floating supply return (phase 3)
HIN1	Logic inputs for high-side gate driver outputs (phase 1); input is in-phase with output
HIN2	Logic inputs for high-side gate driver outputs (phase 2); input is in-phase with output
HIN3	Logic inputs for high-side gate driver outputs (phase 3); input is in-phase with output
LIN1	Logic inputs for low-side gate driver outputs (phase 1); input is in-phase with output
LIN2	Logic inputs for low-side gate driver outputs (phase 2); input is in-phase with output
LIN3	Logic inputs for low-side gate driver outputs (phase 3); input is in-phase with output
HO1	High-side driver outputs (phase 1)
HO2	High-side driver outputs (phase 2)
HO3	High-side driver outputs (phase 3)
LO1	Low-side driver outputs (phase 1)
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FAULT/N	Indicates over-current, over-temperature (ITRIP), or low-side undervoltage lockout has occurred. This pin has negative logic and an open-drain output. The use of over-current and over-temperature protection requires the use of external components.
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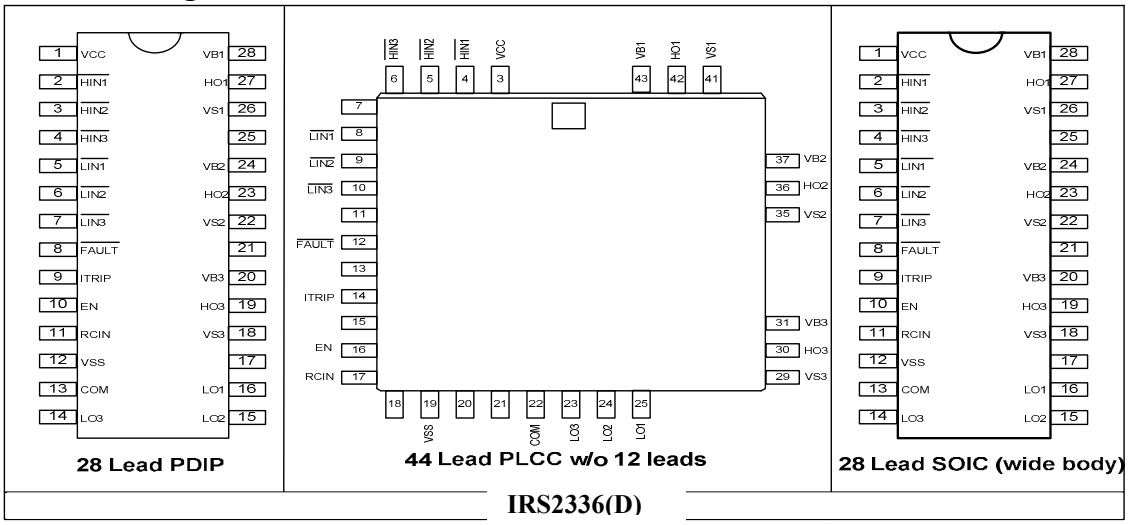
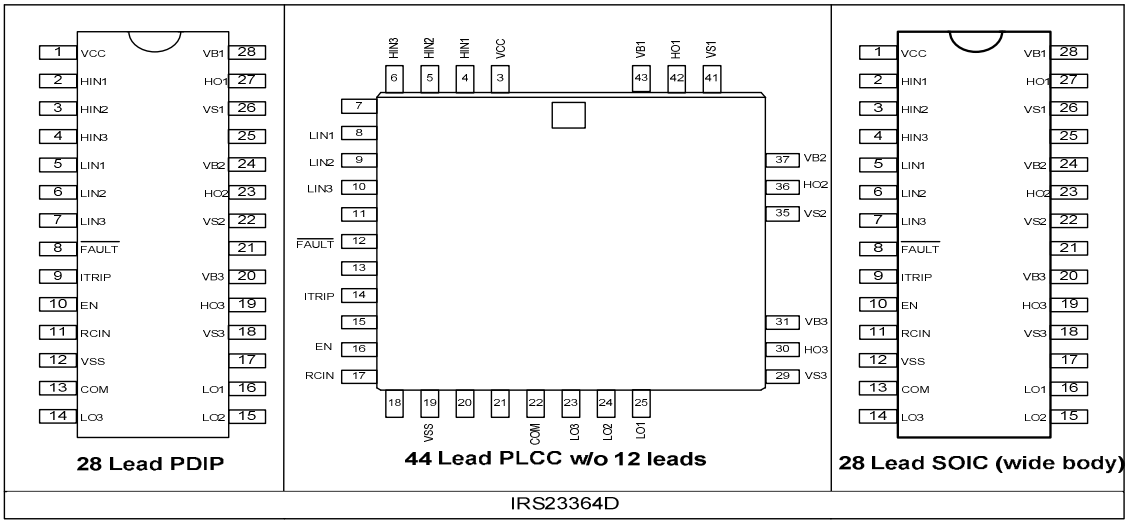
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into an open-drain high-impedance state.

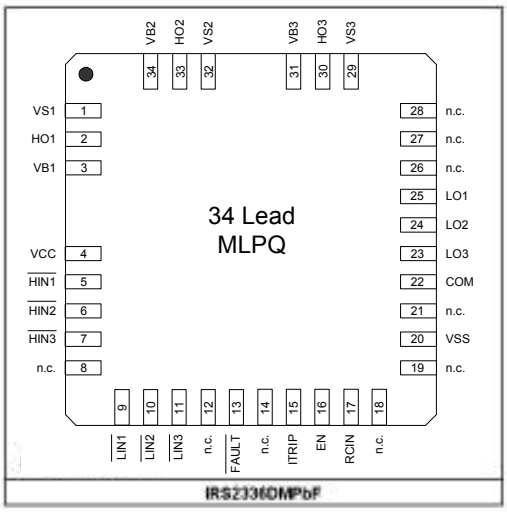
Lead Assignments



IRS2336(D)



IRS23364D



Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Over-Temperature Shutdown Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Tolerant to Negative V_S Transients
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS2336xD HVICs are designed to drive up to six MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

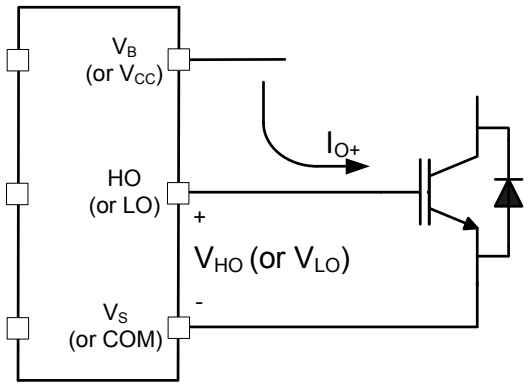


Figure 1: HVIC sourcing current

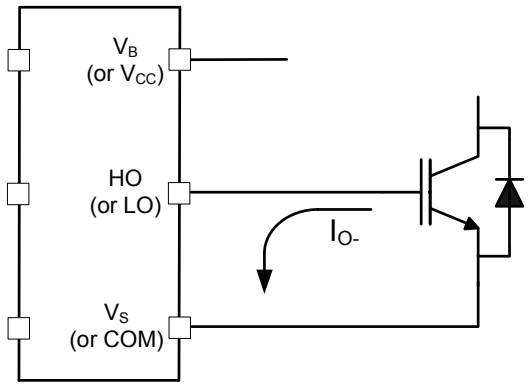


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS2336(D) and IRS23364D are illustrated below in Figures 3 and 4. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

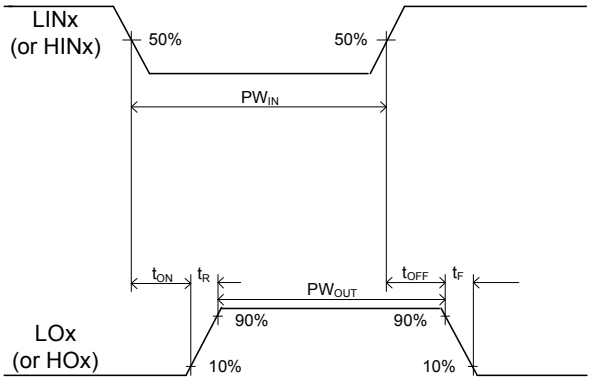


Figure 3: Switching time waveforms (IRS2336(D))

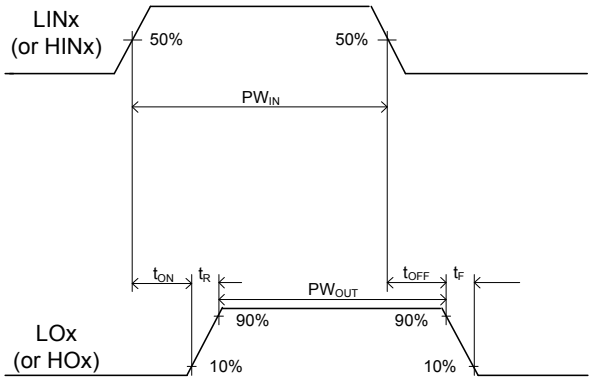


Figure 4: Switching time waveforms (IRS23364D)

The following two figures illustrate the timing relationships of some of the functionality of the IRS2336xD; this functionality is described in further detail later in this document.

During interval A of Figure 5, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 5 and 6 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to $V_{RCIN,TH}$ (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 5, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx) being held in the low state until the enable pin is pulled high.

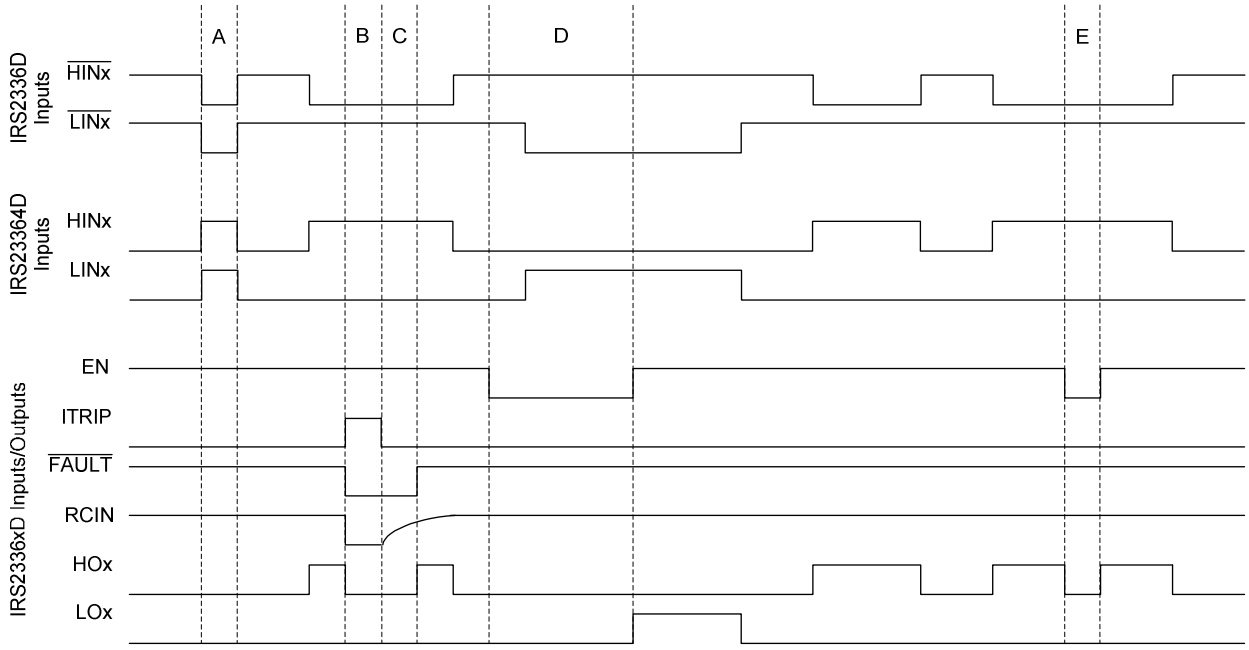


Figure 5: Input/output timing diagram for the IRS2336xD family

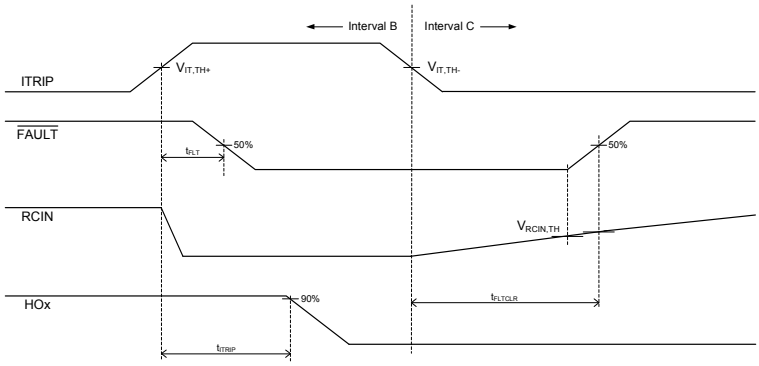


Figure 6: Detailed view of B & C intervals

Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 7 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS2336xD is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched. Figure 7 defines the two deadtime parameters (i.e., DT_1 and DT_2) of a specific channel; the deadtime matching parameter (MDT) associated with the IRS2336xD specifies the maximum difference between DT_1 and DT_2. The MDT parameter also applies when comparing the DT of one channel of the IRS2336xD to that of another.

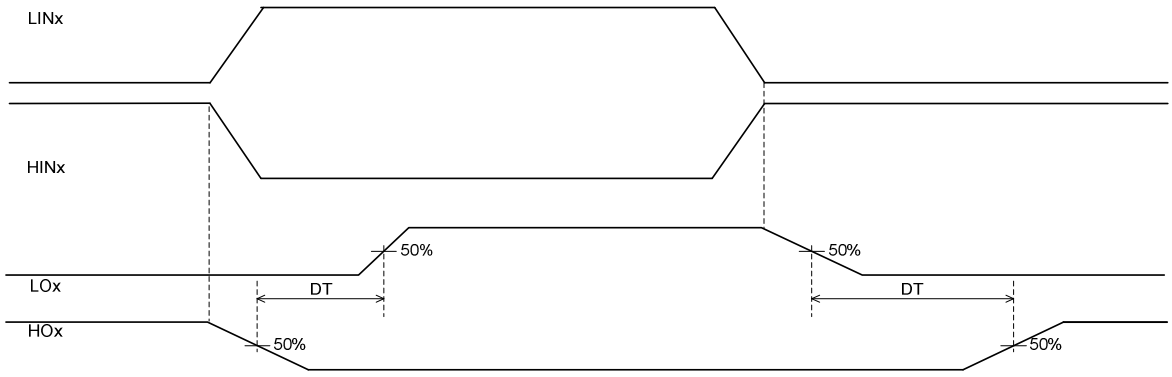


Figure 7: Illustration of deadtime

Matched Propagation Delays

The IRS2336xD family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other; the MT specification applies as well. The propagation turn-on delay (t_{ON}) of the IRS2336xD is matched to the propagation turn-on delay (t_{OFF}).

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS2336xD family has been designed to be compatible with 3.3 V and 5 V logic-level signals. The IRS2336(D) features an integrated 5.2 V Zener clamp on the HIN, LIN, ITRIP, and EN pins; the IRS23364D does not offer this input clamp. Figure 8 illustrates an input signal to the IRS2336(D) and IRS23364D, its input threshold values, and the logic state of the IC as a result of the input signal.

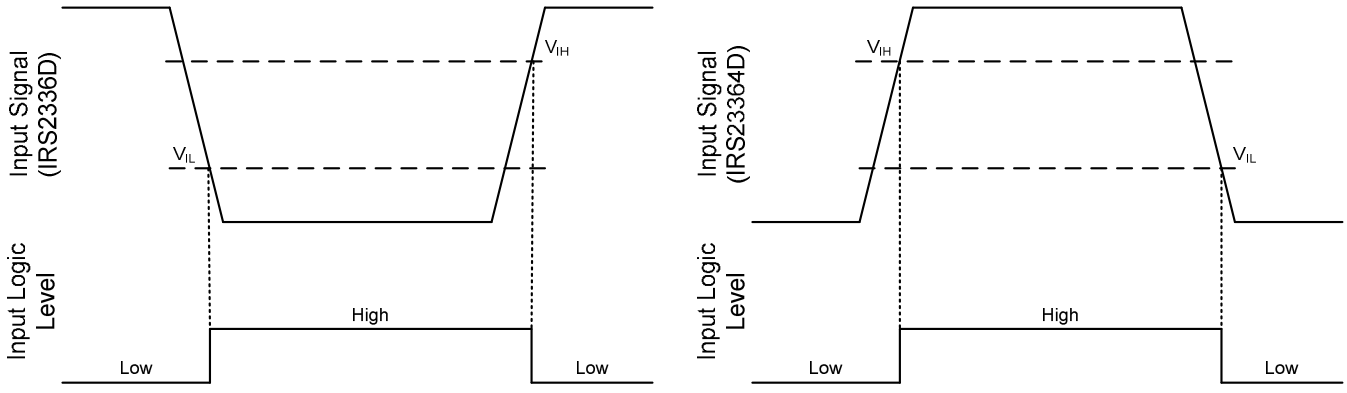


Figure 8: HIN & LIN input thresholds

Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 9 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

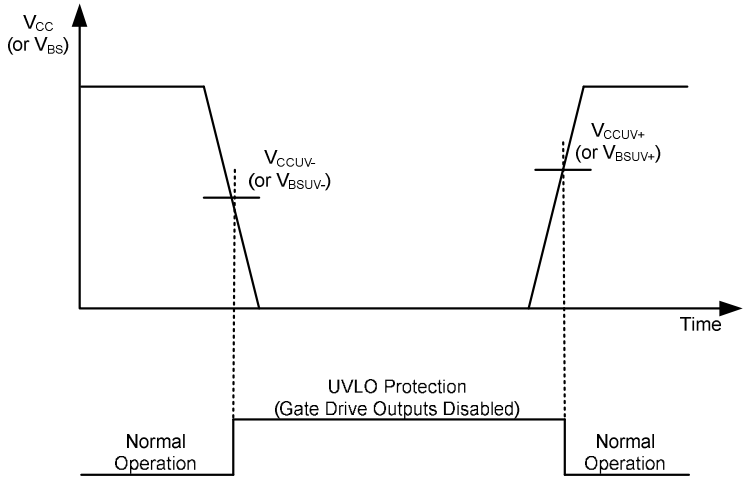


Figure 9: UVLO protection

Shoot-Through Protection

The IRS2336xD family of high-voltage ICs is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table. Note that the IRS2336(D) has inverting inputs (the output is out-of-phase with its respective input) while the IRS23364D has non-inverting inputs (the output is in-phase with its respective input).

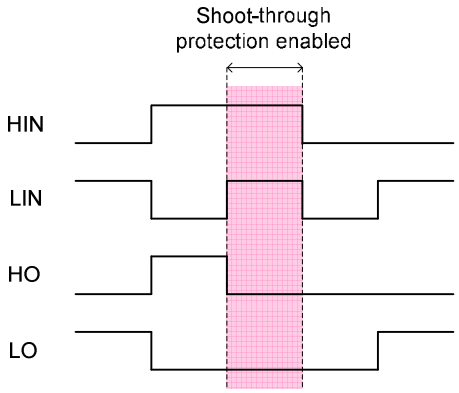


Figure 10: Illustration of shoot-through protection circuitry

IRS2336(D)					IRS23364D			
HIN	**LIN**	**HO**	**LO**		**HIN**	**LIN**	**HO**	**LO**
0	0	0	0		0	0	0	0
0	1	1	0		0	1	0	1
1	0	0	1		1	0	1	0
1	1	0	0		1	1	0	0

Table 1: Input/output truth table for IRS2336D and IRS23364D

Enable Input

The IRS2336xD family of HVICs is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state. The enable circuitry of the IRS2336xD features an input filter; the minimum input duration is specified by $t_{FILTER,EN}$. Please refer to the EN pin parameters $V_{EN,TH+}$, $V_{EN,TH-}$, and I_{EN} for the details of its use. Table 2 gives a summary of this pin's functionality and Figure 11 illustrates the outputs' response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table
(*assumes no other fault condition)

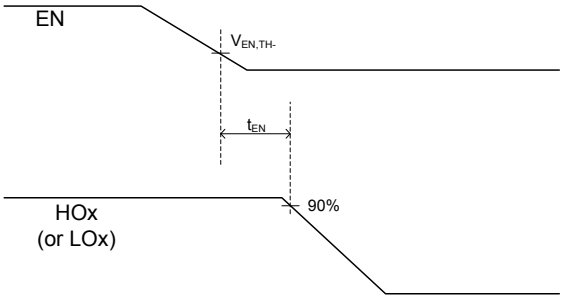


Figure 11: Output enable timing waveform

Fault Reporting and Programmable Fault Clear Timer

The IRS2336xD family provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the FAULT pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 12 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 13 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

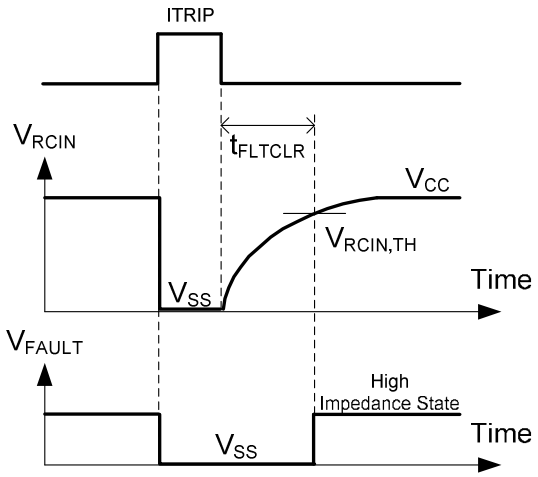


Figure 12: RCIN and FAULT pin waveforms

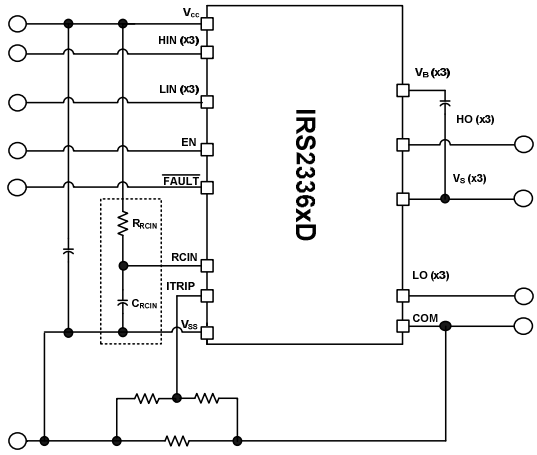


Figure 13: Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RCIN}	≤1 nF
	Ceramic
R_{RCIN}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RCIN}C_{RCIN})\ln(1-V_{RCIN,TH}/V_{CC})$$

Over-Current Protection

The IRS2336xD HVICs are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to V_{SS}.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 14, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{IT,TH+}$) at that current level.

$$V_{IT,TH+} = R_0 I_{DC-}(R_1/(R_1+R_2))$$

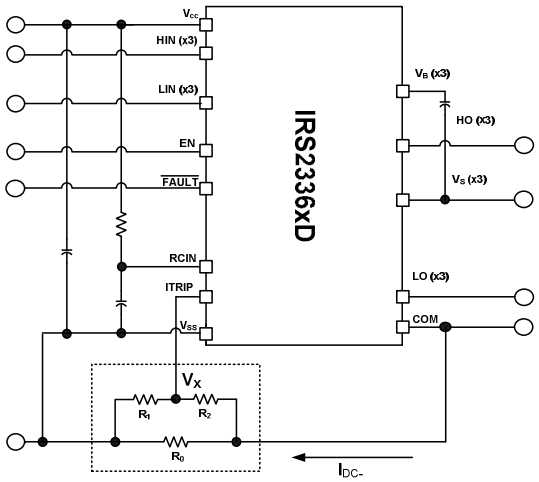


Figure 14: Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

Over-Temperature Shutdown Protection

The ITRIP input of the IRS2336xD can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 15 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors R_3 and R_4. As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node V_X. The resistor values should be selected such the voltage V_X should reach the threshold voltage ($V_{IT,TH+}$) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.

When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 16; the OR-ing diodes have been labeled D_1 and D_2.