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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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September 8, 2010
Datasheet No – PD97524

International
IOR Rectifier

IRS254(01,11)

LED BUCK REGULATOR CONTROL IC

Features

- 200 V (IRS25401) and 600 V (IRS25411) half bridge driver
- Micropower startup (<500 μA)
- ±2% voltage reference
- 140 ns deadtime
- 15.6 V zener clamp on V_{CC}
- Frequency up to 500 kHz
- Auto restart, non-latched shutdown
- PWM dimmable
- Small 8-Lead DIP/8-Lead SOIC packages

Typical Applications

LED drivers for lamp replacement
LED driver back end current regulator

Product Summary

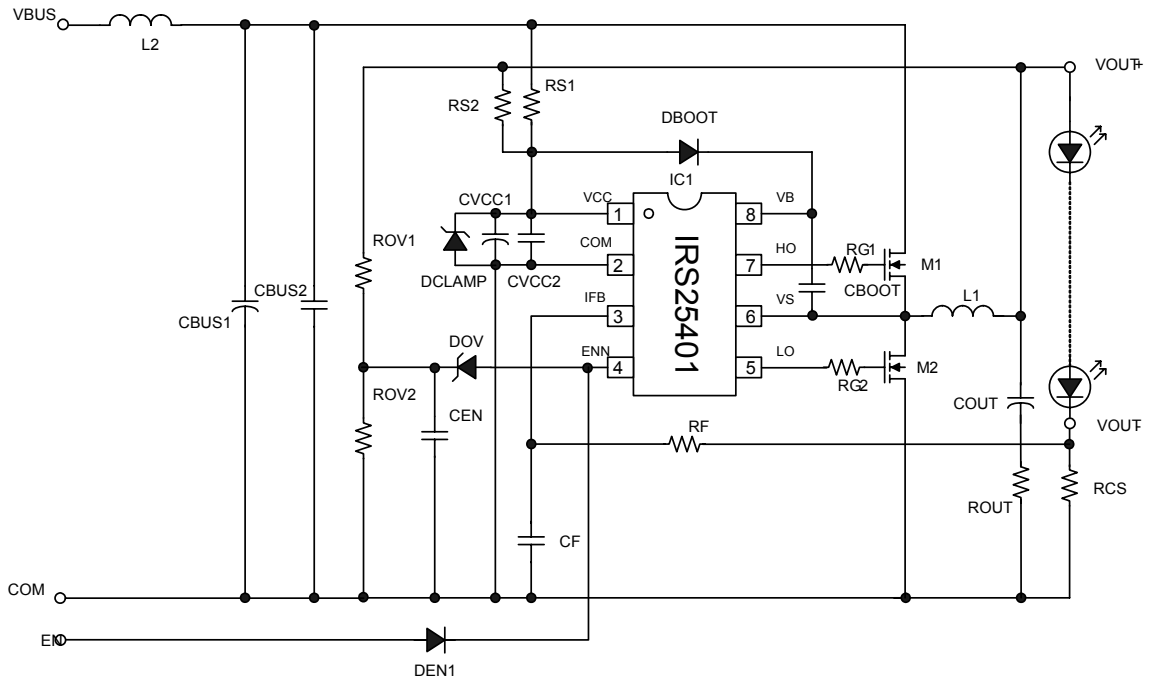
Topology	Buck
V_{OFFSET}	200V,600V
V_{OUT}	VCC
I_{o+} & I_{o-} (typical)	0.5A/0.7A
t_{ON} & t_{OFF} (typical)	50/30nS
Deadtime (typical)	140nS

Packages

8-Lead PDIP
IRS254(01,11)PbF

8-LeadSOIC
IRS254(01,11)SPbF

Typical Connection Diagram

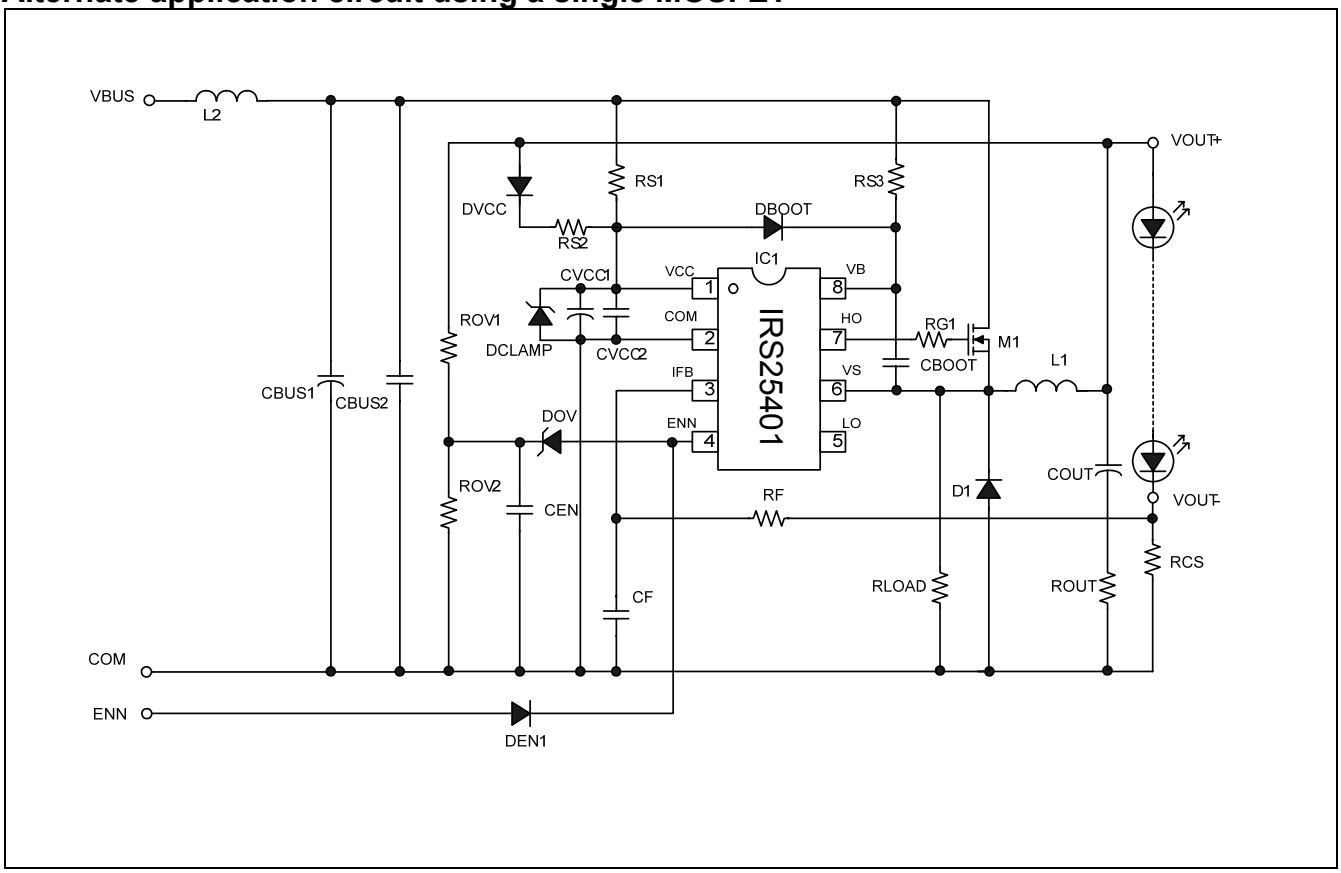


Description

The IRS254(01,11) are high voltage, high frequency buck control ICs for constant LED current regulation. They incorporate a continuous mode time-delayed hysteretic buck regulator to directly control the average load current, using an accurate on-chip bandgap voltage reference. These parts directly replace the IRS2540 and IRS2541 with improved latch up immunity.

The application is inherently protected against short circuit conditions, with the ability to easily add open-circuit protection. An external high-side bootstrap circuit drives the buck switching element at high frequencies. A low-side driver is also provided for synchronous rectifier designs. All functions are realized within a simple 8 pin DIP or SOIC package.

Alternate application circuit using a single MOSFET



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
		PDIP8	Not applicable (non-surface mount package style))
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 1C (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
V_B	High-side floating well supply voltage	IRS25401	-0.3	225	V
		IRS25411	-0.3	625	
V_S	High-side floating well supply return voltage		V_B + 0.3	V_B + 0.3	
V_{HO}	Floating gate drive output voltage		V_S – 0.3	V_B + 0.3	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IFB}	Feedback voltage		-0.3	V_{CC} + 0.3	
V_{ENN}	Enable voltage		-0.3	V_{CC} + 0.3	
I_{CC}	Supply current (†)		-20	20	mA
dV/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq$+25 ºC $P_D = (T_{JMAX}-T_A)/R_{THJA}$	(8-Pin DIP)	---	1	W
		(8-Pin SOIC)	---	0.625	
$R_{\Theta JA}$	Thermal resistance, junction to ambient	(8-Pin DIP)	---	125	ºC/W
		(8-Pin SOIC)	---	200	
T_J	Junction temperature		-55	150	ºC
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

† : This IC contains a zener clamp structure between the chip V_{CC} and COM, with a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a low impedance DC power source greater than V_{CLAMP} specified in the electrical characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within recommended conditions.

Symbol	Definition		Min	Max	Units
V_{BS}	High-side floating supply voltage		V_{CC} -0.7	$V_{CLAMPHS}$	
V_S	Steady state high-side floating supply offset voltage	IRS25401	-1	200	V
		IRS25411	-1	600	
V_{CC}	Supply voltage		V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current		-Note 2	10	
T_J	Junction temperature		-25	125	

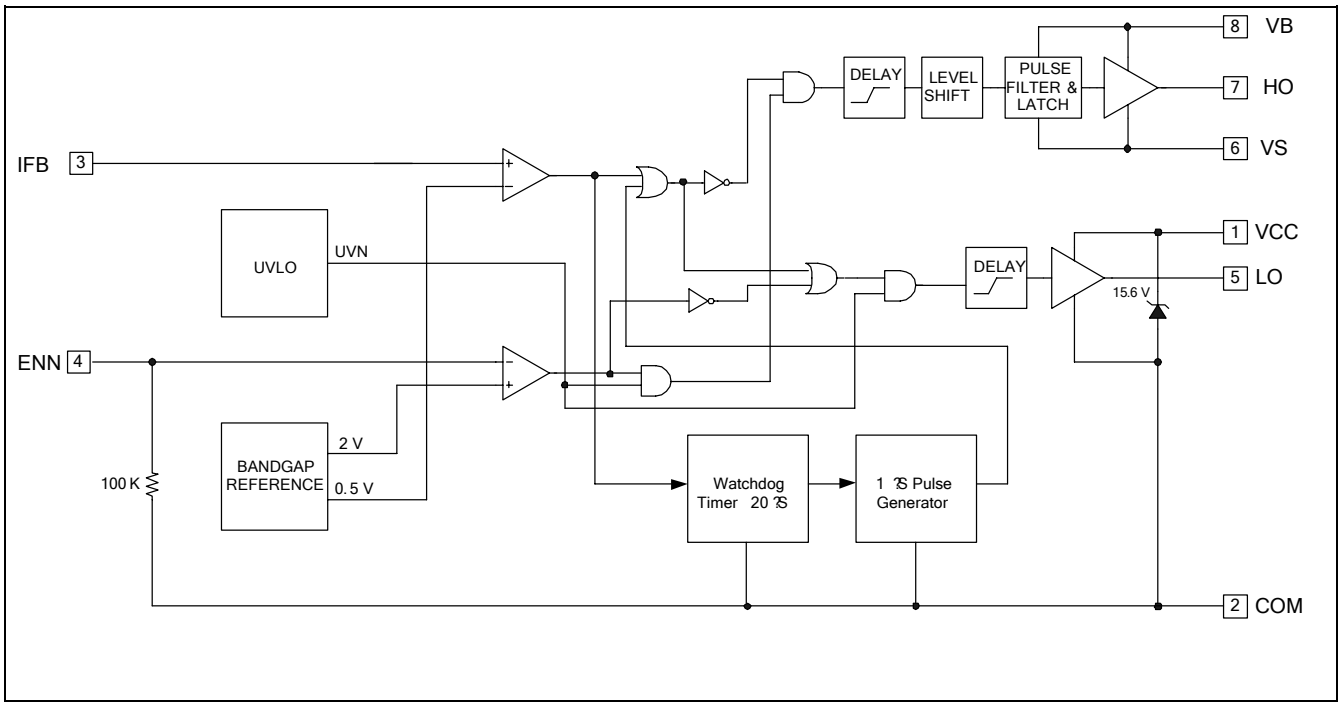
†† : Sufficient current should be supplied to V_{CC} to keep the internal 15.6 V zener regulating at V_{CLAMP}.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14 V +/- 0.25 V, C_{LO}=C_{HO}=1000 pF, C_{VCC}=C_{VBS}=0.1 µF, T_A=25 °C unless otherwise specified.

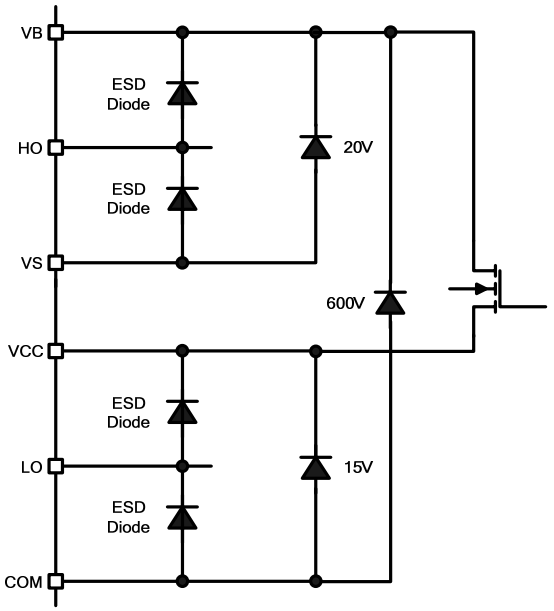
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	9.0	10.0	V	V_{CC} rising from 0 V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	6.5	7.5	8.5		V_{CC} falling from 14 V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	1.0	1.2	2.0		
I_{QCCUV}	UVLO mode quiescent current	---	50	150	µA	V_{CC}=6 V
I_{QCCENN}	Diesabled mode quiescent current	---	1.0	2.0	mA	EN>V_{ENTH+}
I_{QCC}	Quiescent V_{CC} supply current	---	1.0	2.0		I_{FB} = 1 V
I_{CC50k}	V_{CC} supply current, f = 50 kHz	---	2.0	3.0		Duty Cycle = 50% f = 50 kHz
V_{CLAMP}	V_{CC} zener clamp voltage	14.6	15.6	16.6	V	I_{CC} = 10 mA
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} supply current	---	0.05	1.0	mA	V_{HO} = V_S
I_{QBS1}	Quiescent V_{BS} supply current	---	1.0	2.0		I_{FB} = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	6.5	7.5	8.5	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.0	7.0	8.0		
I_{LK}	Offset supply leakage current	---	1	50	µA	IRS25401:V_B=V_S=200 V IRS25411:V_B=V_S=600 V
$V_{CLAMPHS}$	V_{BS} high side zener clamp voltage	24.4	26.0	27.6	V	I_{CC} = 10 mA
Current Control Operation						
V_{ENNTH+}	ENN pin positive threshold	2.5	2.7	3.0	V	
V_{ENNTH-}	ENN pin negative threshold	1.7	2.0	2.3		
$V_{0.5}$	0.5 V voltage reference (die level test)	490	500	510	mV	
V_{IFBTH}	IFB pin threshold	455	500	540		
f	Maximum frequency	---	500	---	kHz	
Gate Driver Output Characteristics						
V_{OL}	Low level output voltage (HO or LO)	---	COM	---	V	
V_{OH}	High level output voltage (HO or LO)	---	V_{CC}	---		
t_r	Turn-on rise time	---	50	120	ns	
t_f	Turn-off fall time	---	30	50		
$I_{O+/-}$	Output source/sink short circuit pulsed current	---	0.5/0.7	---	A	
DT	Deadtime	---	140	---	ns	I_{FB} = 50 kHz square wave, 200 mV pk-pk DC offset = 400 mV Duty Cycle = 50%
$t_{LO,ON}$	Delay between V_{IFB}>V_{IFBTH} and LO turn-on	---	320	---		
$t_{LO,OFF}$	Delay between V_{IFB}<V_{IFBTH} and LO turn-off	---	180	---		
$t_{HO,ON}$	Delay between V_{IFB}<V_{IFBTH} and HO turn-on	---	320	---		
$t_{HO,OFF}$	Delay between V_{IFB}>V_{IFBTH} and HO turn-off	---	180	---		
Watchdog timer						
t_{WD}	Watchdog timer period	---	20	---	µs	I_{FB} =1 V
P_{WWD}	LO pulse width	---	1.0	---		

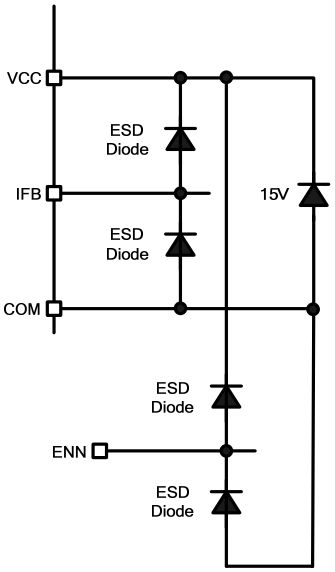
Functional Block Diagram



Values in block diagram are typical values

Input/Output Pin Equivalent Circuit Diagrams: IRS25401/IRS25411

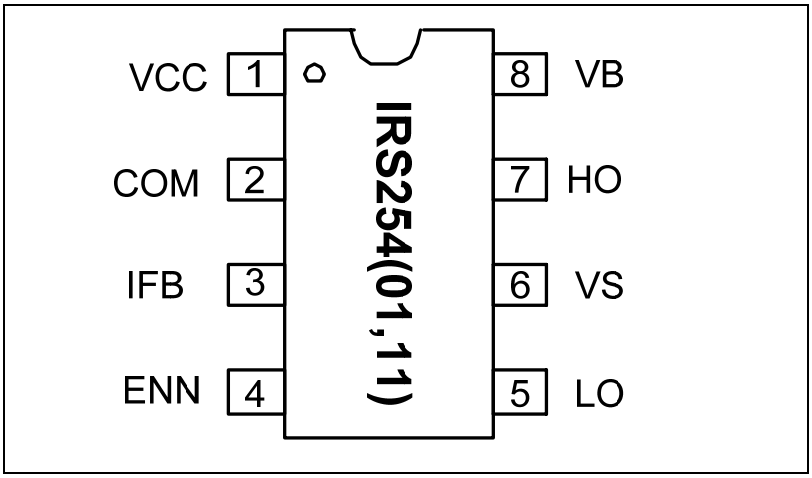




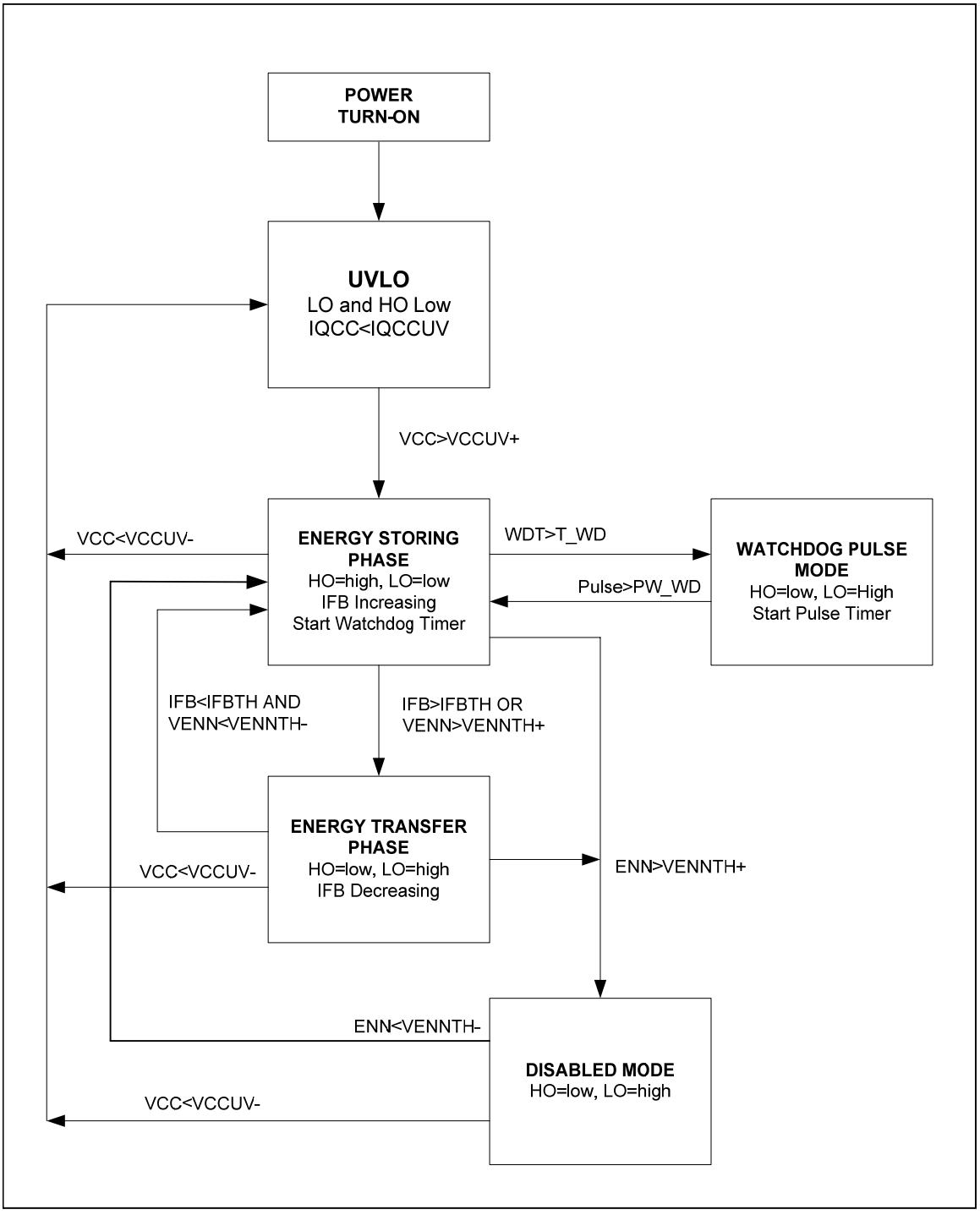
Lead Definitions

PIN #	Symbol	Description
1	VCC	Supply voltage
2	COM	IC power & signal ground
3	IFB	Current feedback
4	ENN	Disable outputs (LO=High, HO=Low)
5	LO	Low–side gate driver output
6	VS	High–side floating return
7	HO	High–side gate driver output
8	VB	High–side gate driver floating supply

Lead Assignments



State Diagram



Application Information and Additional Details

Operating Mode

The IRS254(01,11) operates as a time-delayed hysteritic buck controller. During normal operating conditions the output current is regulated via the IFB pin voltage (nominal value of 500 mV). This feedback is compared to an internal high precision bandgap voltage reference. An on-board dV/dt filter has also been used to ignore erroneous transitioning.

Once the supply to the IC reaches V_{CCUV+}, the LO output is held high and the HO output low for a predetermined period of time. This initiates charging of the bootstrap capacitor, establishing the V_{BS} floating supply for the high-side output. The IC then begins toggling HO and LO outputs as needed to regulate the current.

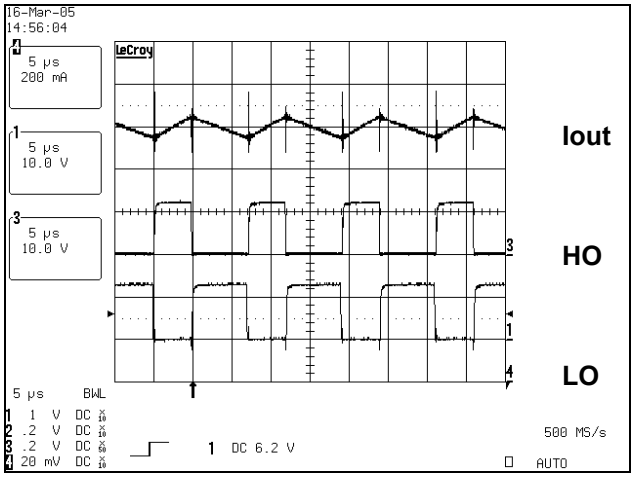


Fig.1 IRS254(01,11) Control Signals, Iavg=1.2 A

As long as V_{IFB} is below V_{IFBTH}, HO is on, modulated by the watchdog timer described below, which maintains charge for the floating high side on the bootstrap capacitor. The load is receiving current from V_{BUS}, which simultaneously stores energy in the inductor, as V_{IFB} increases, unless the load is open circuit. Once V_{IFB} crosses V_{IFBTH}, the control loop switches HO off after the delay $t_{HO,OFF}$. When HO switches off, LO will turn on after the deadtime (DT), the inductor then releases its stored energy into the load and V_{IFB} starts decreasing. When V_{IFB} drops below V_{IFBTH} again, the control loop switches HO on after the delay $t_{HO,ON}$ and LO off after the delay $t_{HO,ON}$ + DT. The switching continues to regulate the current at an average value determined as follows. When the inductance value is large enough to maintain a low ripple on I_{FB}, $I_{out,avg}$ can be calculated:

$$Iout(avg) = VIFBTH / RCS$$

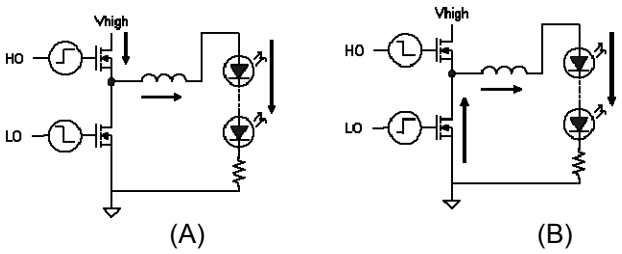


Fig.2 (A) Storing Energy in Inductor
(B) Releasing Inductor Stored Energy

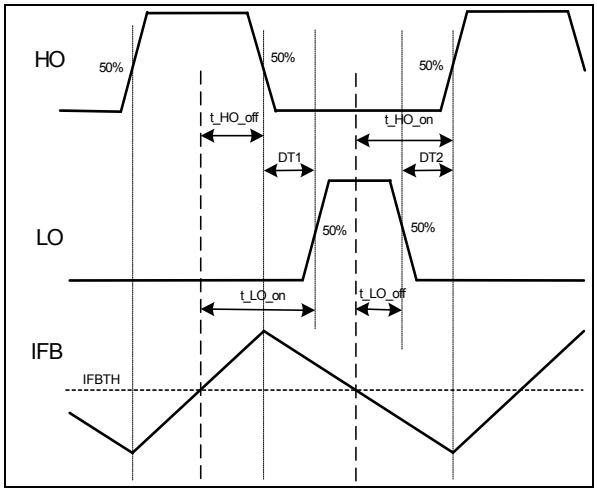


Fig.3 IRS254(0,1) Time Delayed Hysterisis

The control method is hysteretic with a free running frequency, which enables average current regulation in constrast to a fixed frequency scheme providing peak current regulation only. This reduces the part count since there is no need for frequency setting components and also provides an inherently stable system, which acts as a dynamic current source.

A deadtime of approximately 140 ns between the two gate drive signals is incoporated to prevent shoot-through. The deadtime has been adjusted to maintain precise current regulation, while still preventing shoot-through.

Watchdog Timer

During an open circuit condition, without the watchdog timer, the HO output would remain high at all times and the charge stored in the bootstrap capacitor C_{BOOT} would gradually discharge the floating power supply for the high-side driver, which would then be unable to fully switch on the upper MOSFET causing high losses. To maintain sufficient charge on the bootstrap capacitor, a watchdog timer has been implemented. In the condition where V_{IFB} remains below V_{IFBTH}, the HO output is driven low after 20 µs and the LO output forced high. This toggling of the outputs will last for approximately 1 µs to maintain and replenish sufficient charge on C_{BOOT}.

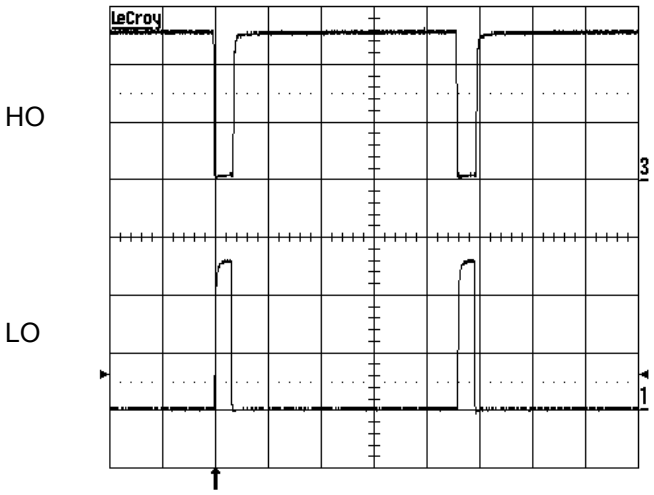


Fig.4 Illustration of Watchdog Timer

Bootstrap Capacitor and Diode

The bootstrap capacitor value needs to be selected so that it maintains sufficient charge for at least the approximately 20 µs interval until the watchdog timer allows the capacitor to recharge. If the capacitor value is too small, it will discharge in less than 20 µs. The typical bootstrap capacitor is approximately 100 nF.

The bootstrap diode must be a fast recovery or ultrafast recovery component to maintain good efficiency. Since the cathode of the bootstrap diode will be switching between zero and to the high voltage bus, the reverse recovery time of this diode is critical. For additional information concerning the bootstrap components, refer to the Design Tip (DT 98-2), *"Bootstrap Component Selection For Control ICs"* at www.irf.com under Design Support

Disable (ENN) Pin

The disable pin can be used for PWM dimming and open-circuit protection. When the ENN pin is held low, the chip remains in a fully functional state with no alterations to the operating environment. To disable the control feedback and regulation, a voltage greater than V_{ENTH} (approximately 2.5 V) needs to be applied to the ENN pin. With the chip in a disabled state, HO output will remain low, whereas the LO output will remain high to prevent V_S from floating, in addition to maintaining charge on the bootstrap capacitor. The threshold for disabling the IRS254(01,11) has been set to 2.5 V to enhance noise immunity. This 2.5 V threshold also provides compatibility for a drive signal from a microcontroller.

Dimming Mode

To achieve dimming, a signal with constant frequency and adjustable duty cycle can be fed into the ENN pin. There is a direct linear relationship between the average load current and duty cycle. If the ratio is 50%, 50% of the maximum set light output will be realized. Likewise if the ratio is 30%, 70% of the maximum set light output will be realized. A sufficiently high frequency of the dimming signal must be chosen to avoid noticeable flashing or "strobe light" effect. A signal above 120Hz up to 5kHz is sufficient.
The ENN pin logic is inverted to provide enable low so that the default state is with the IC running.

The minimum amount of dimming achievable (light output approaches 0%) will be determined by the "on" time of the HO output, when in a fully functional regulating state. To maintain reliable dimming, it is recommended to keep the "off" time of the enable signal at least 10 times that of the HO "on" time. For example, if the application is running at 75 kHz with an input voltage of 100 V and an output voltage of 20 V, the HO "on" time will be approximately 2.7 µs according to standard buck topology theory. This will set the minimum "off" time of the enable signal to 27 µs.

$$Duty\ Cycle = \frac{V_{out}}{V_{in}} * 100 = \frac{20V}{100V} * 100 = 20\%$$

$$HO_{on\ \mathrm{time}} = 20\% * {}^{1}\!/_{75kHz} \approx 2.7\mu s$$

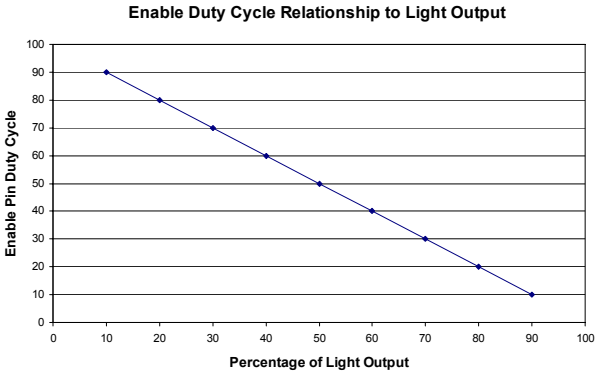


Fig.5 Light Output vs Enable Pin Duty Cycle

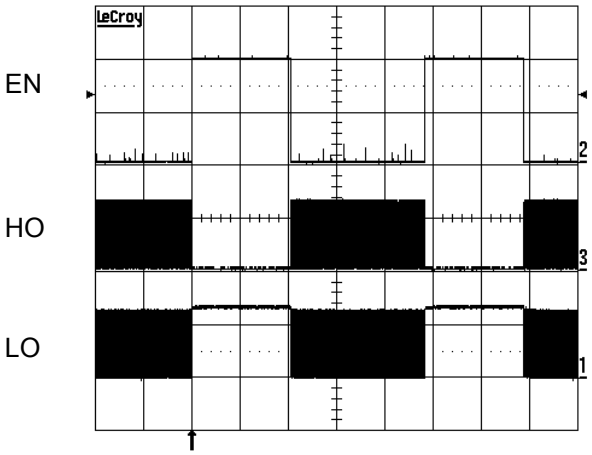


Fig.6 IRS254(01,11) Dimming Signals

Open Circuit Protection Mode

There are several methods of providing over voltage protection at the output if needed. The following very simple method uses a voltage divider, capacitor, and zener diode, the output voltage can be clamped at any desired value. In open-circuit condition without any output clamp, the positive output terminal may reach a high DC voltage. Switching will still occur between the HO and LO outputs, whether due to the output voltage clamp or the watchdog timer. Transients and switching will be observed at the positive output terminal as seen in Fig. 8. The difference in signal shape, between the output voltage and the I_{FB}, is due to the capacitor used to form the voltage clamp. The repetition of the spikes can be reduced by simply increasing the capacitor size.

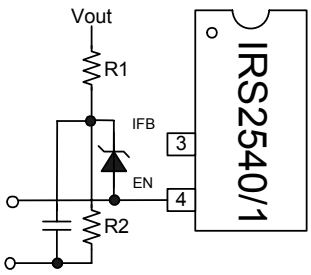


Fig.7 Open Circuit Protection Scheme

The two resistors form a voltage divider for the output, which is then fed into the cathode of the zener diode. The diode will only conduct, flooding the enable pin, when its nominal voltage is exceeded. The chip will enter a disabled state once the divider network produces a voltage at least 2.5 V greater than the zener rating. The capacitor serves only to filter and slow the transients/switching at the positive output terminal. The clamped output voltage can be determined by the following analysis. The choice of capacitor is at the designer's discretion.
This scheme will not be adequate in all applications. An improved method is described in IRPLLED1 Rev D reference design documentation.

$$V_{out} = \frac{(2.5V + DZ)(R_1 + R_2)}{R_2}$$

$$DZ = \text{Zener Diode Nominal Rated Voltage}$$

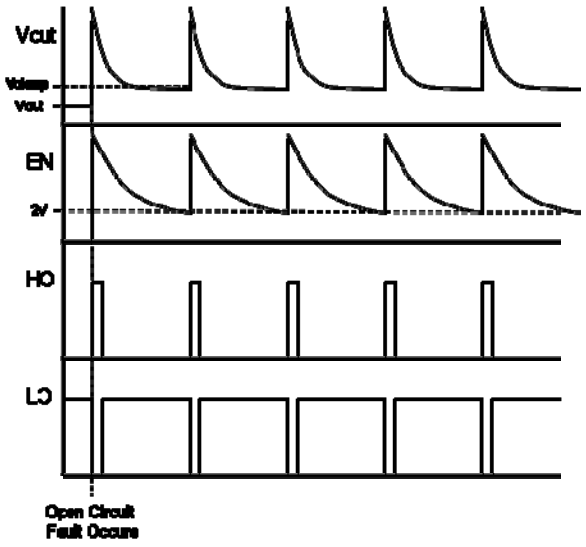


Fig.8 Open Circuit Fault Signals, with Clamp

Under-voltage Lock-out Mode

The under-voltage lock-out mode (UVLO) is defined as the state IRS254(01,11) is in when V_{CC} is below the turn-on threshold of the IC. During startup conditions, if the IC supply remains below V_{CCUV+}, the IRS254(01,11) will enter the UVLO mode. This state is very similar to when the IC has been disabled via control signals, except that LO is also held low. When the supply is increased to V_{CCUV+}, the IC enters

the normal operation mode. If already in normal operation, the IC does not enter UVLO unless the supply voltage falls below V_{CCUV-}.

Inductance Selection

To maintain tight hysteretic current regulation the inductor and output capacitor C_{OUT} (in parallel with the LEDs) need to be large enough to maintain the supply to the load during $t_{HO,ON}$ and avoid significant undershooting of the load current, which in turn causes the average current to fall below the desired value.

First, consider the effect of the inductor when there is no output capacitor to clearly demonstrate the impact of the inductor. In this case, the load current is identical to the inductor current. Fig. 9 shows how the inductor value impacts the frequency over a range of input voltages. As can be seen, the input voltage has a great impact on the frequency and the inductor value has the greatest impact at reducing the frequency for smaller input voltages.

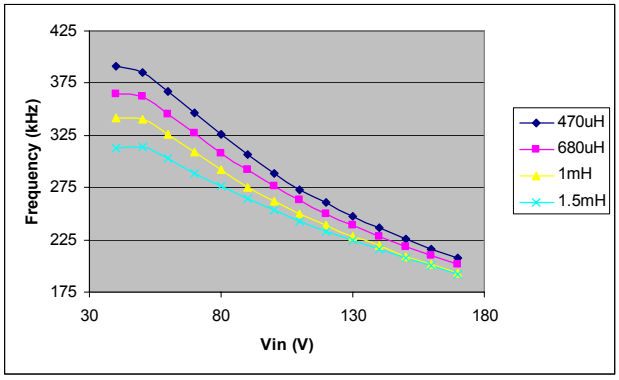


Fig.9 Frequency Response for Chosen Inductances
I_{out} = 350 mA, V_{out} = 16.8 V

Fig. 10 shows how the variation in load current increases over a span of input voltages, as the inductance is decreased. Fig. 11 shows the variation of frequency over different output voltages and different inductance values. Finally Fig. 12 shows how the load current variation increases with lower inductance over a range of output voltages.

The output capacitor can be used simultaneously to achieve the target frequency and current control accuracy. Fig. 11 shows how the capacitance reduces the frequency over a range of input voltage. A small capacitance of 4.7 µF has a large effect on reducing the frequency. Fig. 12 shows how the current regulation is also improved with the output capacitance. There is a point at which continuing to add capacitance no longer has a significant effect on the operating frequency or current regulation, as can be seen in Figs. 13 and 14.

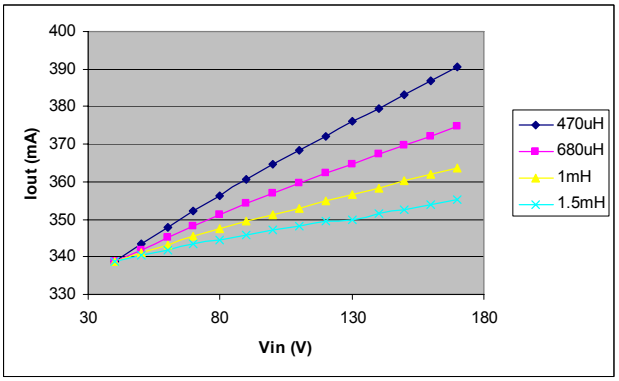


Fig.10 Current Regulation for Chosen Inductances
I_{out} = 350 mA, V_{out} = 16.8 V

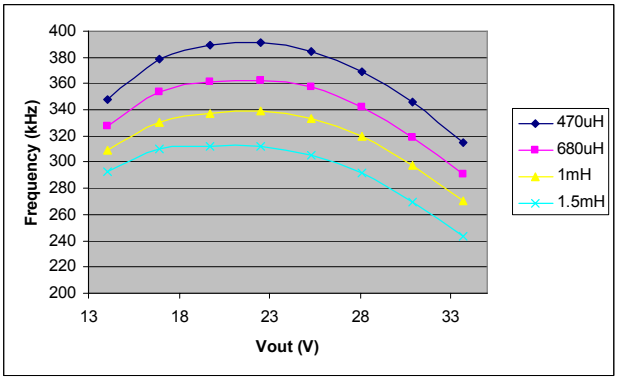


Fig.11 Frequency Response for Chosen Inductances
I_{out} = 350 mA, V_{in} = 50 V

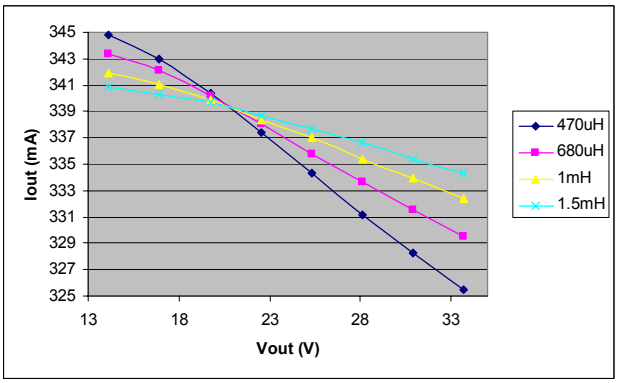


Fig.12 Current Regulation for Chosen Inductances
I_{out} = 350 mA, V_{in} = 50 V

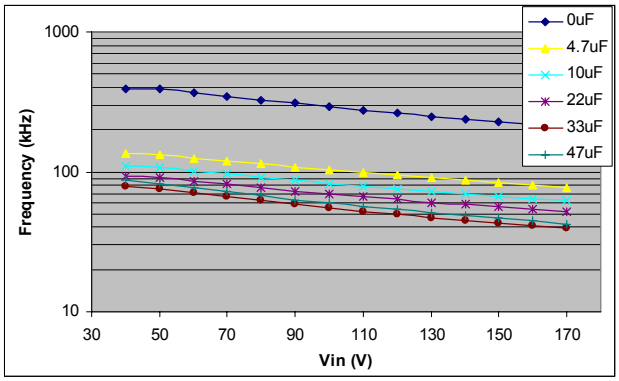


Fig. 13 I_{out} = 350 mA, V_{out} = 16.8 V, L = 470 µH

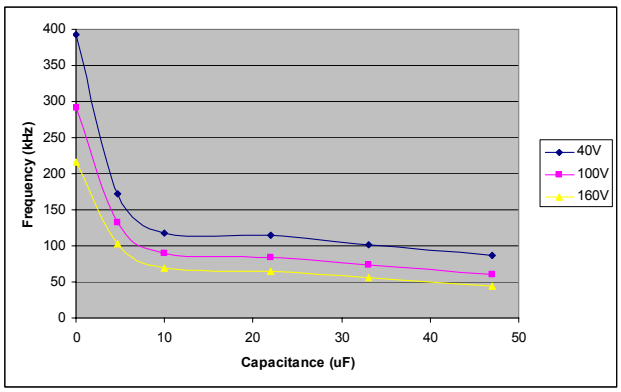


Fig. 14 I_{out} = 350 mA, V_{out} = 16.8 V, L = 470 µH

The addition of the C_{OUT} increases the amount of energy that can be stored in the output stage, which also means it can supply current for an increased period of time. Therefore by slowing down the di/dt transients in the load, the frequency is effectively decreased.

With the C_{OUT} capacitor, the inductor current is no longer identical to that seen in the load. The inductor current will still have a perfectly triangular shape, where as the load will see the same basic trend in the current, but all sharp corners will be rounded with all peaks significantly reduced, as can be seen in Fig. 15

VCC Supply

Since the IRS254(01,11) is rated for 200 V (or 600 V), V_{BUS} can reach values of this magnitude. If a supply resistor to V_{BUS} is used, it can experience high power losses. For higher voltage applications if the output voltage is above VCCUV+ plus one diode drop an alternate V_{CC} supply scheme utilizing the micro-power start-up and a resistor feed-back from the output can to be implemented, as seen in Fig. 16.

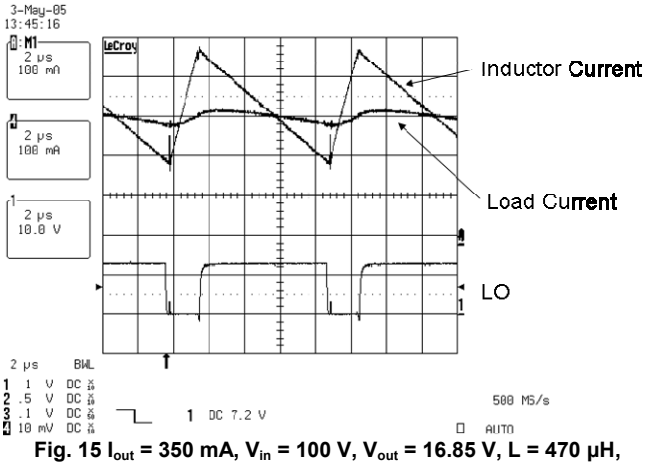


Fig. 15 I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 16.85 V, L = 470 µH, C_{out} = 33 µF

The resistance between V_{BUS} and V_{CC} supply should be large enough to minimize the current sourced directly from the input voltage line; value should be on the order of hundreds of kΩ. Through the supply resistor, a current will flow to charge the V_{CC} capacitor. Once the capacitor is charged up to the V_{CCUV+} threshold, the IRS254(01,11) enters the micro start-up regime and begins to operate, activating the LO and HO outputs. After the first few cycles of switching, the resistor connected between the output and V_{CC} will take over and source all necessary current for the IC. The resistor connecting the output to the supply should be carefully designed according to its power rating.

$$RS2 = \frac{V_{out} - 15.6V}{10mA}$$

$$P_{RS2} = (10mA)^2 RS2 \leq {}^{P_{RS2\_Rated}}\!/_{2}$$

$$Icc \approx 10mA$$

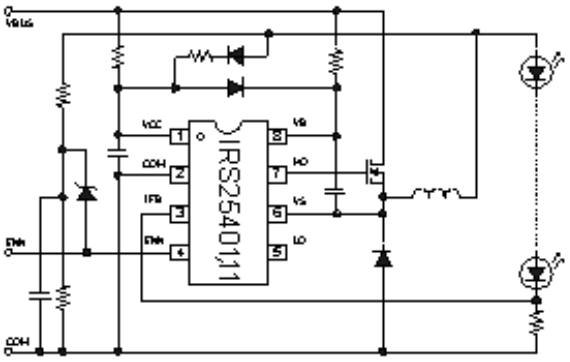
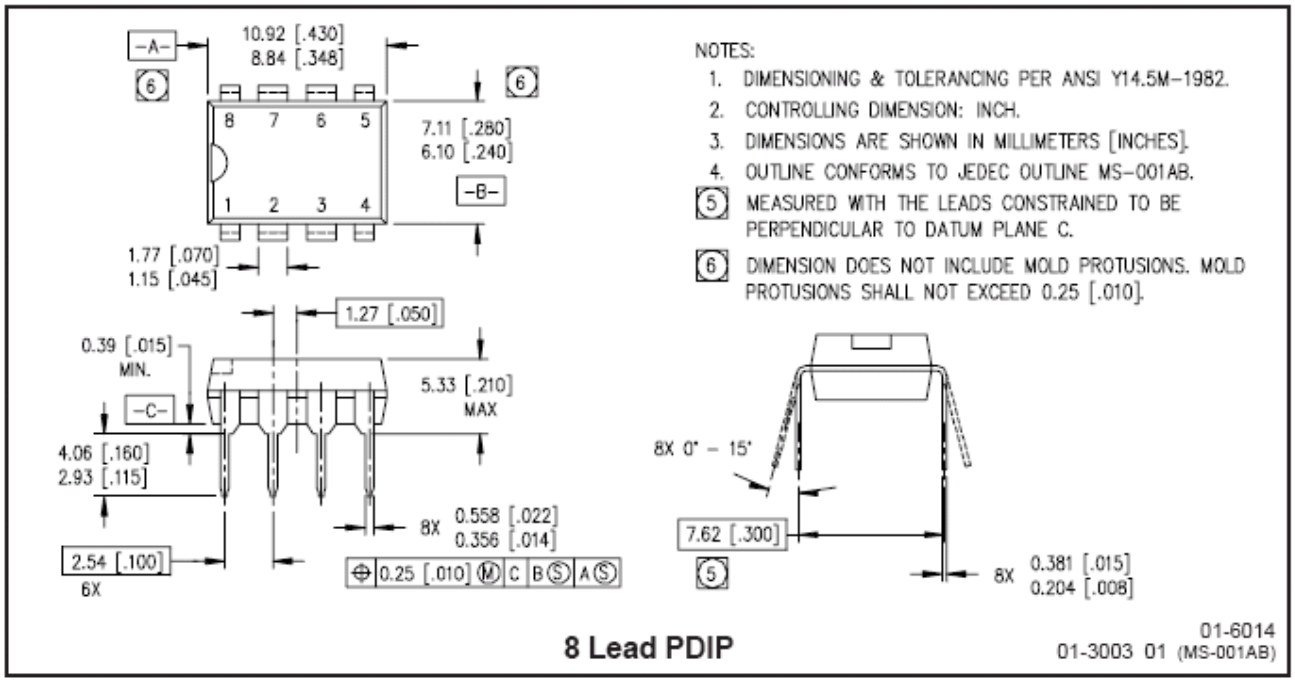
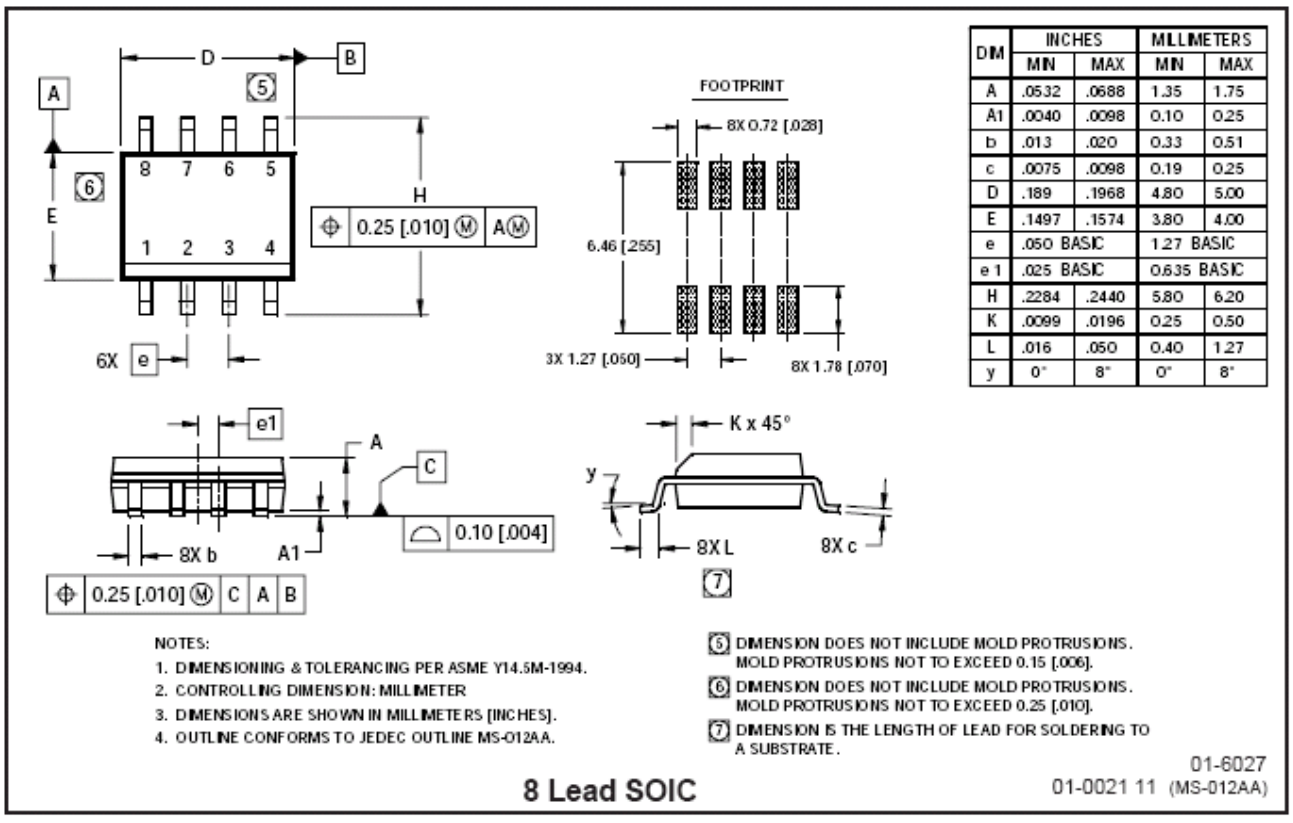


Fig. 16 Alternate Supply Diagram

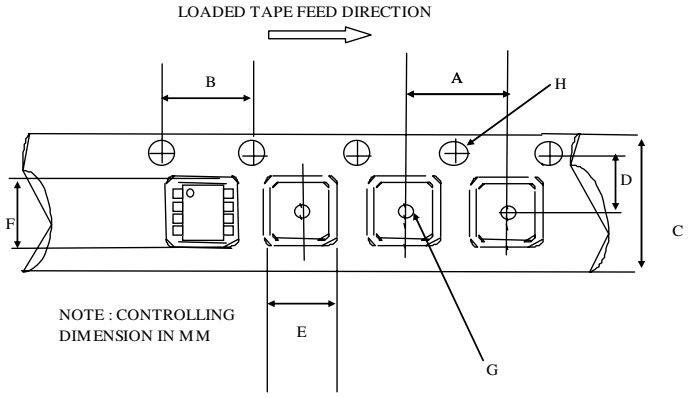
Package Details





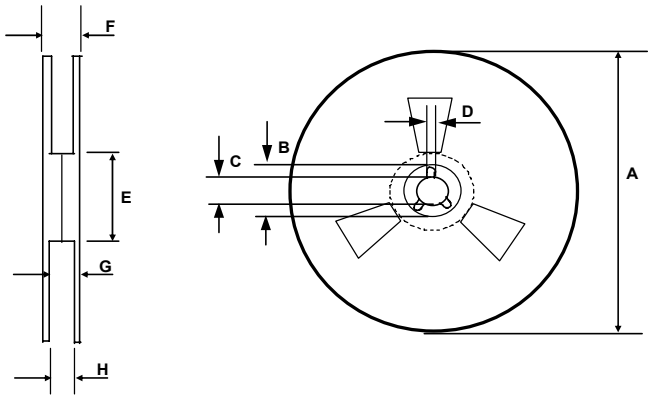
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

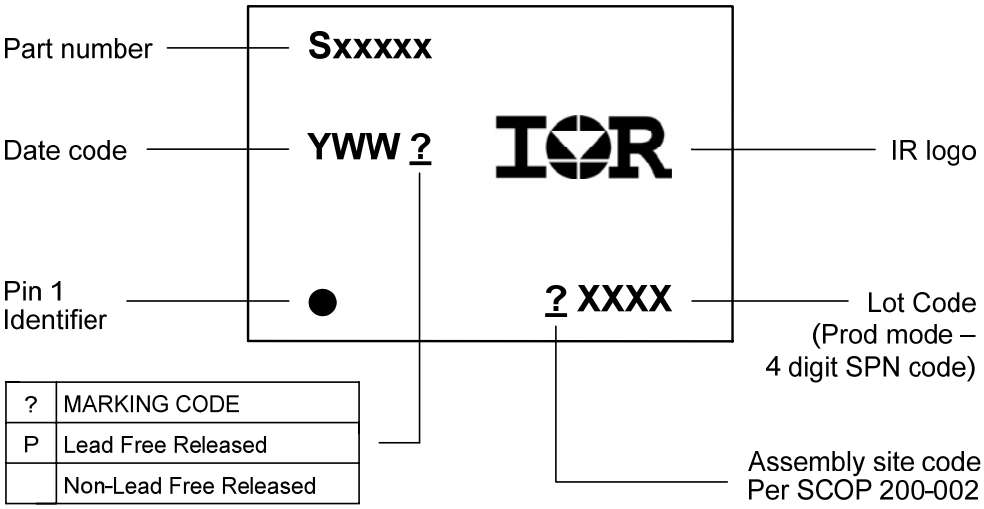


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

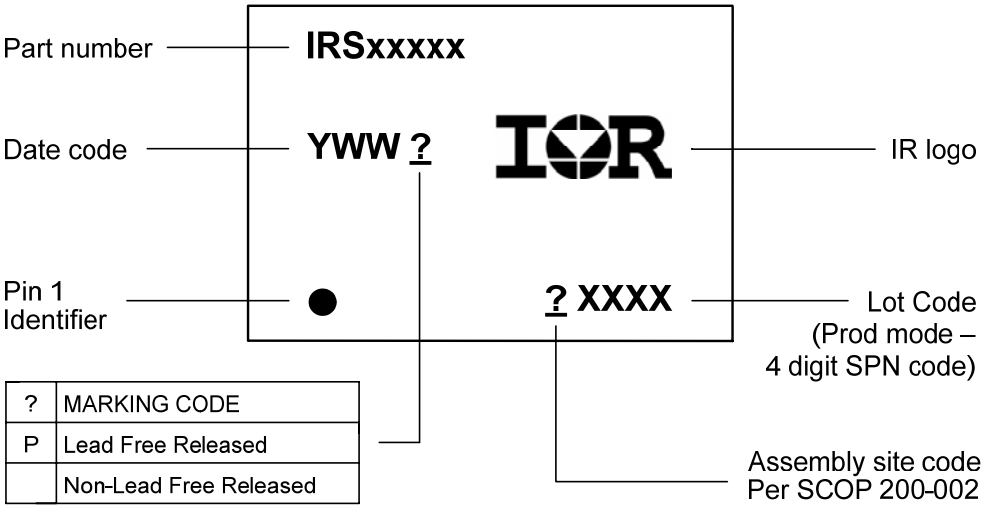
Part Marking Information

SOIC



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

PDIP



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS25401	PDIP8	Tube/Bulk	50	IRS25401PBF
	SOIC8	Tube/Bulk	95	IRS25401SPBF
		Tape and Reel	2500	IRS25401STRPBF
IRS25411	PDIP8	Tube/Bulk	50	IRS25411PBF
	SOIC8	Tube/Bulk	95	IRS25411SPBF
		Tape and Reel	2500	IRS25411STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105