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International
IOR Rectifier

Data Sheet No. PD 97408B
May 30, 2011

IRS26072DSPbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Integrated bootstrap diode suitable for Complimentary PWM switching schemes only
- IRS26072DSPBF is suitable for sinusoidal motor control applications
- **IRS26072DSPBF is NOT recommended for Trapezoidal motor control applications**
- Fully operational to 600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Under-Voltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant

Typical Applications

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drivers

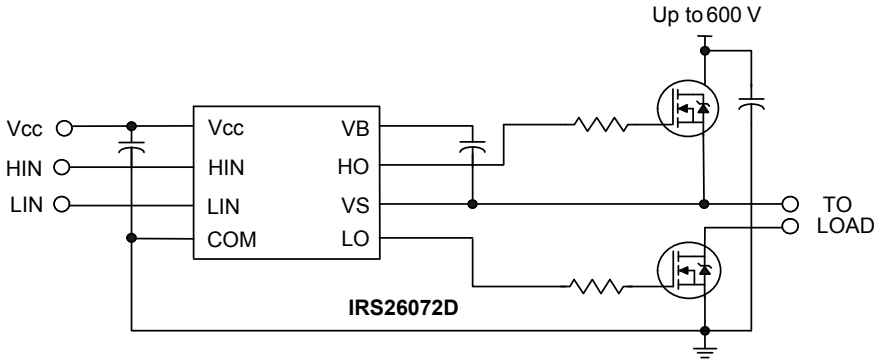
Product Summary

Topology	high and low side driver
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	200 mA & 350 mA
t_{ON} & t_{OFF} (typical)	200 ns

Package Options

8-Lead SOIC

Typical Connection Diagram



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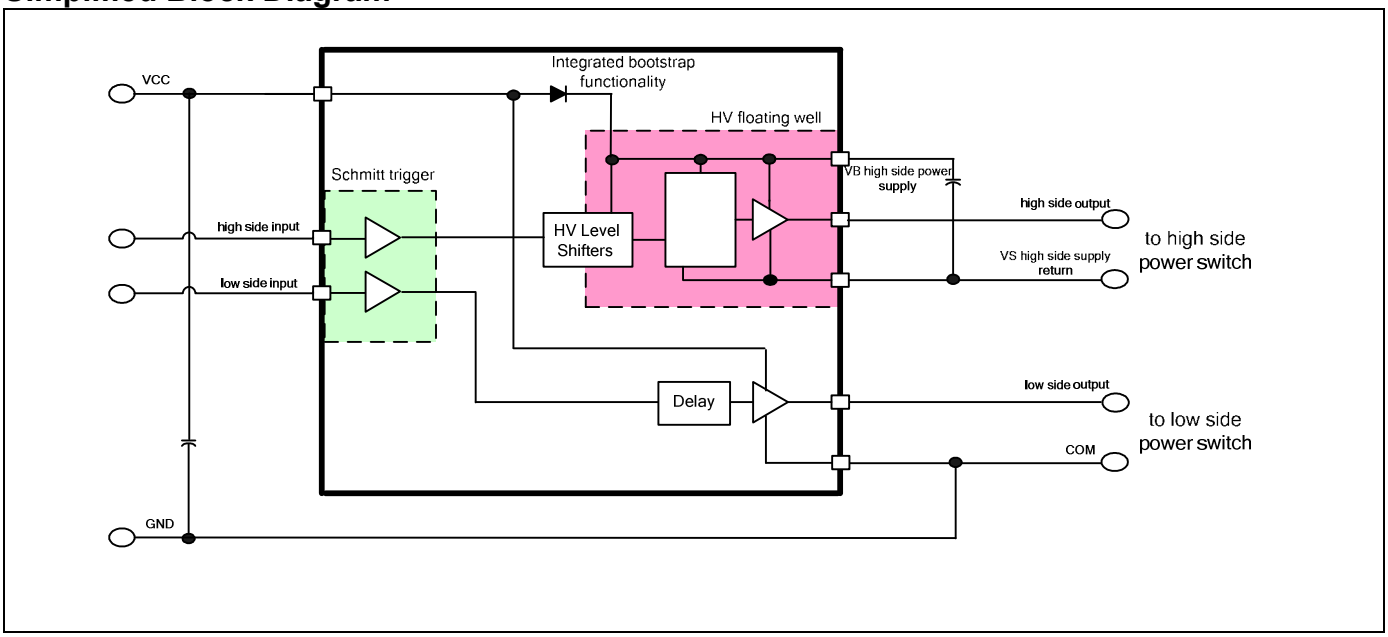
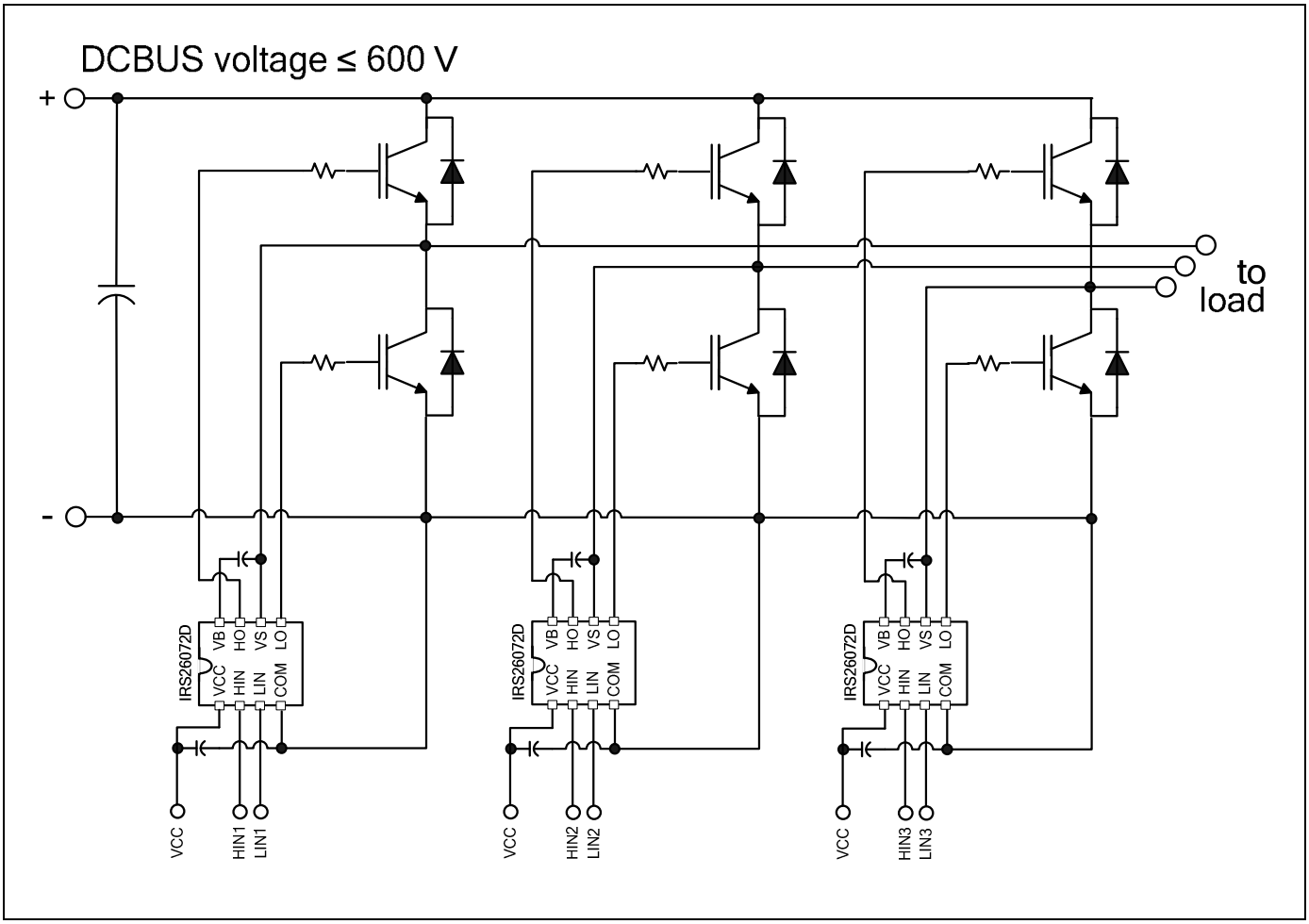
Description

The IRS26072D is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration up to 600 V.

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††
		Comments: This IC has passed JEDEC industrial qualification. IR consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2 , 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise specified. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	620	V
V_S	High side floating supply offset voltage	V_B - 20†	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20†	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic and analog input voltages	-0.3	V_{CC} + 0.3	
PW_{HIN}	High-side input pulse width	500	—	ns
dV_S/dt	Allowable offset supply voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise specified. The V_S offset ratings are tested with all supplies biased at 15 V.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +10	V_S + 20	V
V_S	Static high side floating supply offset voltage†	-8	600	
$V_S(t)$	Transient high side floating supply offset voltage††	-50	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to $–V_{BS}$.
†† Operational for transient negative V_S of -50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S and are applicable to the output leads LO and HO respectively. The V_{CCUV} and V_{BSUV} parameters are referenced to COM and V_S respectively.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
V_{OH}	High level output voltage	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage	—	0.2	0.6		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold	6.9	7.7	8.5		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under-voltage hysteresis	0.35	1.2	—		
I_{LK}	Offset supply leakage current	—	1	50	µA	V_B =V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	1.1	1.8	mA	
I_{IN+}	Logic "1" input bias current	—	5	20	µA	V_{IN} = 5 V
I_{IN-}	Logic "0" input bias current	—	—	2		V_{IN} = 0 V
I_{o+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0 V or 15 V PW ≤ 10 µs
I_{o-}	Output low short circuit pulsed current	250	350	—		
R_{BS}	Bootstrap resistance ††	—	200	—	Ω	

†† Integrated bootstrap diode is suitable for Complimentary PWM schemes only. IRS26072D is suitable for sinusoidal motor control applications. IRS26072D is NOT recommended for Trapezoidal motor control applications. Refer to the Integrated Bootstrap Functionality section of this datasheet for more details.

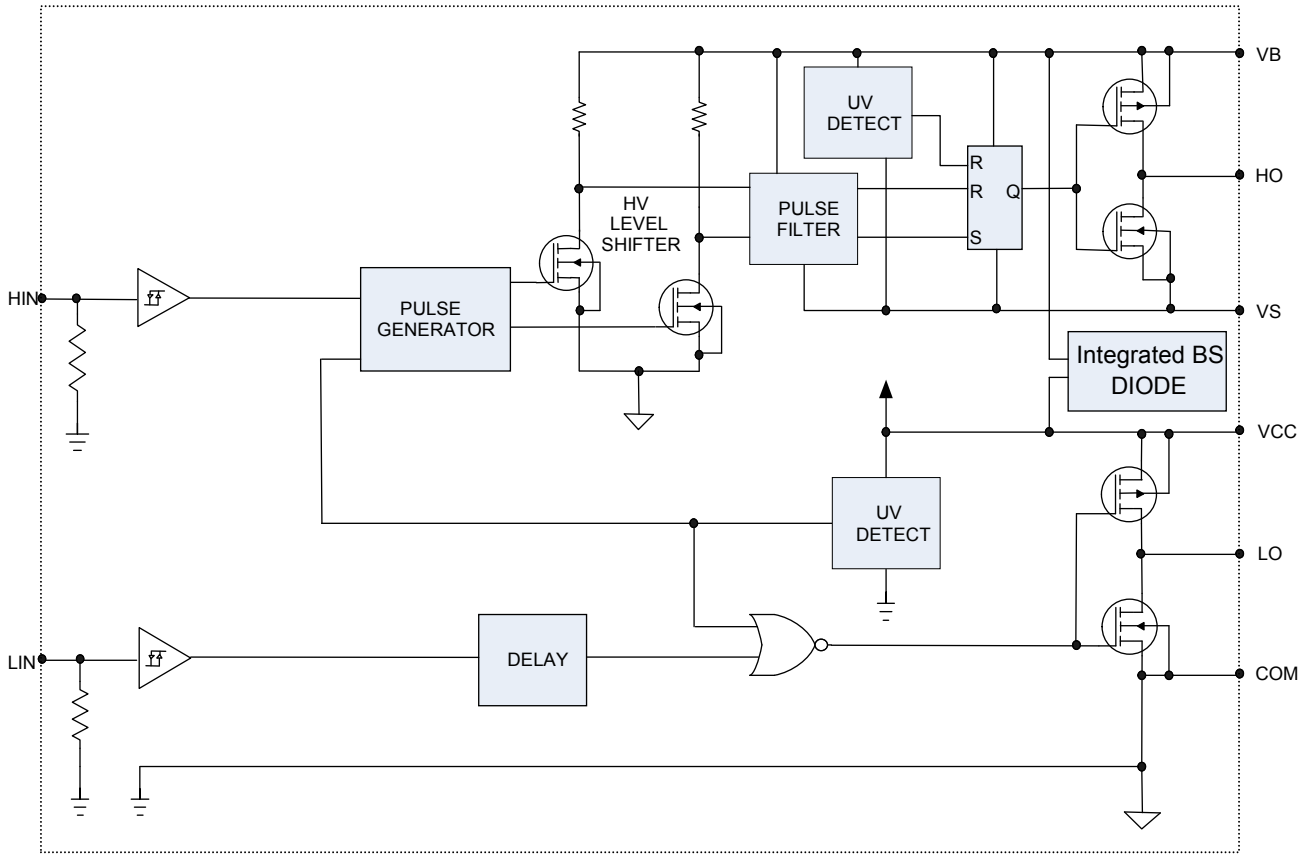
Dynamic Electrical Characteristics

V_{CC} = V_B = 15 V, V_S = COM, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

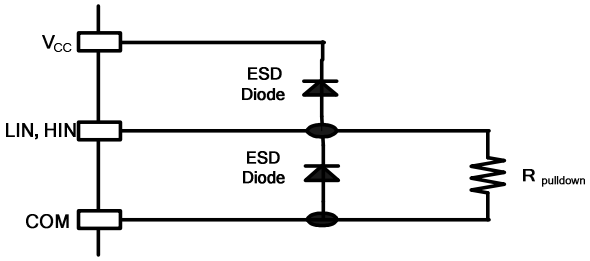
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	100	200	300	ns	V_{IN} = 0V and 5V
t_{off}	Turn-off propagation delay	100	200	300		
t_r	Turn-on rise time	—	150	220		
t_f	Turn-off fall time	—	50	80		
MT	t_{on}, t_{off} propagation delay matching time	—	—	50		
PM	PW pulse width distortion†	—	—	75		PW input =10µs

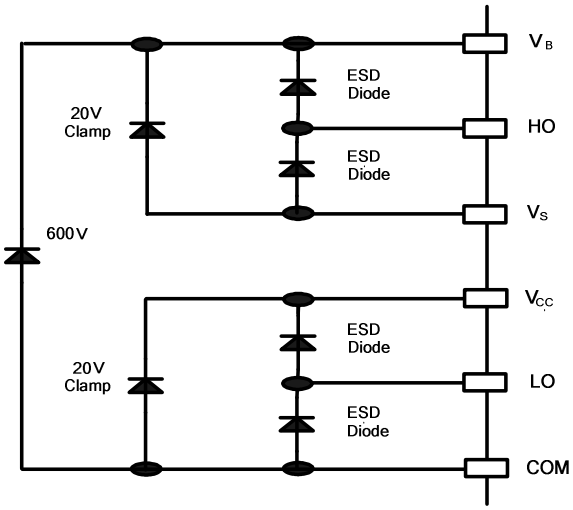
† PM is defined as PW_{IN} - PW_{OUT}.

Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams

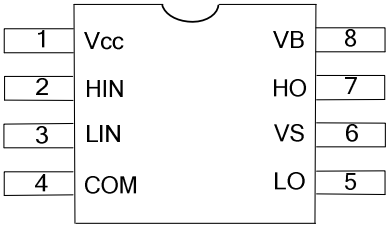




Lead Definitions

Symbol	Description
VCC	Low side and logic power supply
VB	High side floating power supply
VS	High side floating supply return
HIN	Logic input for high side gate driver output HO, input is in-phase with output
LIN	Logic input for low side gate driver output LO, input is in-phase with output
HO	High side gate driver output
LO	Low side gate driver output
COM	Low side supply return

Lead Assignments



Application Information and Additional Details

IGBT/MOSFET Gate Drive

The IRS26072D HVIC is designed to drive high side and low side MOSFET or IGBT power devices. Figures 1 and 2 show the definition of some of the relevant parameters associated with the gate driver output functionality. The output current that drives the gate of the external power switches is defined as I_O. The output voltage that drives the gate of the external power switches is defined as V_{HO} for the high side and V_{LO} for the low side; this parameter is sometimes generically called V_{OUT} and in this case the high side and low side output voltages are not differentiated.

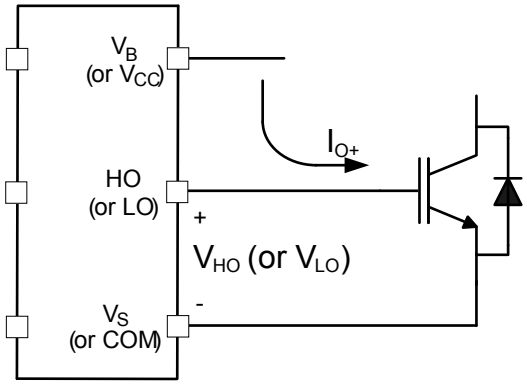


Figure 1: HVIC sourcing current

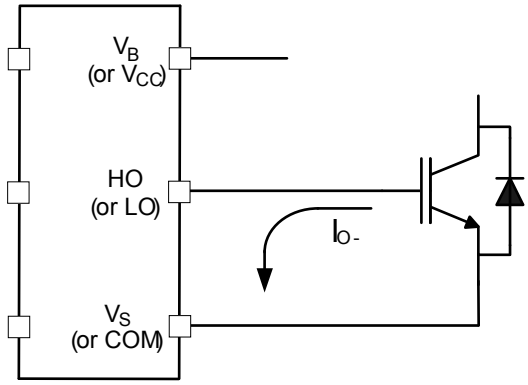


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS26072D HVIC is shown in Figure 3. The definitions of some of the relevant parameters associated with the gate driver input to output transmission are given.

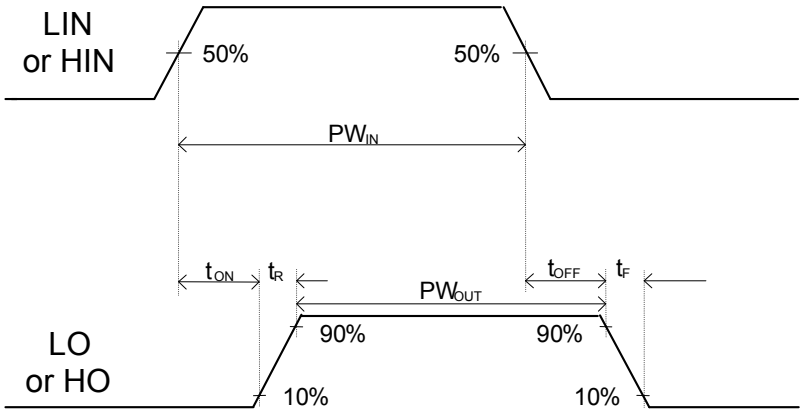


Figure 3: Switching time waveforms

During interval A of Figure 4 the HVIC receives the command to turn on both the high and low side switches at the same time; correspondingly, the high and low side signals HO and LO turn on simultaneously.

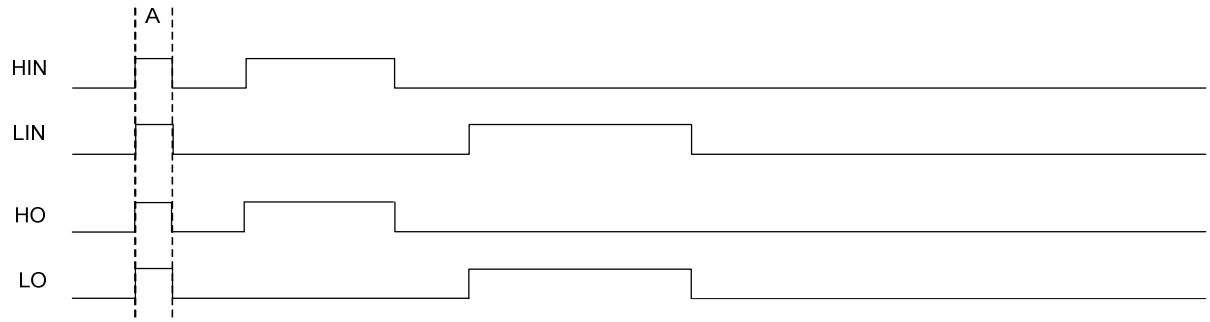


Figure 4: Input/output timing diagram

Matched Propagation Delays

The IRS26072D HVIC is designed for propagation delay matching. With this feature, the input to output propagation delays t_{ON}, t_{OFF} are the same for the low side and the high side channels; the maximum difference being specified by the delay matching parameter MT as defined in Figure 6.

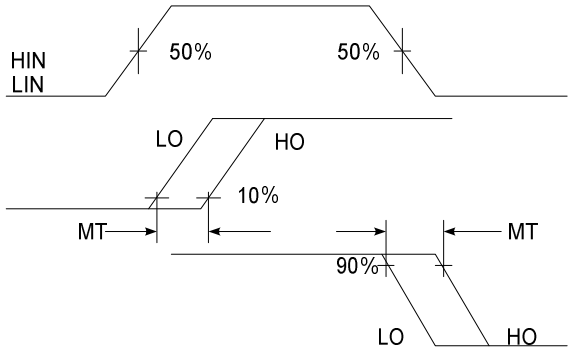


Figure 6: Delay Matching Waveform Definition

Input Logic Compatibility

The IRS26072D HVIC is designed with inputs compatible with standard CMOS and TTL outputs with 3.3 V and 5 V logic level signals. Figure 7 shows how an input signal is logically interpreted.

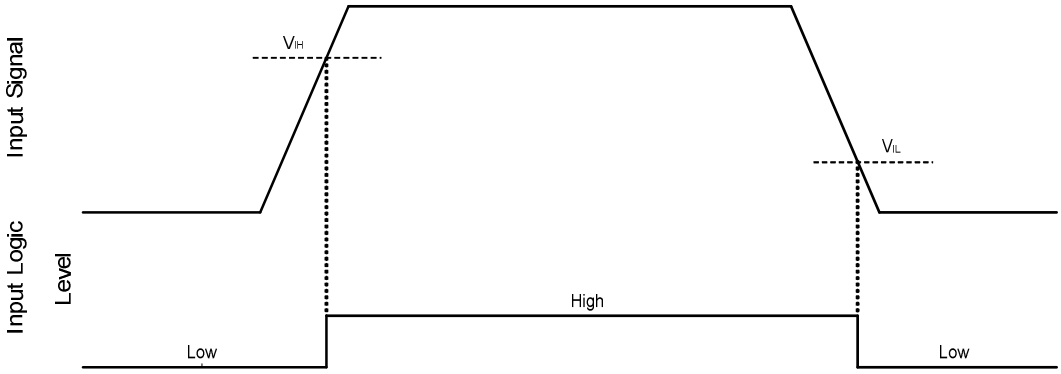


Figure 7: HIN & LIN input thresholds

Under-Voltage Lockout Protection

The IRS26072D HVIC provides under-voltage lockout protection on both the V_{CC} low side and logic fixed power supply and the VBS high side floating power supply. Figure 8 illustrates this concept by considering the V_{CC} (or V_{BS}) plotted over time: as the waveform crosses the UVLO threshold, the under-voltage protection is entered or exited.

Upon power up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the gate driver outputs LO and HO will remain disabled. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during normal operation, the under-voltage lockout circuitry will shutdown the gate driver outputs LO and HO.

Upon power up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the gate driver output HO will remain disabled. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during normal operation, the under-voltage lockout circuitry will shutdown the high side gate driver output HO.

The UVLO protection ensures that the HVIC drives external power devices only with a gate supply voltage sufficient to fully enhance them. Without this protection, the gates of the external power switches could be driven with a low voltage, which would result in power switches conducting current while with a high channel impedance, which would produce very high conduction losses possibly leading to power device failure.

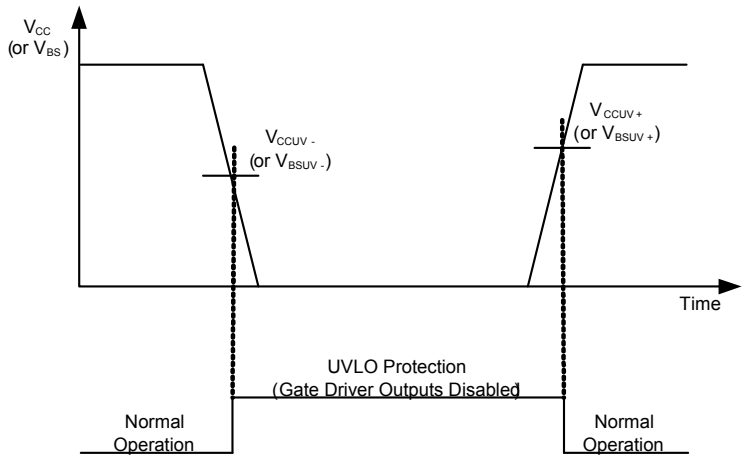


Figure 8: UVLO protection

Truth Table: Under-Voltage lockout

Table 2 provides the truth table for the IRS26072D HVIC.

The 1st line shows that for V_{CC} below the UVLO threshold both the gate driver outputs LO and HO are disabled. After V_{CC} returns above V_{CCUV}, the gate driver outputs return functional.

The 2nd line shows that for V_{BS} below the UVLO threshold, the gate driver output HO is disabled. After V_{BS} returns above V_{BSUV}, HO remains low until a new rising transition of HIN is received.

The last line shows the normal operation of the HVIC.

	VCC	VBS	outputs	
			LO	HO
UVLO V_{CC}	$<V_{CCUV}$		0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	LIN	0
Normal operation	15 V	15 V	LIN	HIN

Table 2: UVLO truth table

Integrated Bootstrap Functionality

The IRS26072D HVIC embeds an integrated bootstrap FET that eliminates the need of external bootstrap diodes and resistors allowing an alternative drive of the bootstrap supply for a wide range of applications.
A bootstrap FET is connected between the high side floating power supply VB and the low side and logic fixed power supply VCC (see Fig. 9).

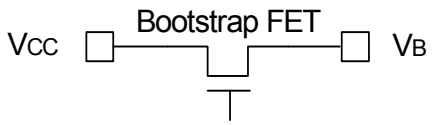


Figure 9: Simplified Bootstrap FET connection

The bootstrap FET is suitable for complimentary PWM switching schemes only. Complimentary PWM refers to PWM schemes where the HIN & LIN input signals are alternately switched on and off. IRS26072D is suitable for sinusoidal motor control and the integrated bootstrap feature can be used either in parallel with the external bootstrap network (diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations at very high PWM duty cycle, corresponding to very short LIN pulses, due to the bootstrap FET equivalent resistance R_{BS}. **IRS26072D is NOT recommended for trapezoidal motor control, even if an external bootstrap network is employed in parallel.**

The bootstrap FET is conditioned as follows:

- bootstrap turns-off (immediately) or stays off when either:
  - HO goes/stays high;
  - V_B goes/ stays high (> 1.1*V_{CC});
- bootstrap turns-on when:
  - LO is high (low side is on) AND V_B is low (<1.1*V_{CC});
  - LO and HO are low after a transition of LIN from high to low AND V_B goes low (<1.1*V_{CC}) before a fixed time of 20us;
  - LO and HO are low after a transition of HIN from high to low AND V_B goes low (<1.1*V_{CC}) before a re-triggerable time of 20us. In this case the time counter is kept in reset state until VB goes high (>1.1V_{CC}).

In Figure 10 the BootFET timing diagram details are represented.

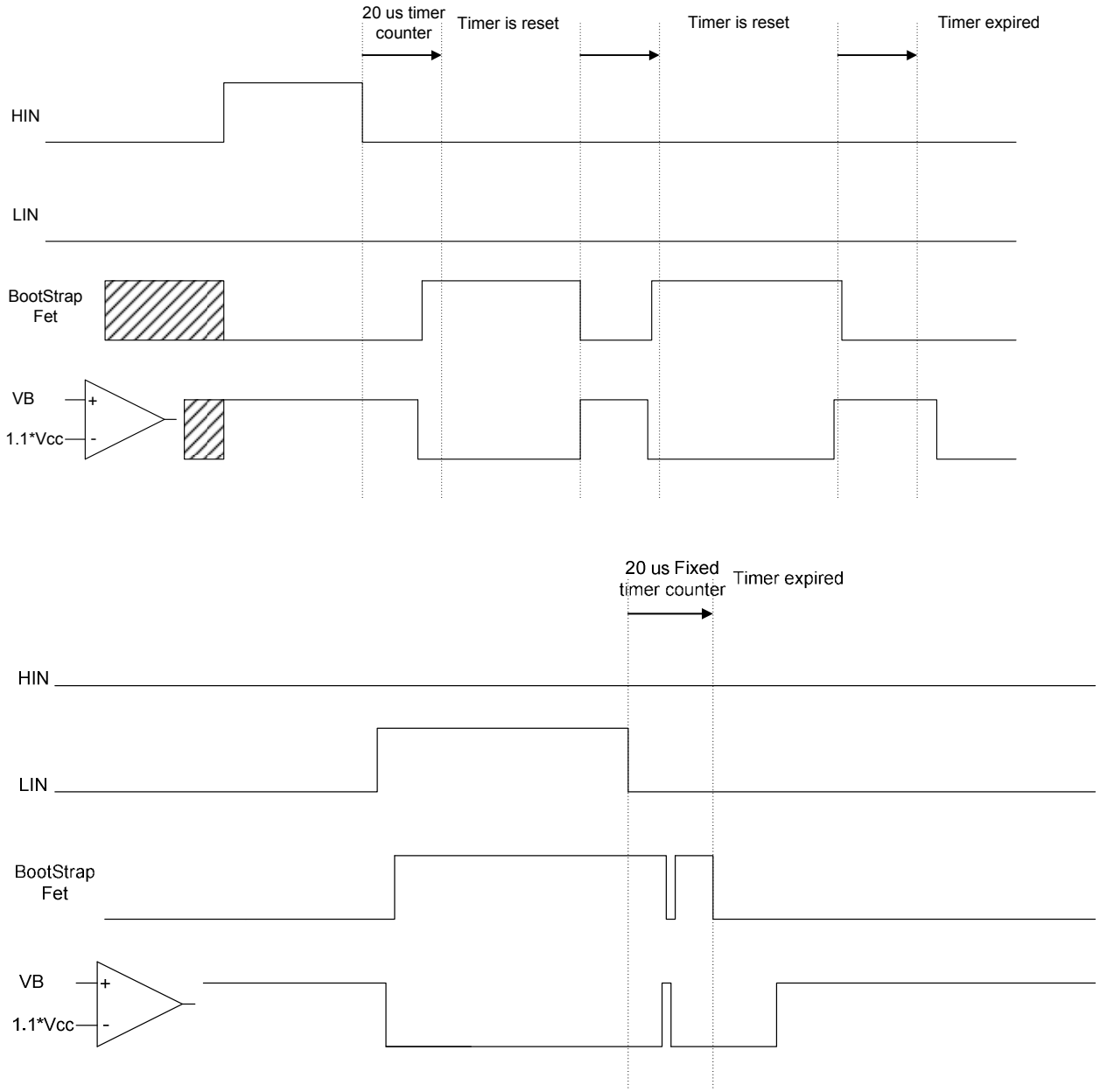


Figure 10: BootFET timing diagram

Bootstrap Power Supply Design

For information related to the design of the bootstrap power supply while using the integrated bootstrap functionality of the IRS26072D, please refer to Application Note 1123 (AN-1123) entitled "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality." This application note is available at www.irf.com.

For information related to the design of a standard bootstrap power supply (i.e., using an external discrete diode) please refer to Design Tip 04-4 (DT04-4) entitled "Using Monolithic High Voltage Gate Drivers." This design tip is available at www.irf.com.

Tolerant to Negative VS Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power devices switch on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 11; where we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 12 and 13) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

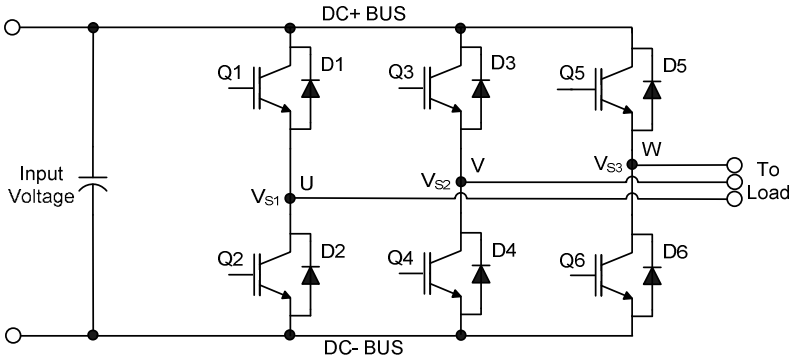


Figure 11: Three phase inverter

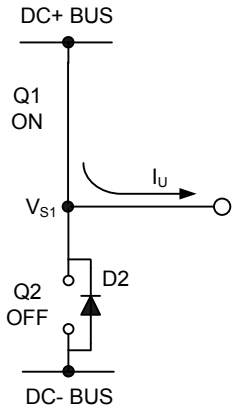


Figure 12: Q1 conducting

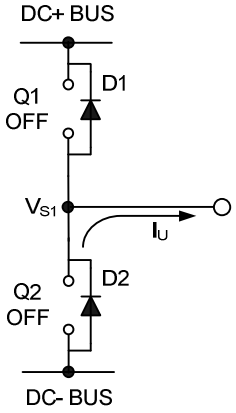


Figure 13: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 14 and 15), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

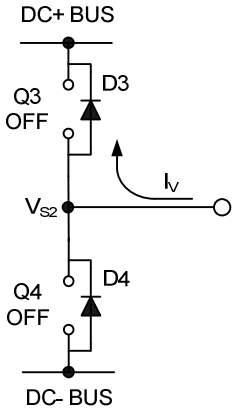


Figure 14: D3 conducting

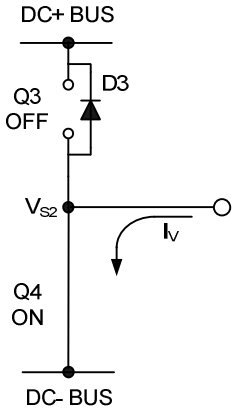


Figure 15: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 16 depicts one leg of the three phase inverter; Figures 17 and 18 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

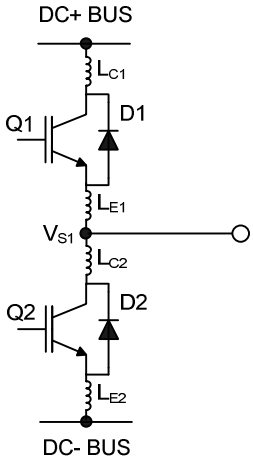


Figure 16: Parasitic Elements

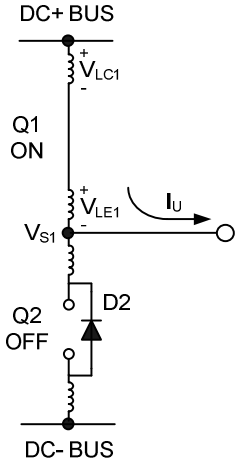


Figure 17: V_S positive

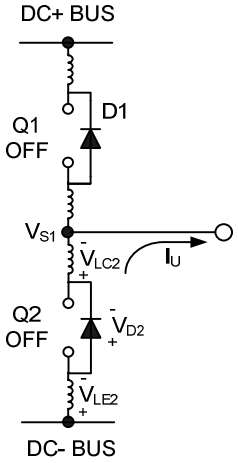


Figure 18: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS26072D's robustness can be seen in Figure 19, where there is represented the IRS26072D Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

At V_{BS}=15V in case of -V_S transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5 µs.

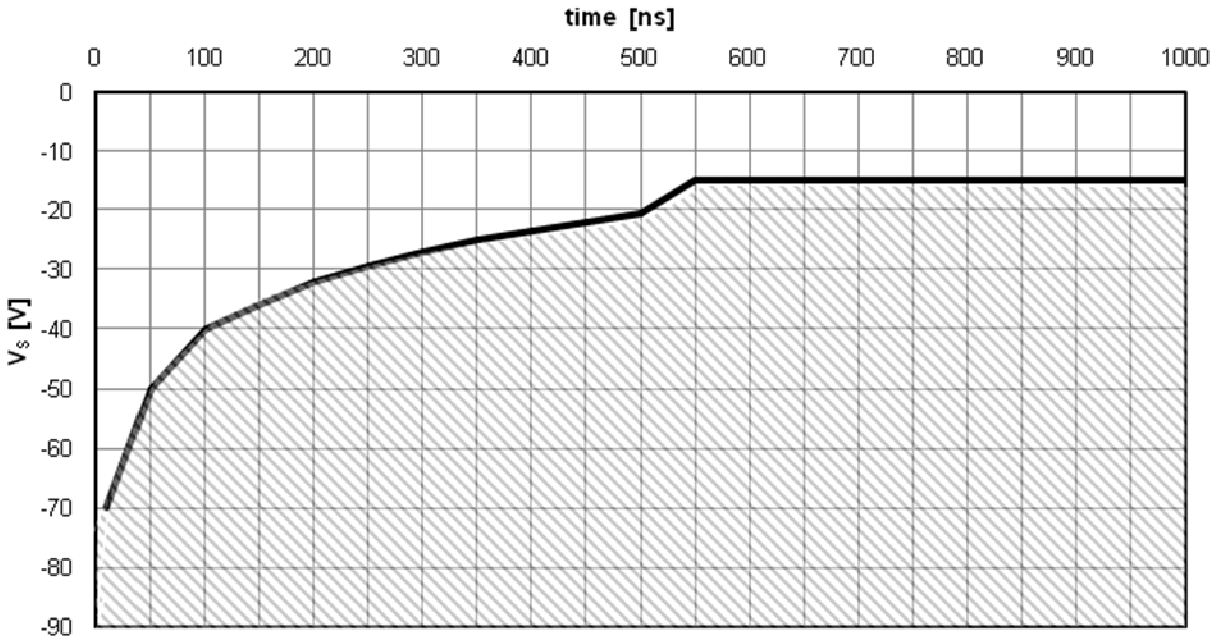


Figure 19: Negative V_S transient SOA @ VBS=15V

Even though the IRS26072D has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 20). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

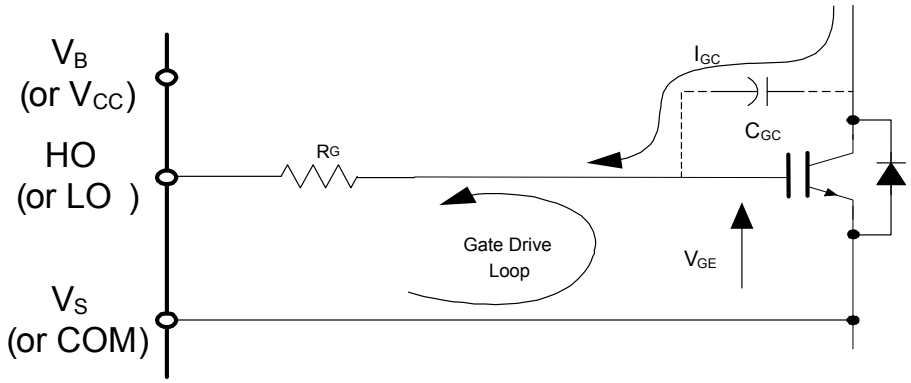


Figure 20: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor between the VCC and COM pins. This connection is shown in Figure 21. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

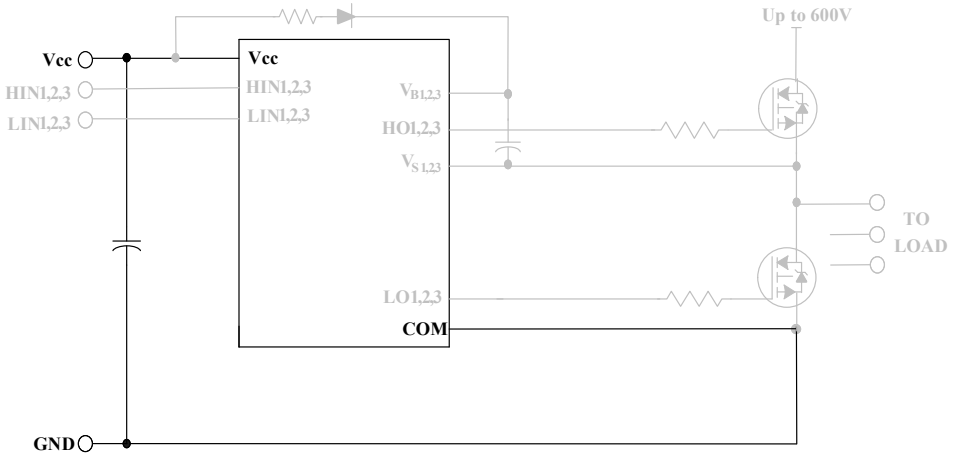


Figure 21: Supply capacitor

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side source to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 22), and in some cases using a clamping diode between COM and V_S (see Figure 23). See DT04-4 at www.irf.com for more detailed information.

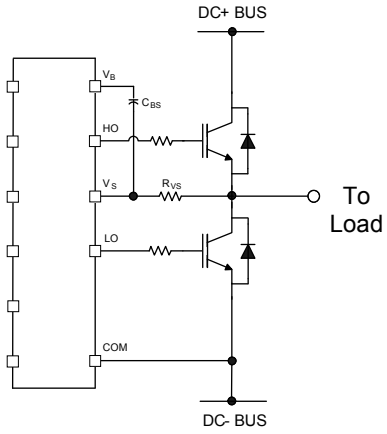


Figure 22: V_S resistor

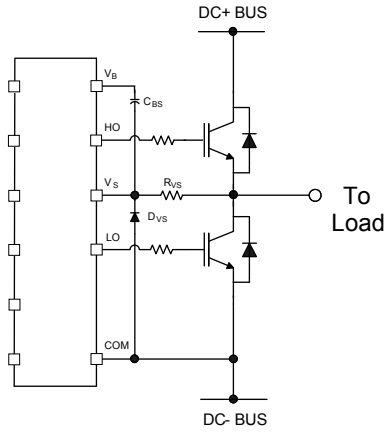


Figure 23: V_S clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.24 below, resulting in power loss and possible damage to the HVIC.

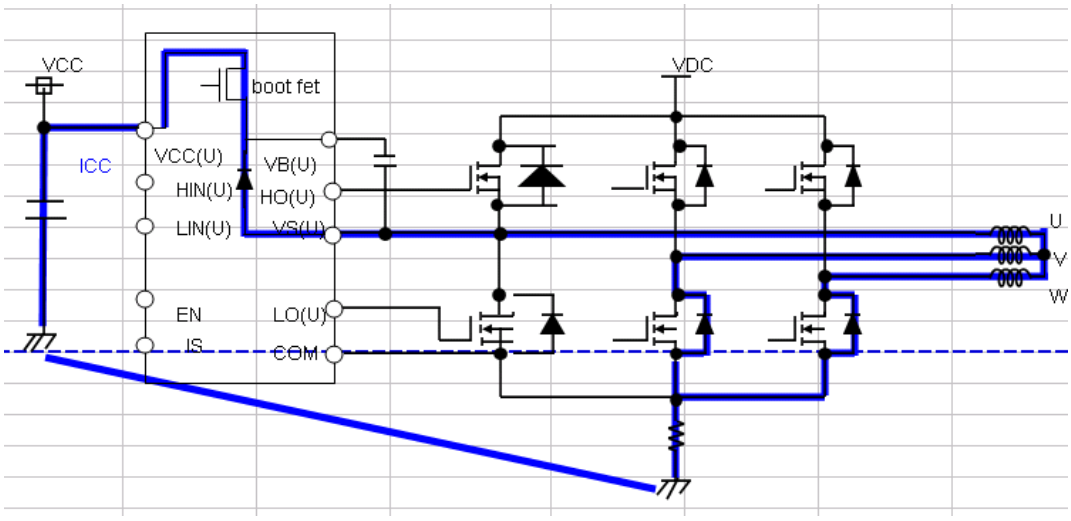


Figure 24: Current conduction path between VCC and VB pin

Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.25) prevents current conduction "out-of" VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

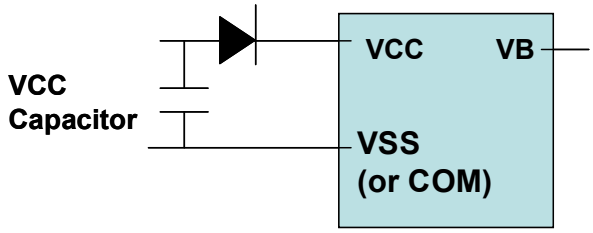


Figure 25: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage – V_F of Diode*.

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Parameter Temperature Trends

Figures 26-43 provide information on the experimental performance of the IRS26072D HVIC. The line plotted in each figure is generated from actual experimental data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

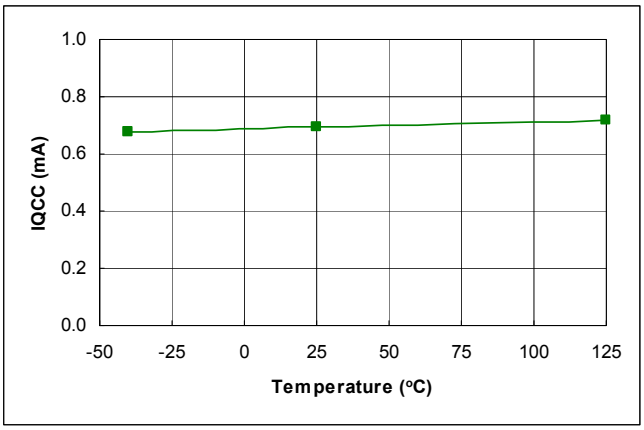


Figure 26: I_{QCC} vs. temperature

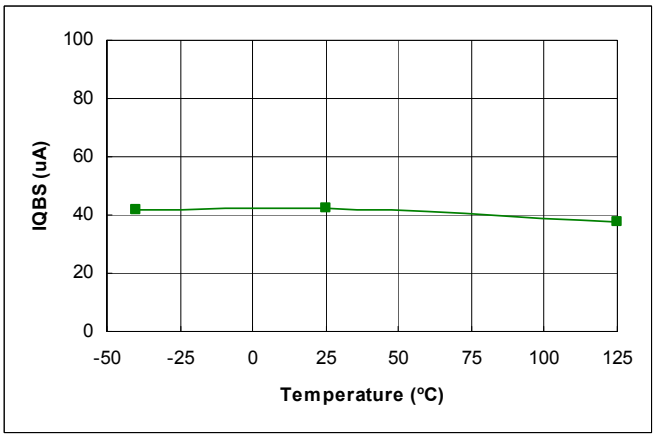


Figure 27: I_{QBS} vs. temperature

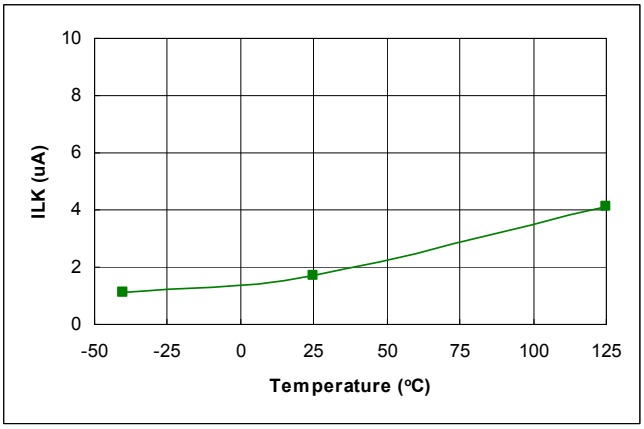


Figure 28: I_{LK} vs. temperature

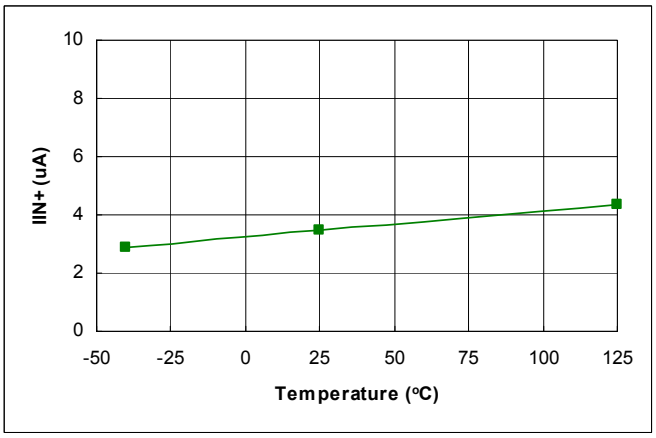


Figure 29: I_{IN+} vs. temperature

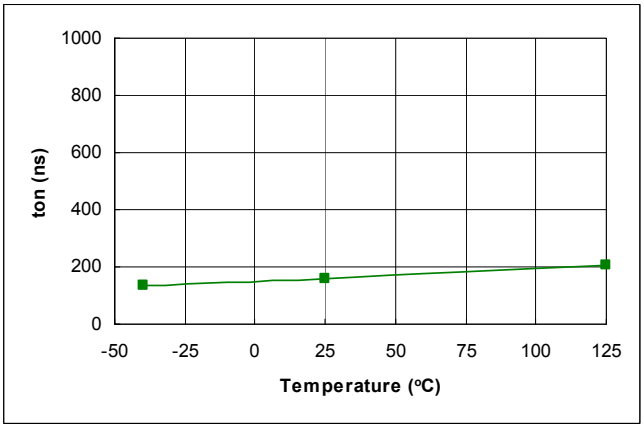


Figure 30: t_{ON} vs. temperature

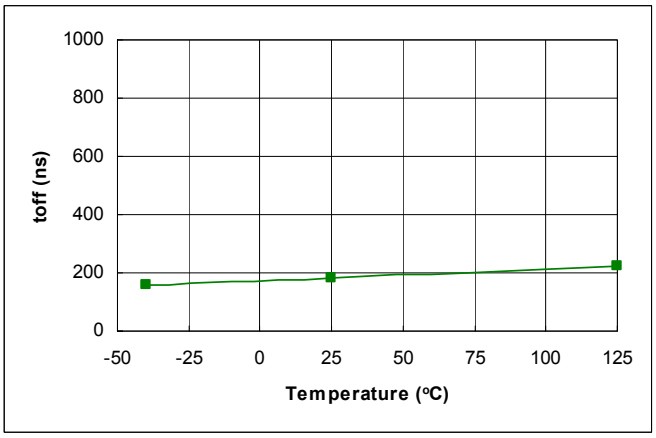


Figure 31: t_{OFF} vs. temperature

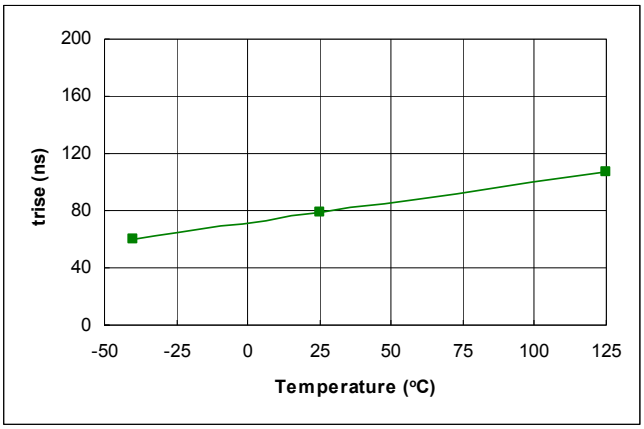


Figure 32: t_{RISE} vs. temperature

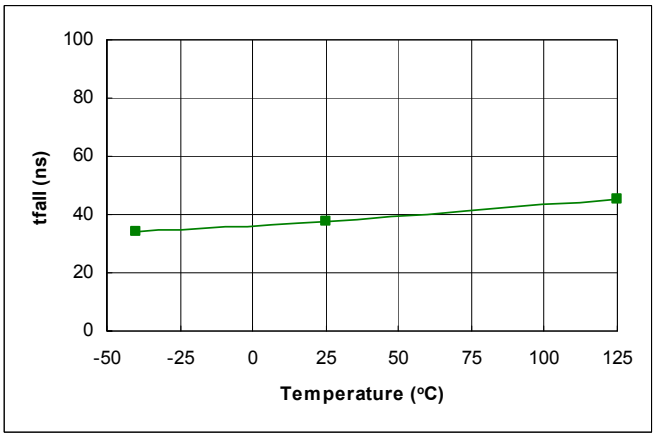


Figure 33: t_{FALL} vs. temperature

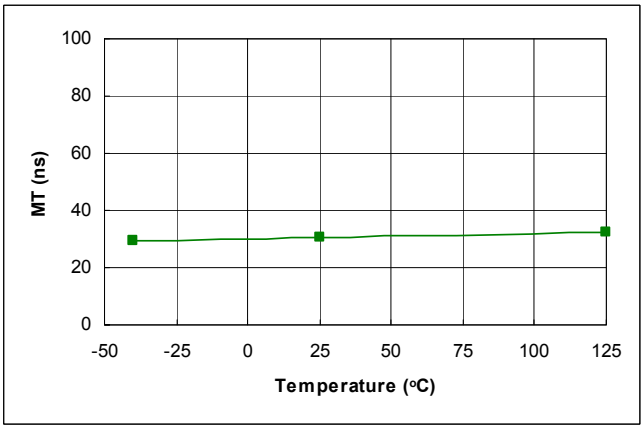


Figure 34: MT vs. temperature

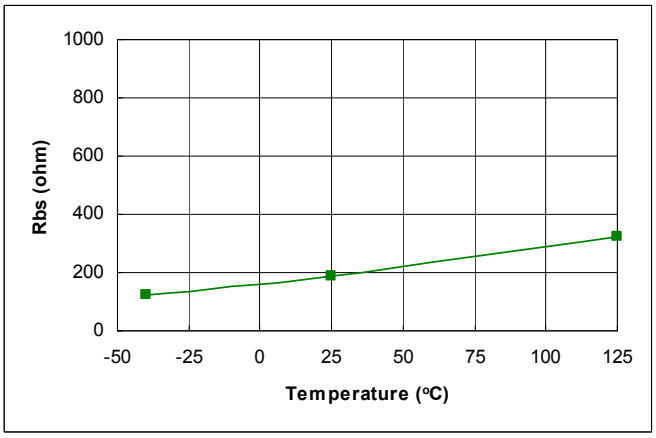


Figure 35: R_{BS} vs. temperature

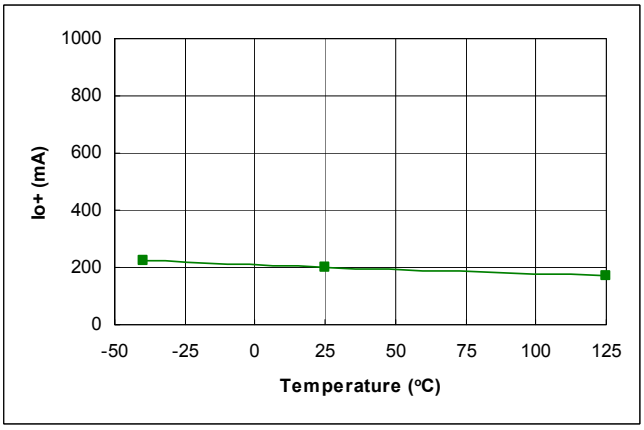


Figure 36: I_{O+} vs. temperature

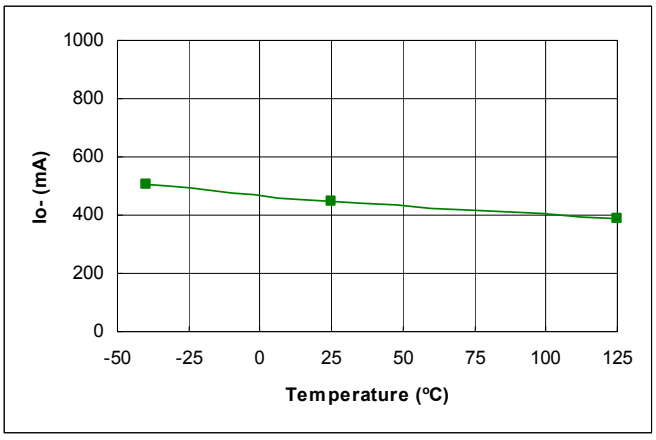


Figure 37: I_{O-} vs. temperature

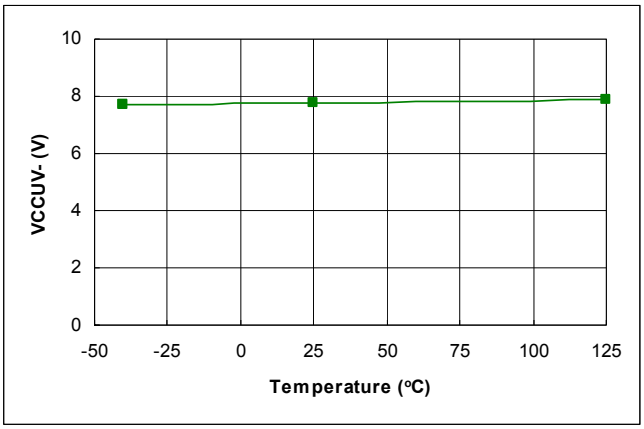


Figure 38: V_{CCUV-} vs. temperature

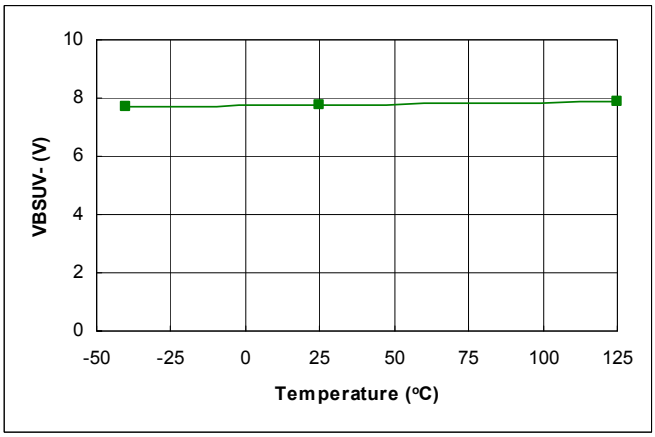


Figure 39: V_{BSUV-} vs. temperature

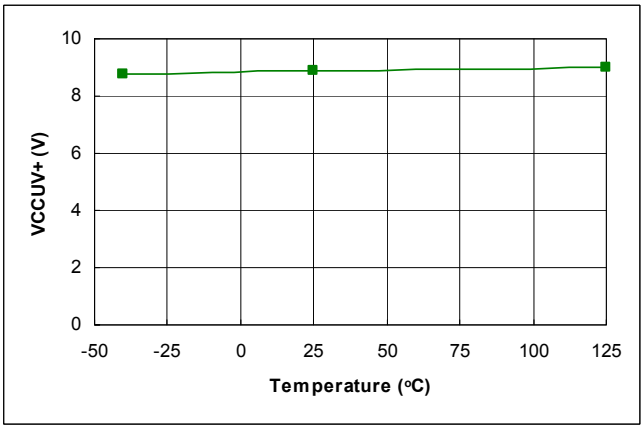


Figure 40: V_{CCUV+} vs. temperature

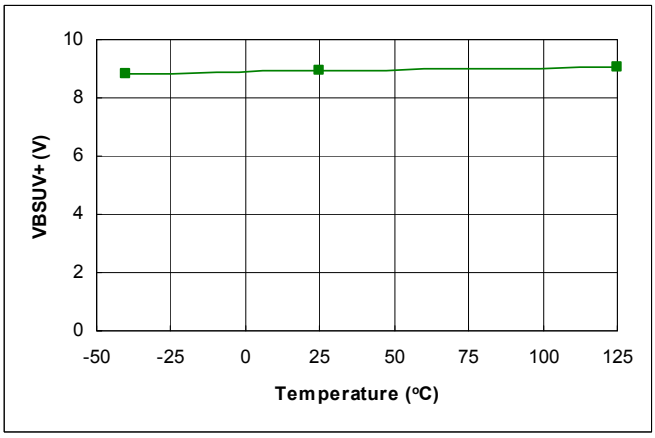


Figure 41: V_{BSUV+} vs. temperature

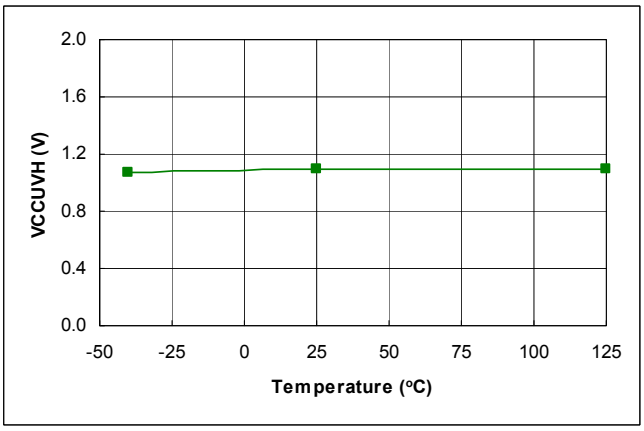


Figure 42: V_{CCUVH} vs. temperature

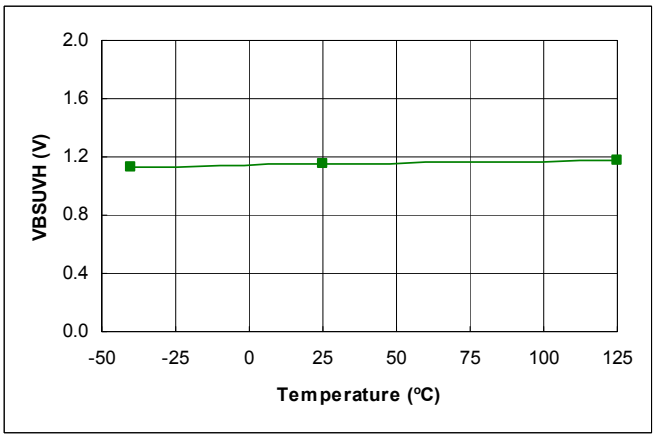


Figure 43: V_{BSUVH} vs. temperature