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International
IOR Rectifier

Data Sheet No. PD 60273

IRS2607DSPbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Integrated bootstrap diode
- Suitable for both trapezoidal and sinusoidal motor control
- RoHS compliant

Packages

8-Lead SOIC

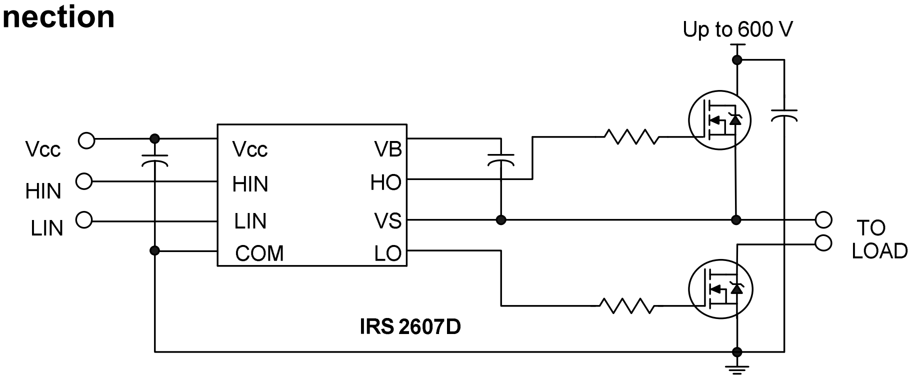
Applications:

*Motor Control
*Air Conditioners/ Washing Machines
*General Purpose Inverters
*Micro/Mini Inverter Drives

Description

The IRS2607D is a high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Qualification Information†

Qualification Level		Industrial†† Comments: This IC has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2, 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	620	V
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage	COM -0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \le +25$ °C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Note 1: Zener clamps are included between VCC & COM, VB & VS (20V).

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	Static High side floating supply offset voltage	COM- 8(Note 1)	600	
V_{St}	Transient High side floating supply offset voltage	-50 (Note2)	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -8 V to +600 V. Logic state held for V_S of -8 V to – $V_{BS.}$

Note 2: Operational for transient negative VS of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

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Static Electrical Characteristics

V_{CC} = V_{BS} = 15 V and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to COM and are applicable to the respective input leads. The V_O, I_O, and R_{ON} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.2	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8	V	
V_{OH}	High level output voltage	—	0.8	1.4	V	I_O = 20 mA
V_{OL}	Low level output voltage	—	0.3	0.6	V	I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70	µA	V_{IN} = 0 V or 4 V
I_{QCC}	Quiescent V_{CC} supply current	400	1100	1800	µA	V_{IN} = 0 V or 4 V
I_{IN+}	Logic "1" input bias current	—	5	20	µA	V_{IN} = 4 V
I_{IN-}	Logic "0" input bias current	—	—	2	µA	V_{IN} = 0 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	6.9	7.7	8.5	V	
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage hysteresis	—	1.2	—	V	
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—	mA	V_O = 15 V, PW ≤ 10 µs
R_{BS}	Bootstrap resistance	—	200	—	Ω	

Note: Please refer to Application Section for integrated bootstrap description.

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = 15 V, C_L = 1000 pF, T_A = 25 °C

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	515	715	ns	V_S = 0 V or 600 V
t_{off}	Turn-off propagation delay	—	500	700	ns	V_S = 0 V or 600 V
MT	Delay matching, HS & LS turn-on/off	—	—	50	ns	
t_r	Turn-on rise time	—	150	220	ns	V_S = 0 V
t_f	Turn-off fall time	—	50	80	ns	V_S = 0 V
t_{fil}	Minimum pulse input filter time	—	300	—	ns	

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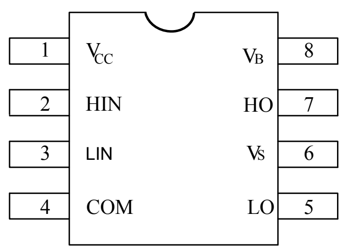
Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead SOIC

IRS2607DS

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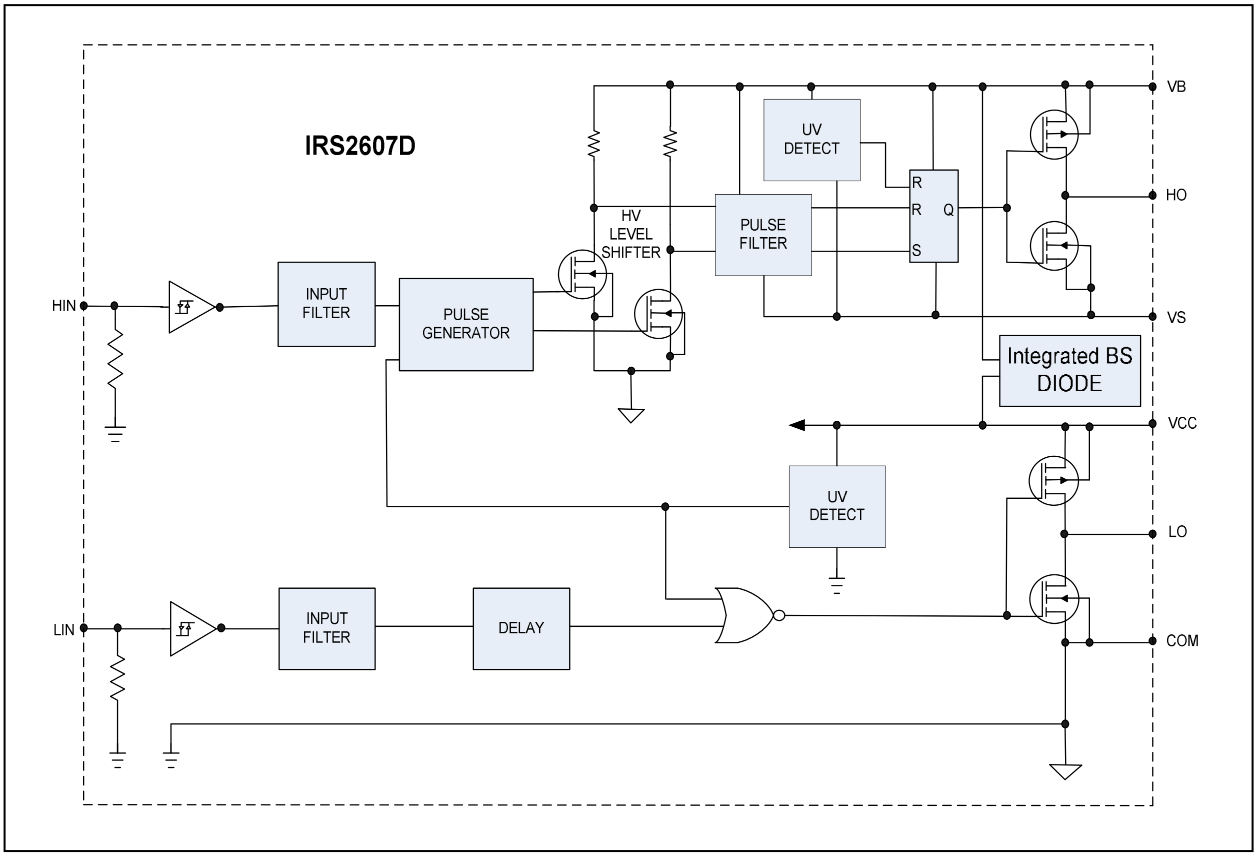
Functional Block Diagrams



Application Information and Additional Details

Informations regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Negative V_S Transient SOA
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS2607D HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

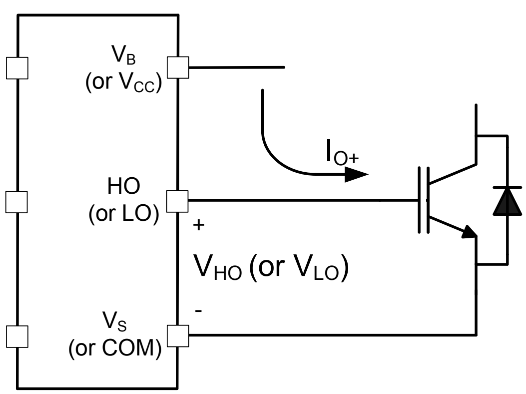


Figure 1: HVIC sourcing current

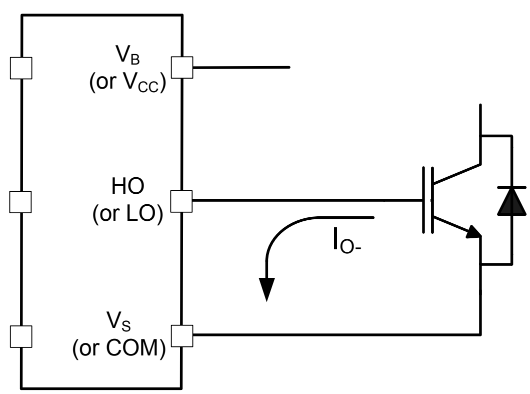


Figure 2: HVIC sinking current

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Switching and Timing Relationships

The relationships between the input and output signals of the IRS2607D are illustrated below in Figures 3, 4. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

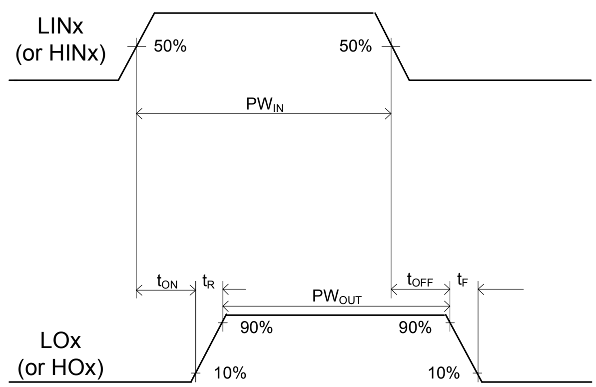

Figure 3: Switching time waveforms

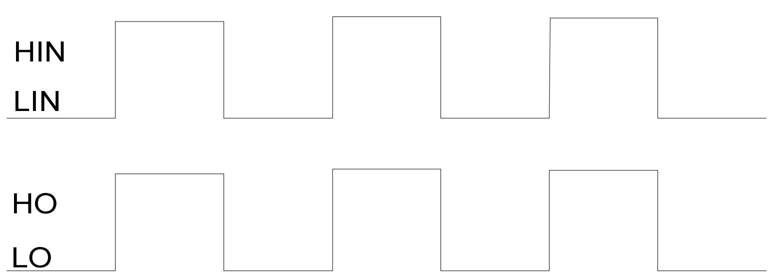

Figure 4: Input/output timing diagram

Matched Propagation Delays

The IRS2607D family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the IRS2607D is matched to the propagation turn-on delay (t_{OFF}).

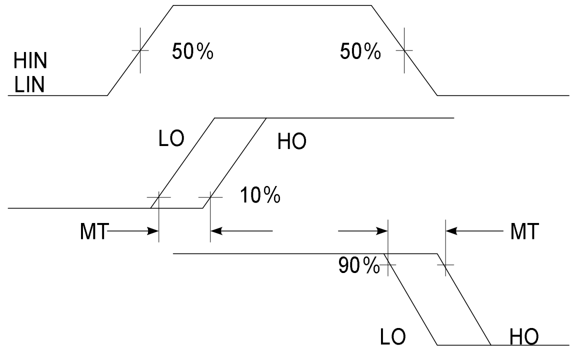

Figure 5: Delay Matching Waveform Definition

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS2607D has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the IRS2607D, its input threshold values, and the logic state of the IC as a result of the input signal.

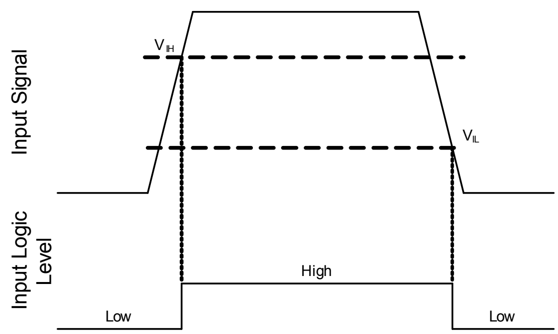

Figure 6: HIN & LIN input thresholds

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Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 7 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

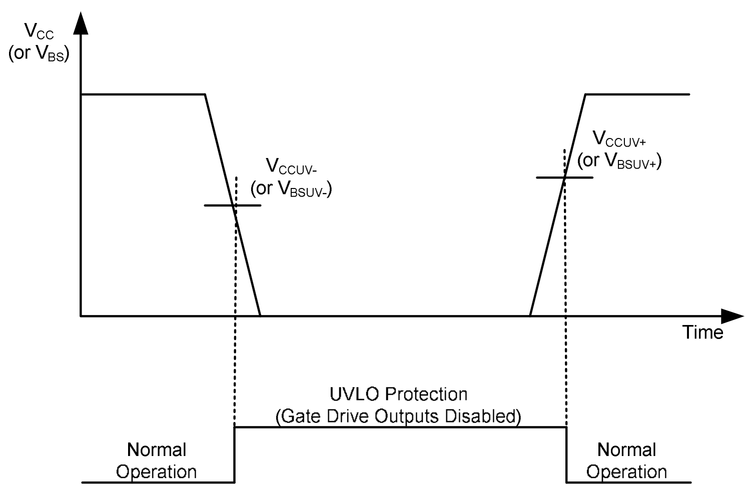

Figure 7: UVLO protection

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Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN ans LIN inputs. The working principle of the new filter is shown in Figures 8 and 9.

Figure 8 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 9 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

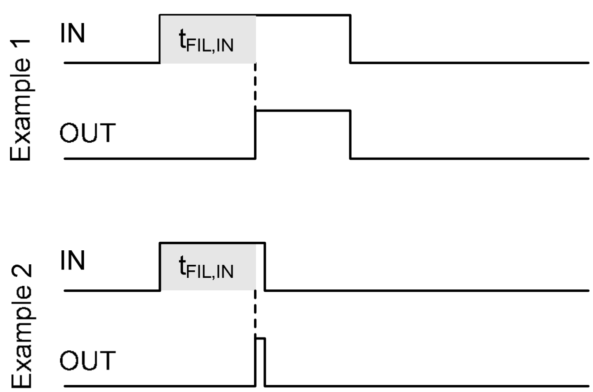

Figure 8: Typical input filter

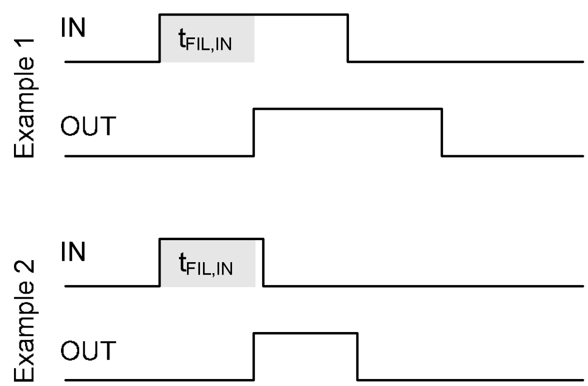

Figure 9: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 10 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 10 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

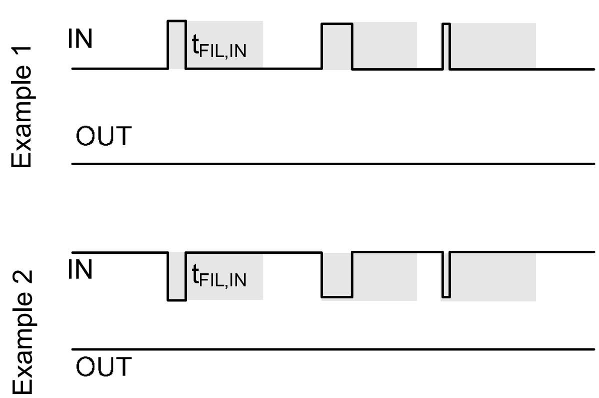

Figure 10: Noise rejecting input filters

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Figures 11 and 12 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 11; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the left shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 11 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PW_{IN} duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PW_{IN} duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PW_{OUT} and PW_{IN} signals of both the narrow ON and narrow OFF cases is shown in Figure 12; the careful reader will note the scale of the y-axis. The x-axis of Figure 12 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

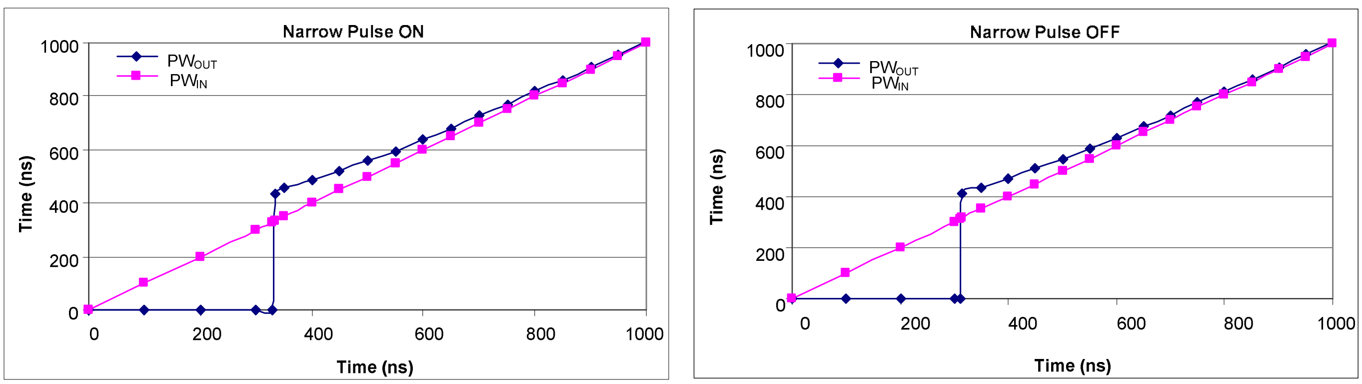

Figure 11: IRS2607D input filter characteristic

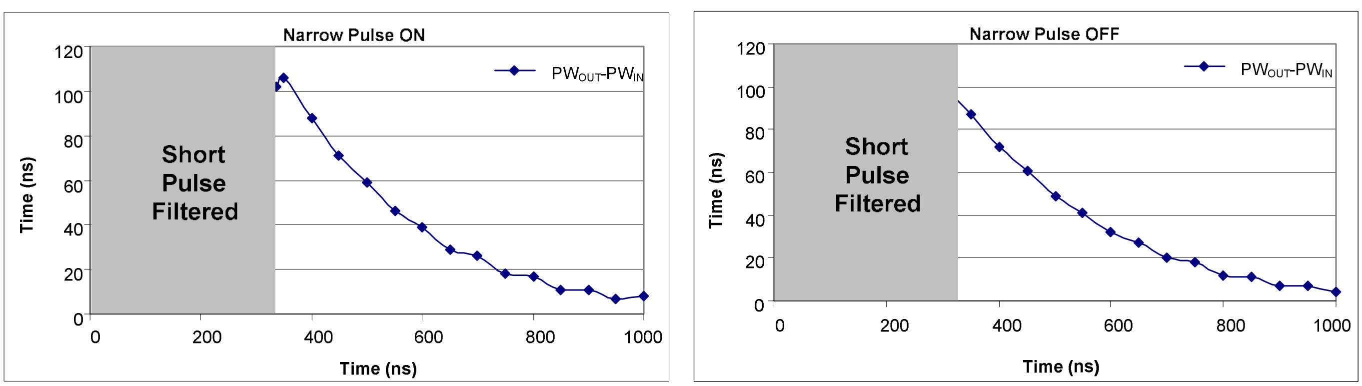

Figure 12: Difference between the input pulse and the output pulse

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Integrated Bootstrap Functionality

The IRS2607D embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.
A bootstrap FET is connected between the floating supply V_B and V_{CC} (see Fig. 13).

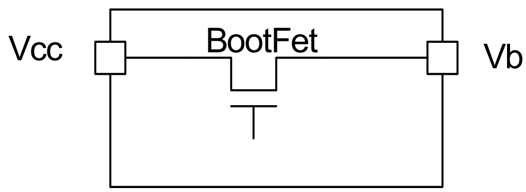

Figure 13: Semplified BootFET connection

The bootstrap FET is suitable for most PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode+ resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- When the motor runs at a very low current (so that the negative phase voltage decay can be longer than 20us) and complementary PWM is not used.
- At a very high PWM duty cycle due to the bootstrap FET equivalent resistance (R_{BS}, see page 3).

The summary for the bootstrap state follows:

- **Bootstrap turns-off (immediately) or stays off when at least one of the following conditions are met***:*
  1- HO goes/is high
  2- V_B goes/is high (> 1.1*V_{CC})
- ***Bootstrap turns-on when***:
  1- LO is high (low side is on) **AND** V_B is low (< ~1.1(V_{CC}))
  2- LO and HO are low after a LIN transition from H to L (HB output is in tri-state) **AND** V_B goes low (<1.1*V_{CC}) before a fixed time of 20us.
  3- LO and HO are low after a HIN transition from H to L (HB output is in tri-state) **AND** V_B goes low (<1.1(V_{CC})) before a retriggerable time of 20us. In this case the time counter is kept in reset state until VB goes high (>1.1V_{CC}). Please refer to the BootFET timing diagram for more details.

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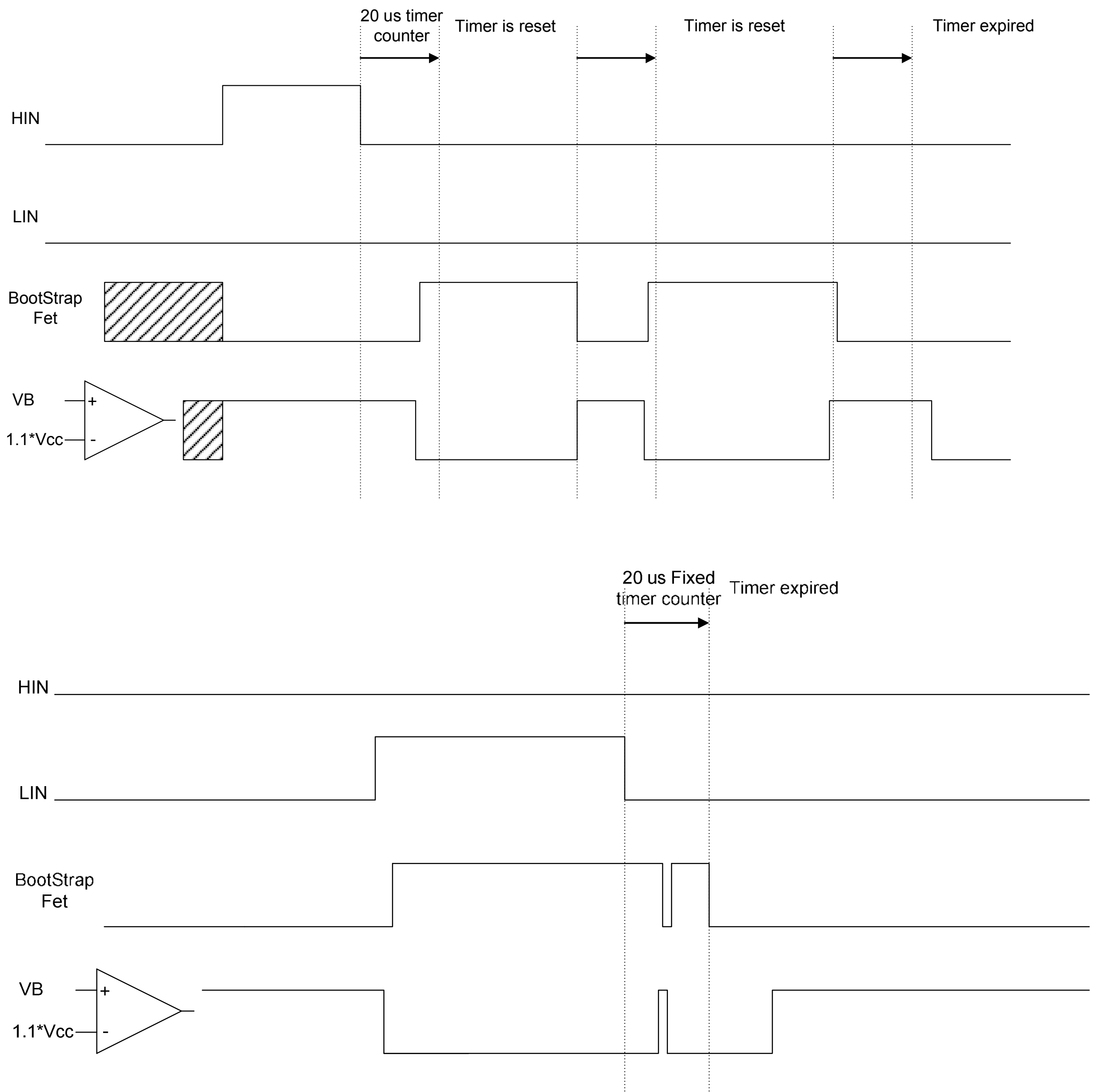

Figure 14: BootFET timing diagram

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Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 15; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 16 and 17) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

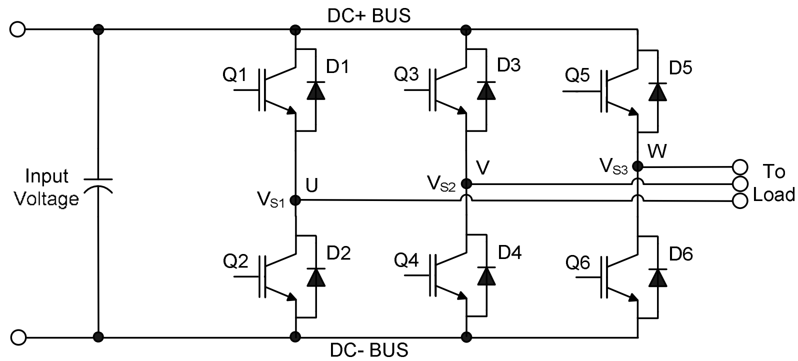

Figure 15: Three phase inverter

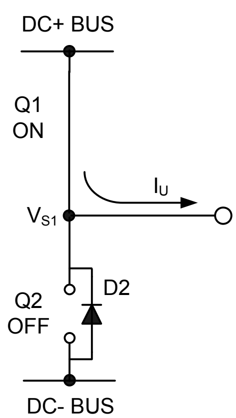

Figure 16: Q1 conducting

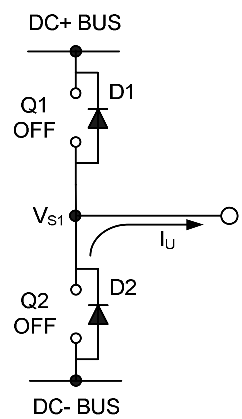

Figure 17: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 18 and 19), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

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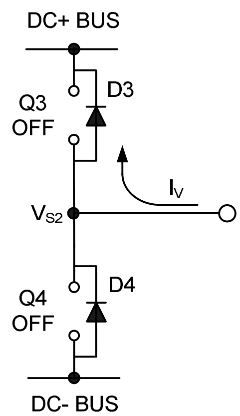


Figure 18: D3 conducting

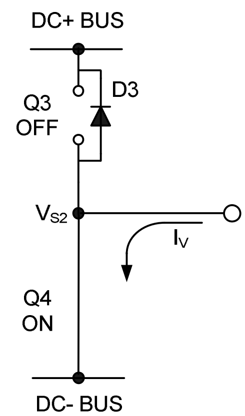


Figure 19: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”.

The circuit shown in Figure 20 depicts one leg of the three phase inverter; Figures 21 and 22 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

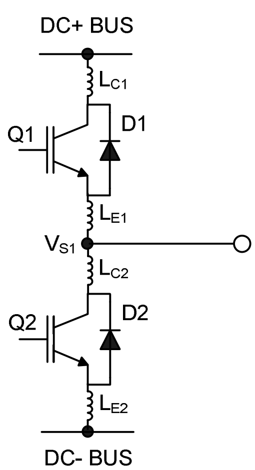


Figure 20: Parasitic Elements

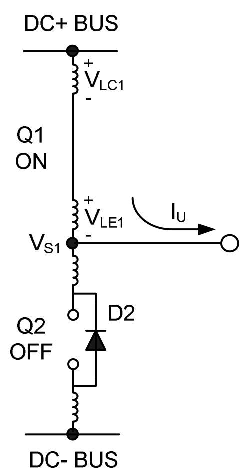


Figure 21: V_S positive

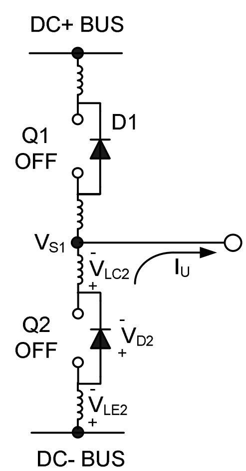


Figure 22: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the IRS2607D’s robustness can be seen in Figure 23, where there is represented the IRS2607D Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.
At V_{BS}=15V in case of -V_S transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5 μs.

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

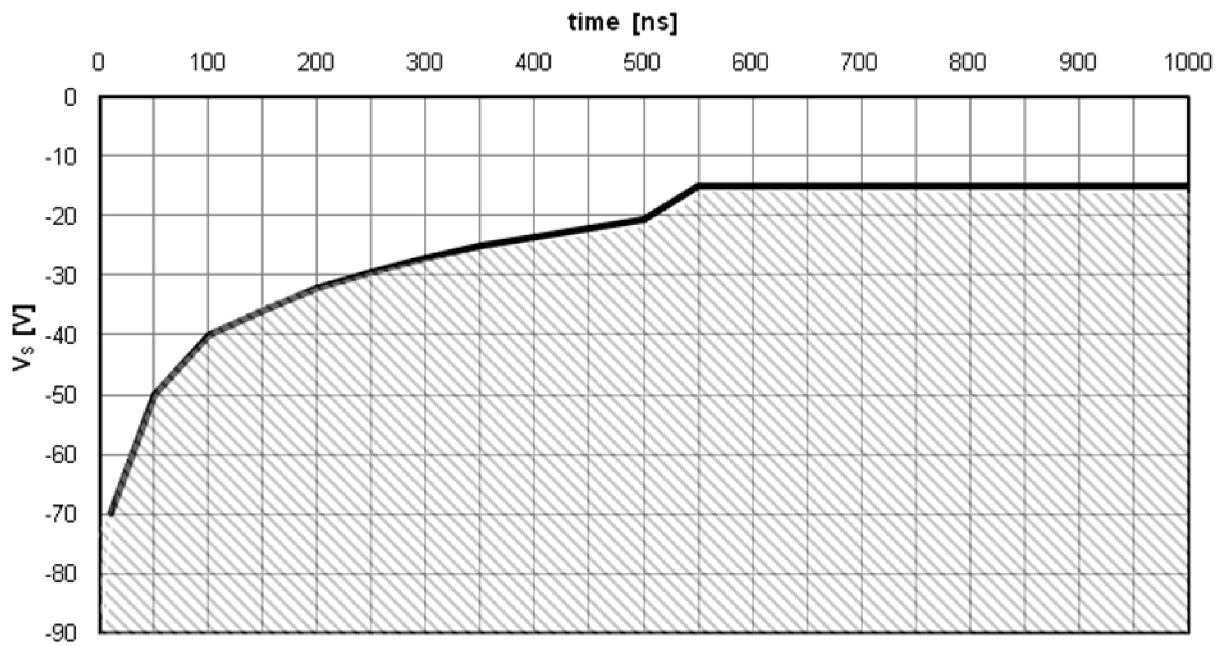


Figure 23: Negative V_S transient SOA for IRS2607D @ VBS=15V

Even though the IRS2607D has been shown able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 24). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

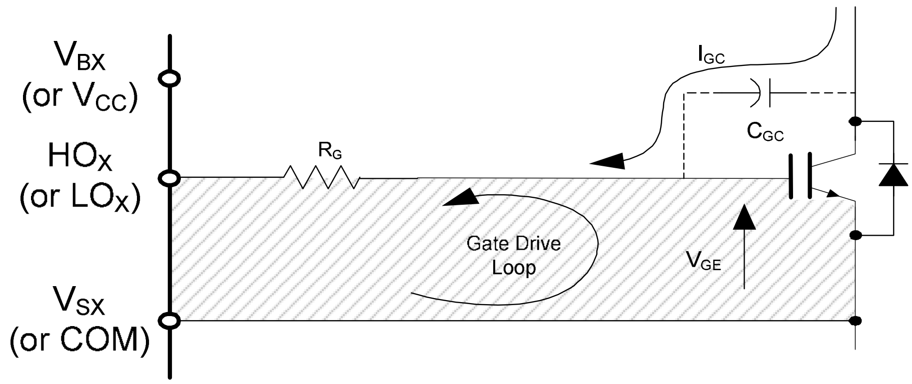


Figure 24: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 25), and in some cases using a clamping diode between COM and V_S (see Figure 26). See DT04-4 at www.irf.com for more detailed information.

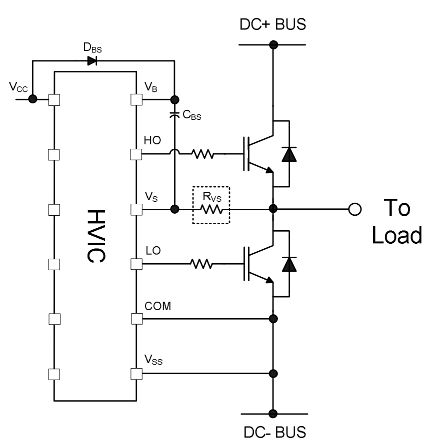


Figure 25: V_S resistor

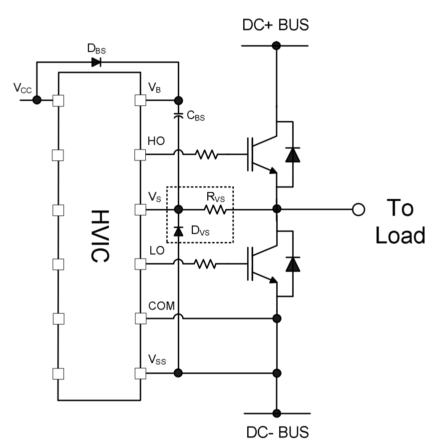


Figure 26: V_S clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.27 below, resulting in power loss and possible damage to the HVIC.

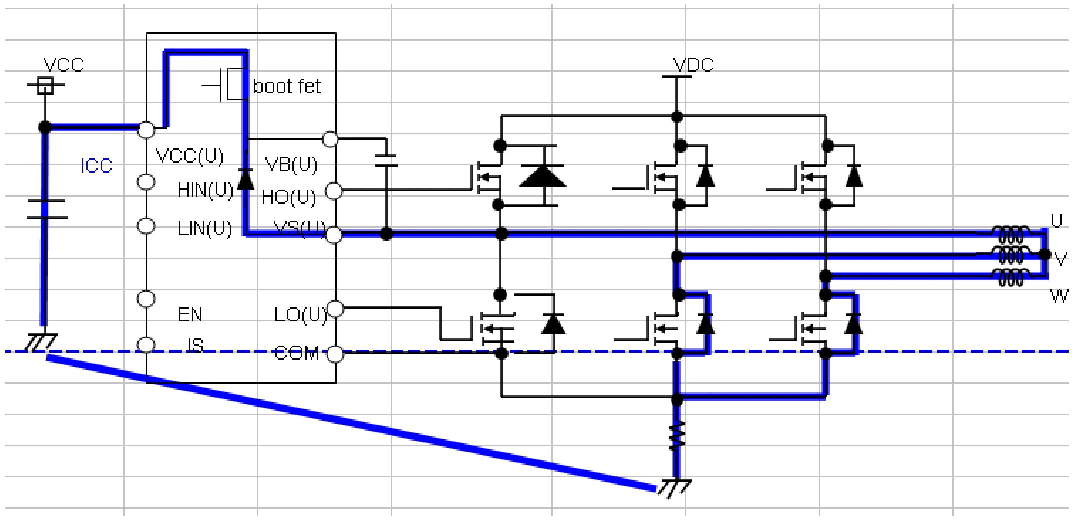


Figure 27: Current conduction path between VCC and VB pin

Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.28) prevents current conduction “out-of” VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

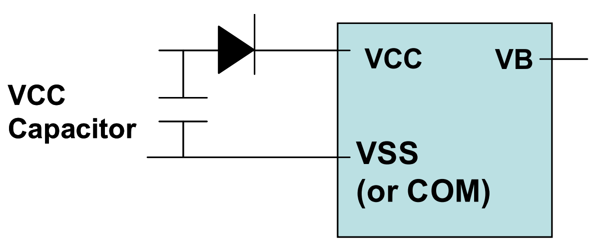


Figure 28: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage –* V_F *of Diode*.

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

Parameters trend in temperature

Figures 29-50 provide information on the experimental performance of the IRS2607DS HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

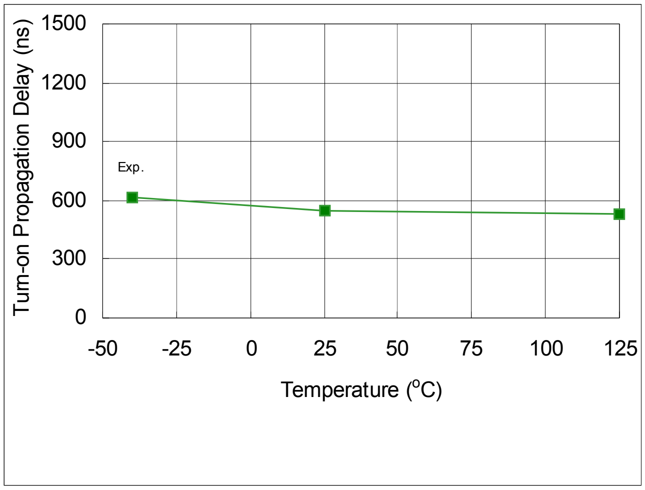


Fig. 29. Turn-on Propagation Delay vs. Temperature

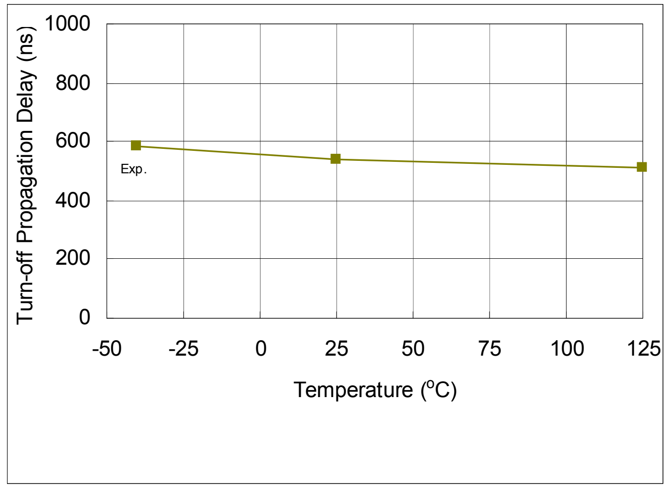


Fig. 30. Turn-off Propagation Delay vs. Temperature

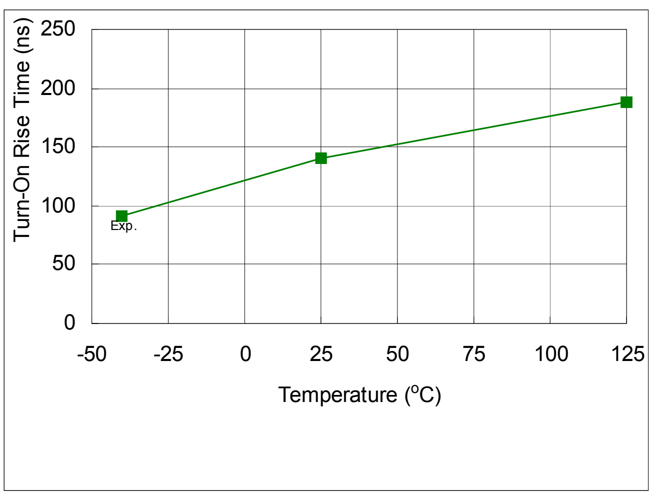


Fig. 31. Turn-on Rise Time vs. Temperature

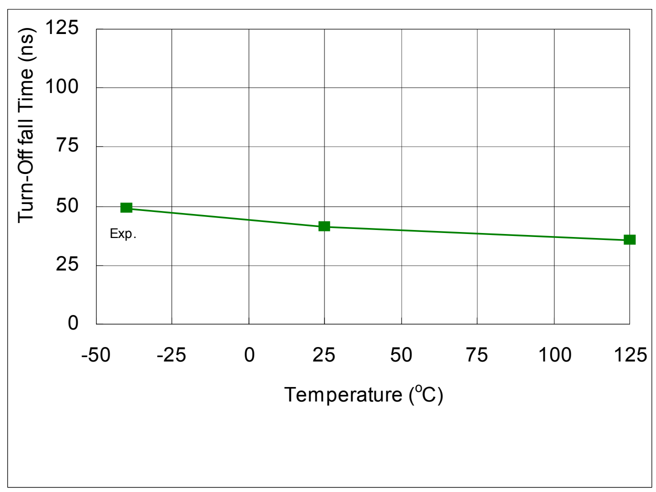


Fig. 32. Turn-off Rise Time vs. Temperature

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

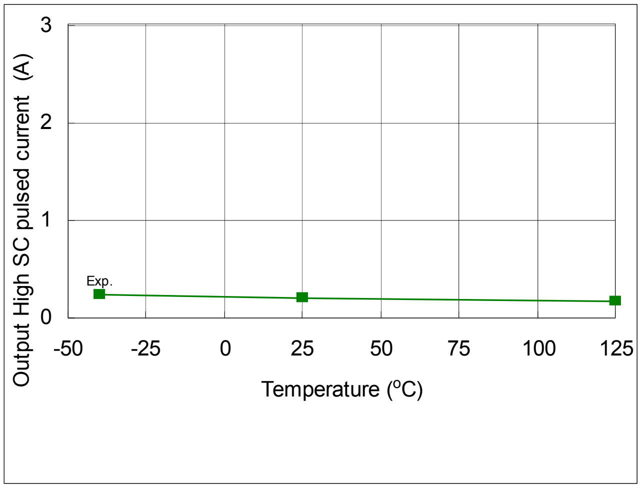


Fig. 33. Output High SC Pulsed Current vs. Temperature

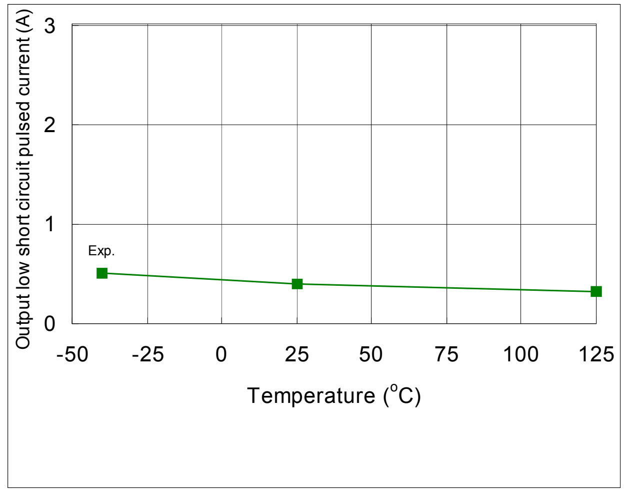


Fig. 34. Output Low Short Circuit Pulsed Current vs. Temperature

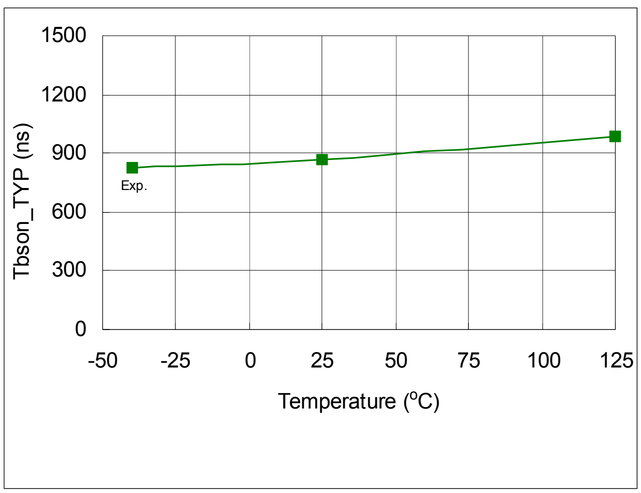


Fig. 35. Tbson_TYP vs. Temperature

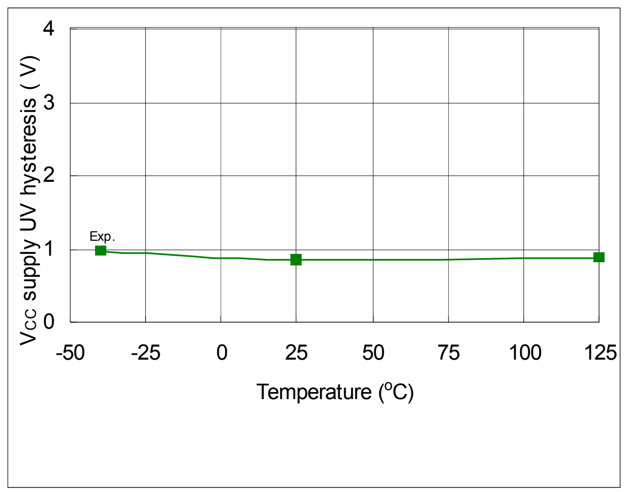


Fig. 36. V_{CC} Supply UV Hysteresis vs. Temperature

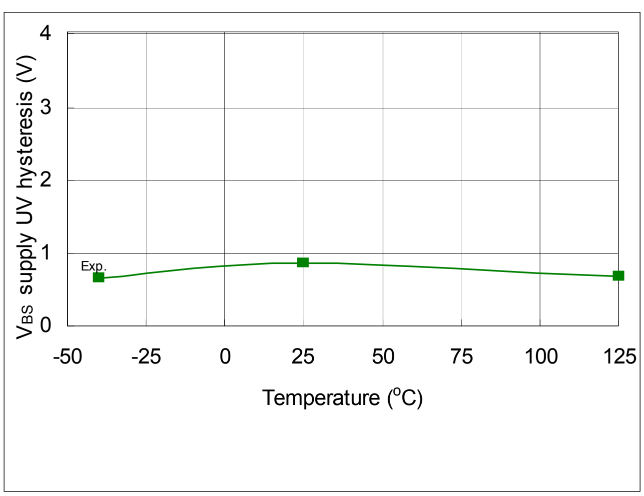


Fig. 37. V_{BS} Supply UV Hysteresis vs. Temperature

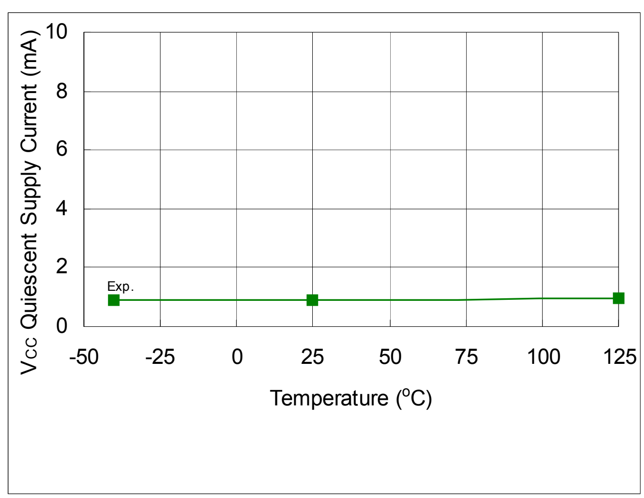


Fig. 38. V_{CC} Quiescent Supply Current vs. Temperature

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

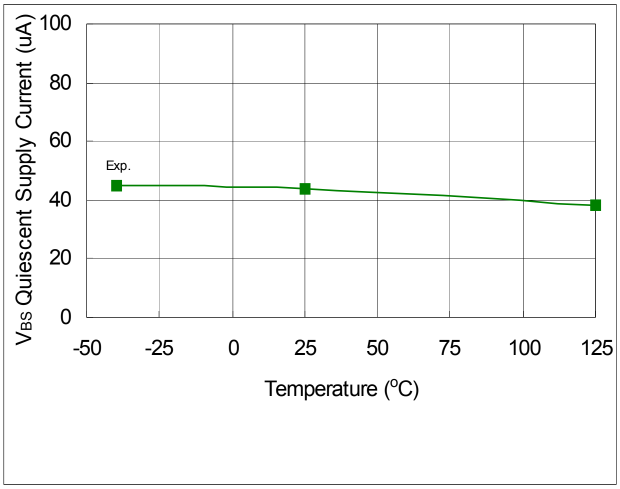


Fig. 39. V_{BS} Quiescent Supply Current vs. Temperature

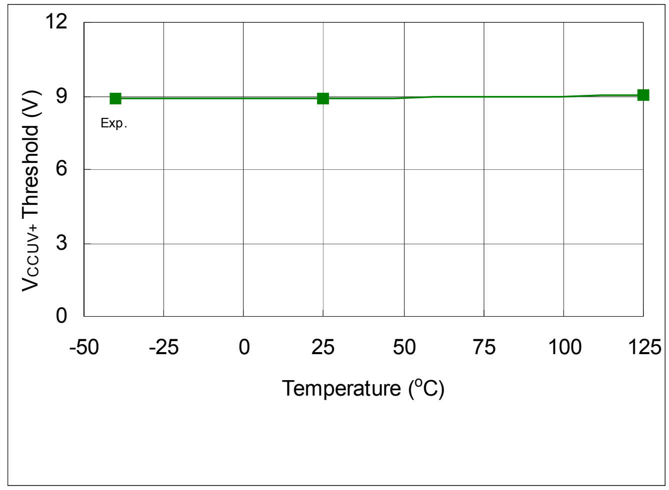


Fig. 40. V_{CCUV+} Threshold vs. Temperature

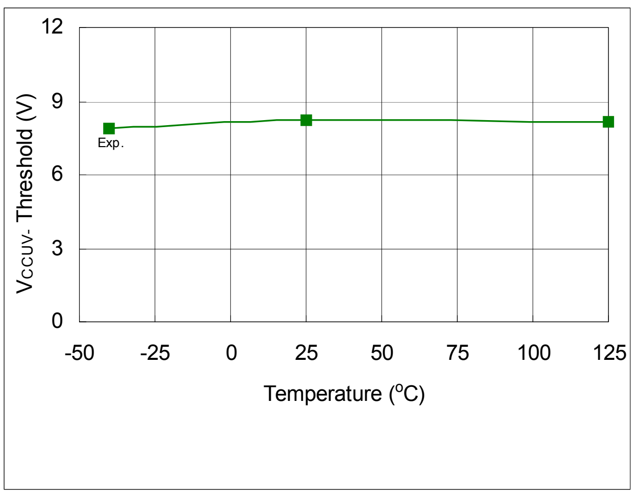


Fig. 41. V_{CCUV-} Threshold vs. Temperature

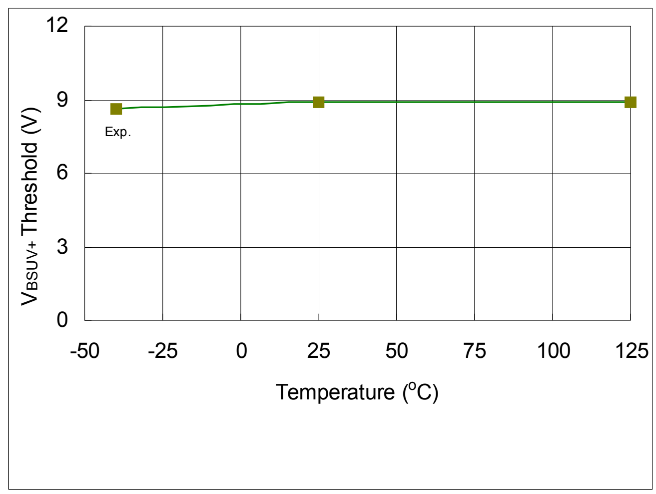


Fig. 42. V_{BSUV+} Threshold vs. Temperature

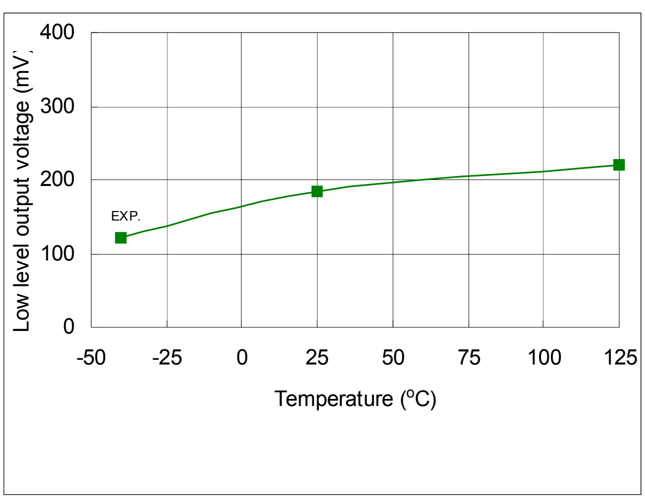


Fig. 43. Low Level Output Voltage vs. Temperature

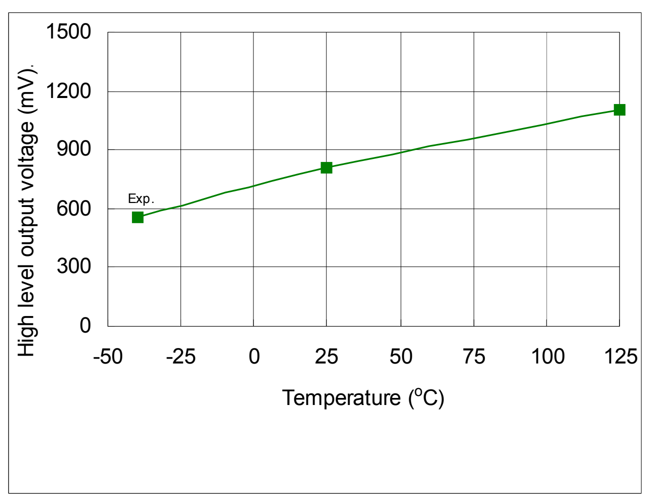


Fig. 44. High Level Output Voltage vs. Temperature

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

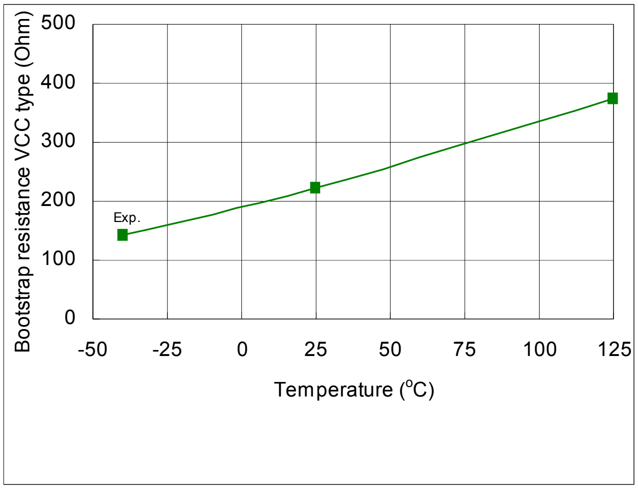


Fig. 45. Bootstrap Resistance VCC type vs. Temperature

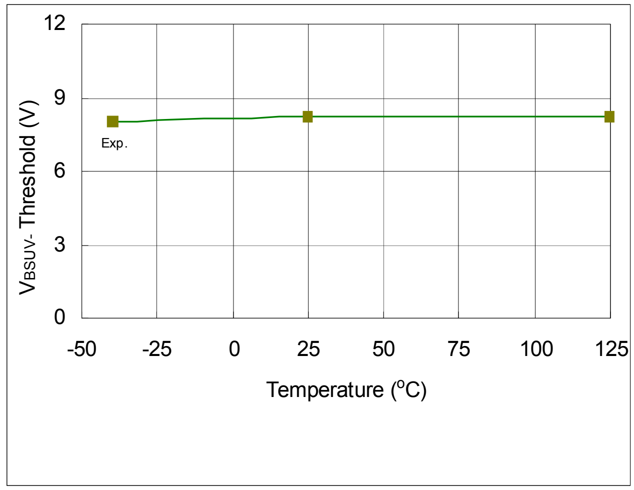


Fig. 46. V_{BSUV-} Threshold vs. Temperature

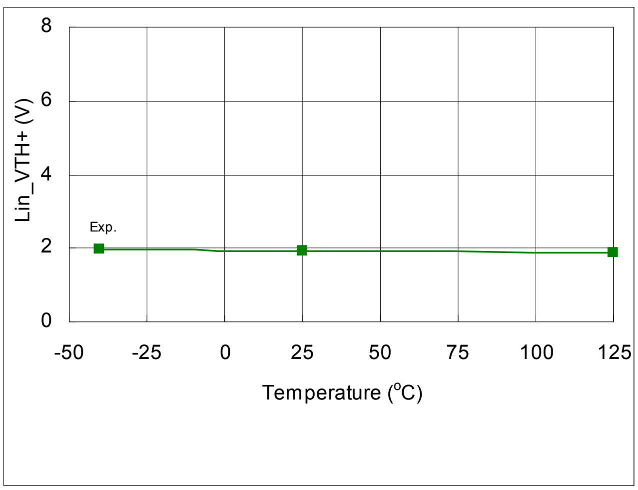


Fig. 47. Lin_VTH+ vs. Temperature

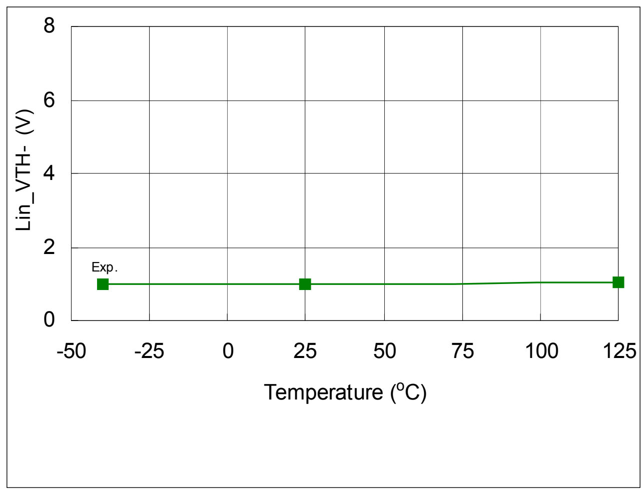


Fig. 48. Lin_VTH- vs. Temperature

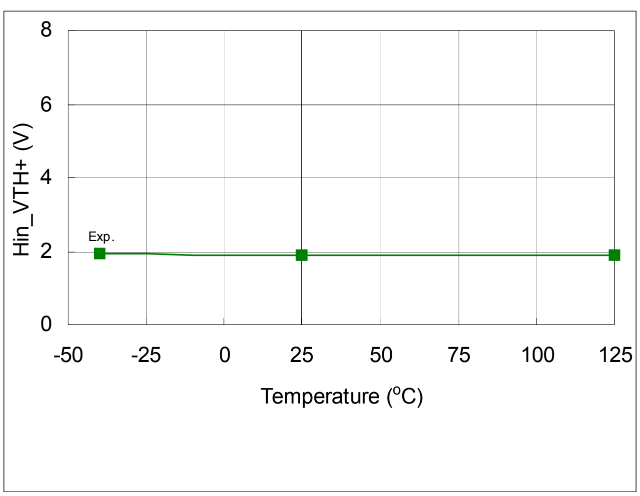


Fig. 49. Hin_VTH+ vs. Temperature

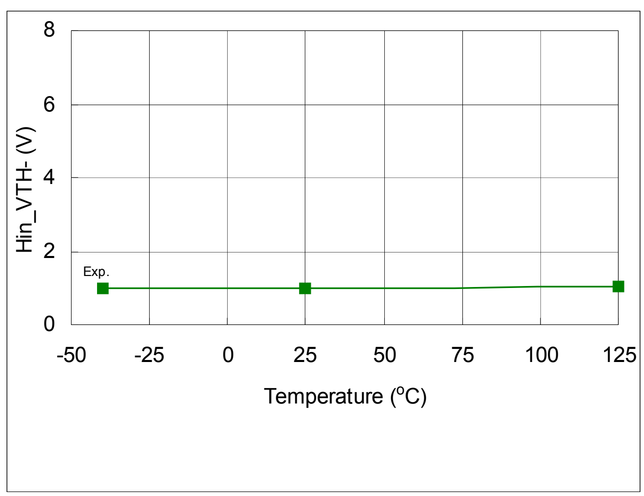
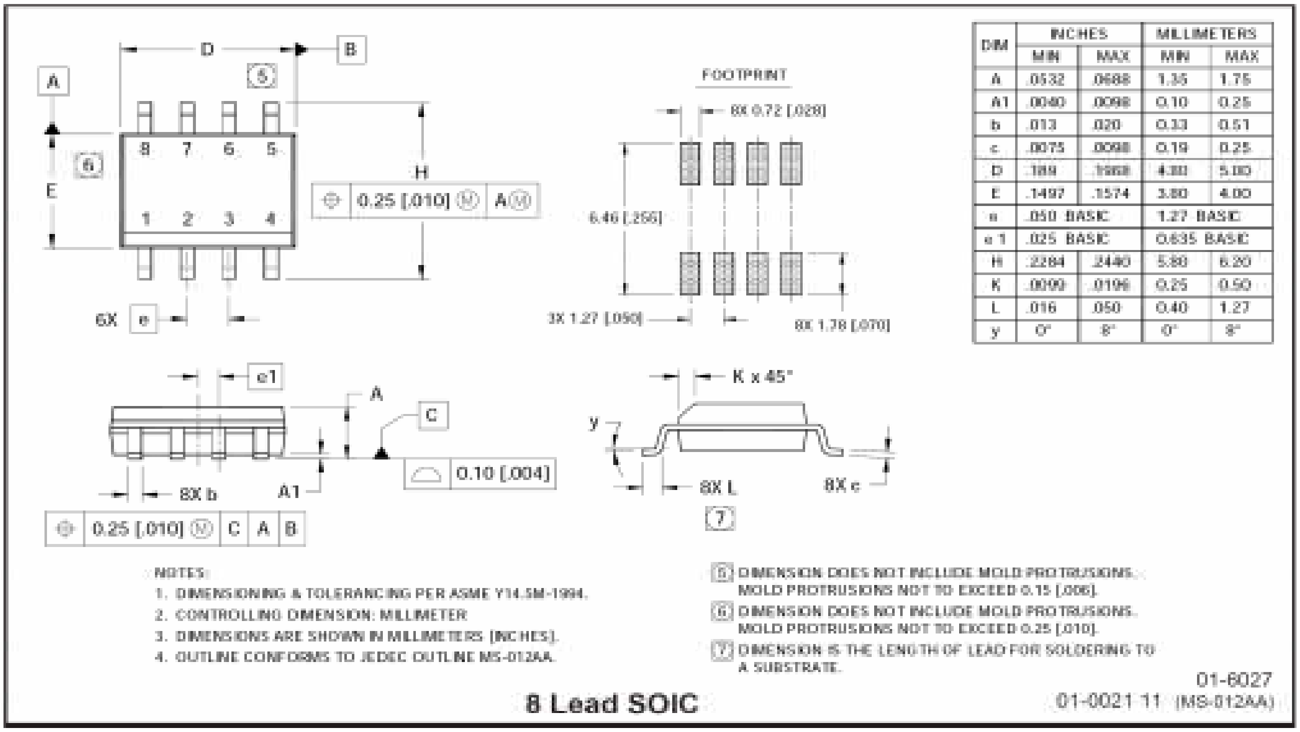


Fig. 50. Hin_VTH- vs. Temperature

Not recommended for new designs. For new designs, we recommend 2EDL05N06PF

Case Outlines



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

8 Lead SOIC