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## HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600 V  
Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V and 15 V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Internal 530 ns dead-time
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels
- Integrated bootstrap diode
- RoHS compliant

### Packages



### Product Summary

$V_{\text{OFFSET}}$	600 V max.
$I_{\text{O}+/-}$	120 mA / 250 mA
$V_{\text{OUT}}$	10 V – 20 V
$t_{\text{on/off (typ.)}}$	750 ns & 200 ns
Dead Time	530 ns

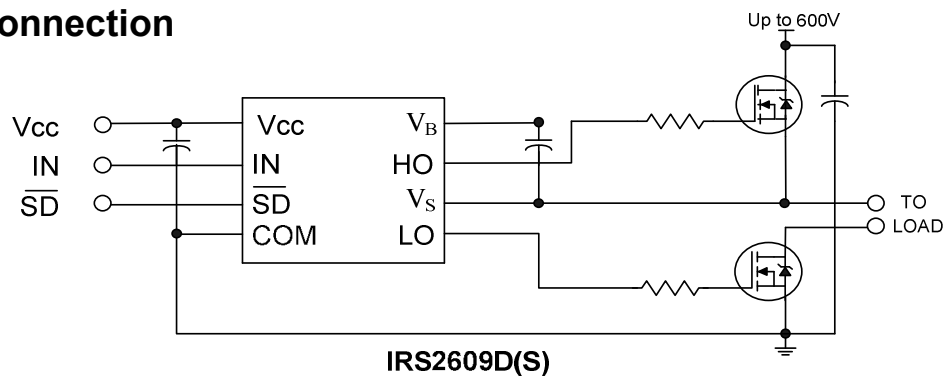
### Description

The IRS2609D is a high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with Standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

### Applications:

- \*Air Conditioner
- \*Micro/Mini Inverter Drives
- \*General Purpose Inverters
- \*Motor Control

### Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>††</sup>	
	Comments: This IC has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>	MSL2, 260°C (per IPC/JEDEC J-STD-020)	
<b>ESD</b>	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)
<b>IC Latch-Up Test</b>	Class I, Level A (per JESD78)	
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating absolute voltage	-0.3	620	V
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 20	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	20	
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage (IN & SD)	COM - 0.3	V <sub>CC</sub> + 0.3	
COM	Logic ground	V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns
P <sub>D</sub>	Package power dissipation @ TA ≤ +25 °C	—	0.625	W
Rth <sub>JA</sub>	Thermal resistance, junction to ambient	—	200	°C/W
T <sub>J</sub>	Junction temperature	—	150	°C
T <sub>S</sub>	Storage temperature	-50	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and COM offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	Static High side floating supply offset voltage	COM - 8 (Note 1)	600	
V <sub>St</sub>	Transient High side floating supply offset voltage	-50 (Note 2)	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (IN & SD)	V <sub>SS</sub>	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

**Note 1:** Logic operational for V<sub>S</sub> of -8 V to +600 V. Logic state held for V<sub>S</sub> of -8 V to -V<sub>BS</sub>.

**Note 2:** Operational for transient negative V<sub>S</sub> of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V, COM =  $V_{CC}$ ,  $C_L$  = 1000 pF,  $T_A$  = 25 °C, DT =  $V_{SS}$  unless otherwise specified.

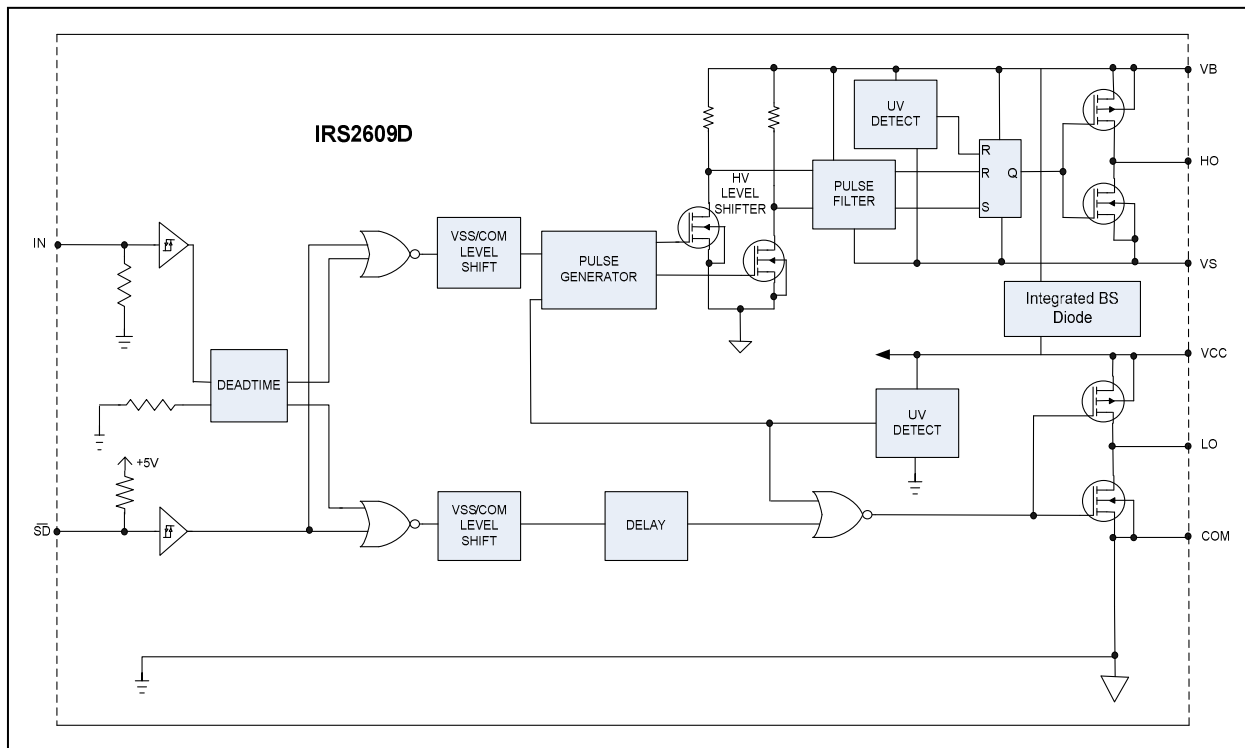
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	750	1100	ns	$V_S = 0$ V or 600 V
$t_{off}$	Turn-off propagation delay	—	250	400		$V_S = 0$ V or 600 V
$t_{sd}$	Shut-down propagation delay	—	250	400		
MT	Delay matching, HS & LS turn-on/off	—	—	60		
$t_r$	Turn-on rise time	—	150	220		$V_S = 0$ V
$t_f$	Turn-off fall time	—	50	80		$V_S = 0$ V
DT	Deadtime: LO turn-off to HO turn-on( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ )	350	530	800		$V_{IN} = 0$ V & 5 V Without external deadtime
MT	Delay matching time ( $t_{ON}$ , $t_{OFF}$ )	—	—	60		
MDT	Deadtime matching = $DT_{LO-HO} - DT_{HO-LO}$	—	—	60		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $V_{CC}$  = COM, DT =  $V_{CC}$  and  $T_A$  = 25 °C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to  $V_{CC}/COM$  and are applicable to the respective input leads: IN and  $\overline{SD}$ . The  $V_O$ ,  $I_O$  and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{IH}$	logic "1" input voltage for HO & logic "0" for LO	2.2	—	—	V	
$V_{IL}$	logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
$V_{OL}$	Low level output voltage, $V_O$	—	0.3	0.6		$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 600$ V
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	45	70		$V_{IN} = 0$ V or 4 V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	1000	2000	3000		$V_{IN} = 0$ V or 4 V
$I_{IN+}$	Logic "1" input bias current	—	5	20		$V_{IN} = 4$ V
$I_{IN-}$	Logic "0" input bias current	—	—	2		$V_{IN} = 0$ V
$I_{SD, TH+}$	$\overline{SD}$ input positive going threshold	—	15	30		
$I_{SD, TH-}$	$\overline{SD}$ input negative going threshold	—	10	20		
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going Threshold	8.0	8.9	9.8		V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going Threshold	7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	—	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0$ V, $PW \leq 10$ $\mu$ s
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15$ V, $PW \leq 10$ $\mu$ s
Rbs	Bootstrap resistance	—	200	—	Ohm	

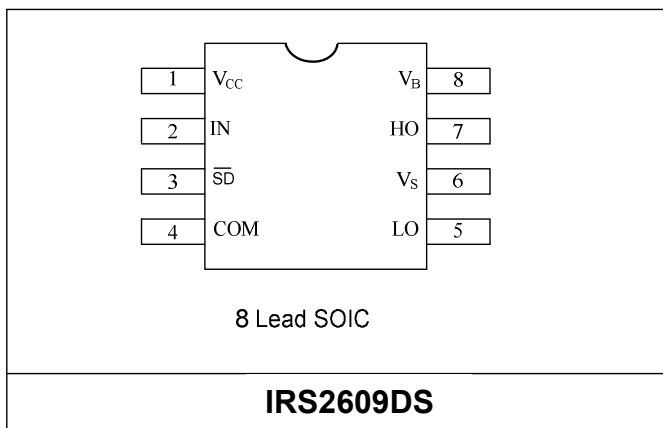
### Functional Block Diagrams



### Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase
$\overline{SD}$	Logic input for shutdown
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

### Lead Assignments



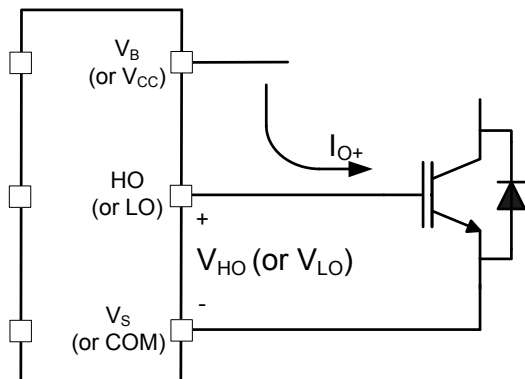
## Application Information and Additional Details

Informations regarding the following topics are included as subsections within this section of the datasheet.

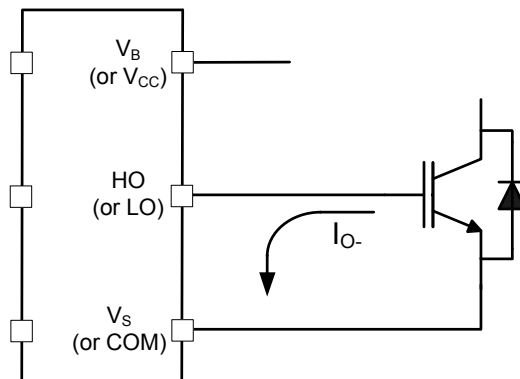
- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Shut down Input
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Integrated Bootstrap Functionality
- Negative  $V_S$  Transient SOA
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

### IGBT/MOSFET Gate Drive

The IRS2609D HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as  $I_O$ . The voltage that drives the gate of the external power switch is defined as  $V_{HO}$  for the high-side power switch and  $V_{LO}$  for the low-side power switch; this parameter is sometimes generically called  $V_{OUT}$  and in this case does not differentiate between the high-side or low-side output voltage.



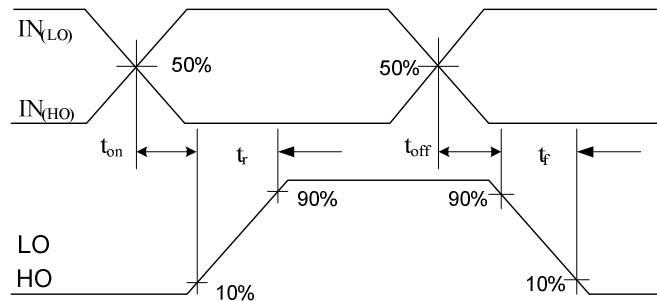
**Figure 1: HVIC sourcing current**



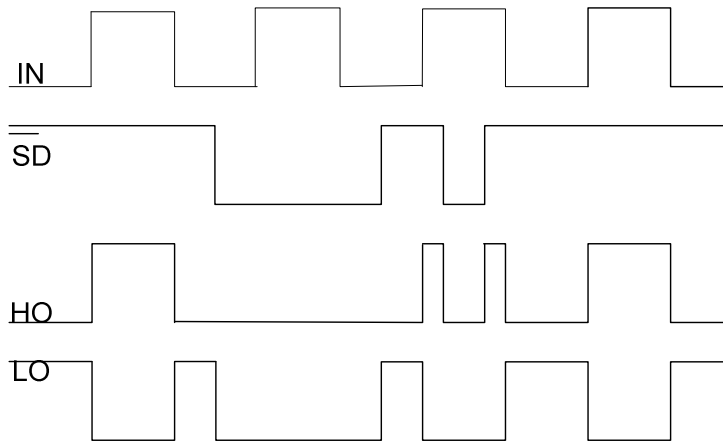
**Figure 2: HVIC sinking current**

**Switching and Timing Relationships**

The relationships between the input and output signals of the IRS2609D are illustrated below in Figures 3, 4. From these figures, we can see the definitions of several timing parameters (i.e.  $t_{ON}$ ,  $t_{OFF}$ ,  $t_R$ , and  $t_F$ ) associated with this device.



**Figure 3: Switching time waveforms**



**Figure 4: Input/output timing diagram**

**Deadtime**

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR’s HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 5 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS2609D is matched with respect to the high- and low-side outputs. Figure 6 defines the two deadtime parameters (i.e.,  $DT_{LO-HO}$  and  $DT_{HO-LO}$ ); the deadtime matching parameter (MDT) associated with the IRS2609D specifies the maximum difference between  $DT_{LO-HO}$  and  $DT_{HO-LO}$ .

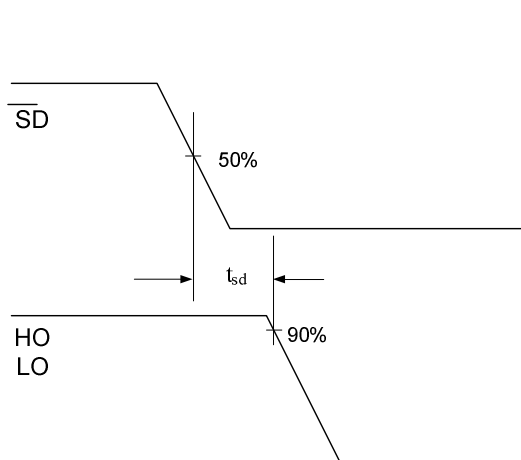
**Matched Propagation Delays**

The IRS2609D family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC’s response at the output to a signal at the input requires approximately the same time duration (i.e.,  $t_{ON}$ ,  $t_{OFF}$ ) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay ( $t_{ON}$ ) of the IRS2609D is matched to the propagation turn-off delay ( $t_{OFF}$ ).

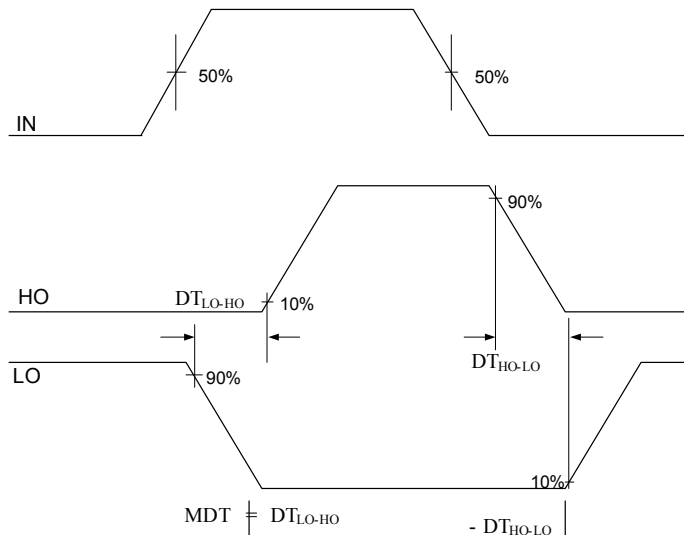


**Shut down Input**

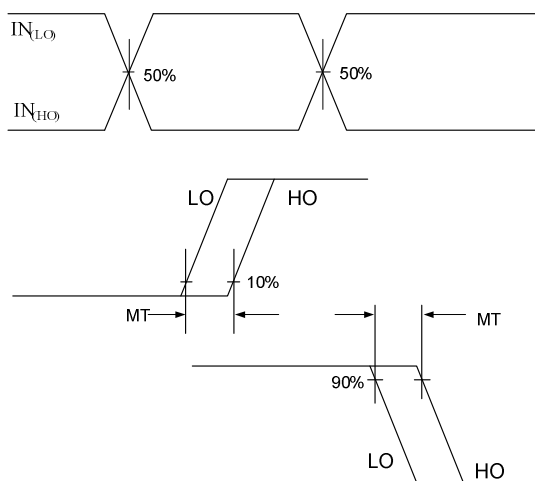
The IRS2609D family of HVICs is equipped with a shut down (/SD) input pin that is used to shutdown or enable the HVIC. When the /SD pin is in the high state the HVIC is able to operate normally. When the /SD pin is in low state the HVIC is tristated.



**Figure 5: Shut down**



**Figure 6: Dead time Definition**



**Figure 7: Delay Matching waveform Definition**

**Input Logic Compatibility**

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS2609D has been designed to be compatible with 3.3 V and 5 V logic-level signals. The IRS2609D features an integrated 5.2 V Zener clamp on the /SD. Figure 8 illustrates an input signal to the IRS2609D, its input threshold values, and the logic state of the IC as a result of the input signal.

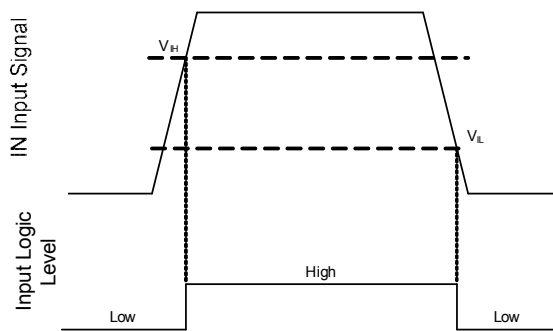


Figure 8: HIN & LIN input thresholds

### Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the  $V_{CC}$  (logic and low-side circuitry) power supply and the  $V_{BS}$  (high-side circuitry) power supply. Figure 9 is used to illustrate this concept;  $V_{CC}$  (or  $V_{BS}$ ) is plotted over time and as the waveform crosses the UVLO threshold ( $V_{CCUV+/-}$  or  $V_{BSUV+/-}$ ) the undervoltage protection is enabled or disabled.

Upon power-up, should the  $V_{CC}$  voltage fail to reach the  $V_{CCUV+}$  threshold, the IC will not turn-on. Additionally, if the  $V_{CC}$  voltage decreases below the  $V_{CCUV-}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the  $V_{BS}$  voltage fail to reach the  $V_{BSUV}$  threshold, the IC will not turn-on. Additionally, if the  $V_{BS}$  voltage decreases below the  $V_{BSUV}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

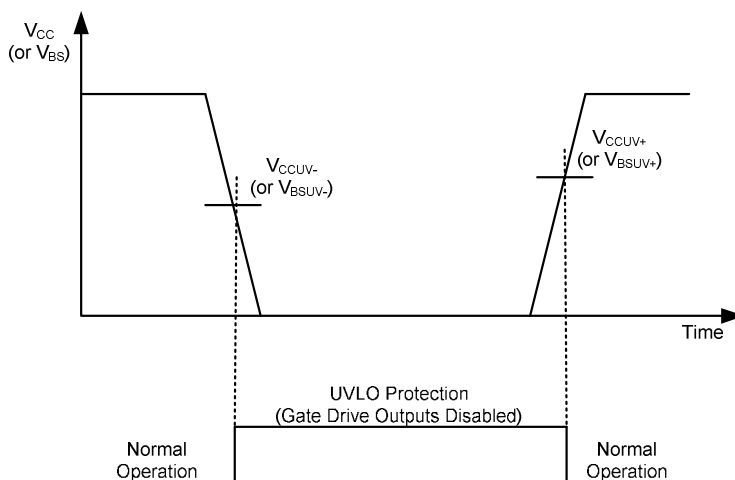


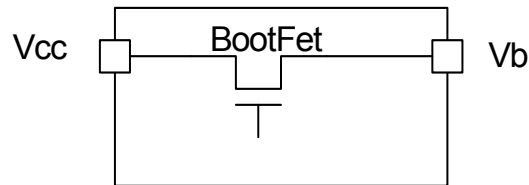
Figure 9: UVLO protection

### Shoot-Through Protection

The IRS2609D high-voltage ICs is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry).

**Integrated Bootstrap Functionality**

The IRS2609D embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications. A bootstrap FET is connected between the floating supply  $V_B$  and  $V_{CC}$  (see Fig. 10).

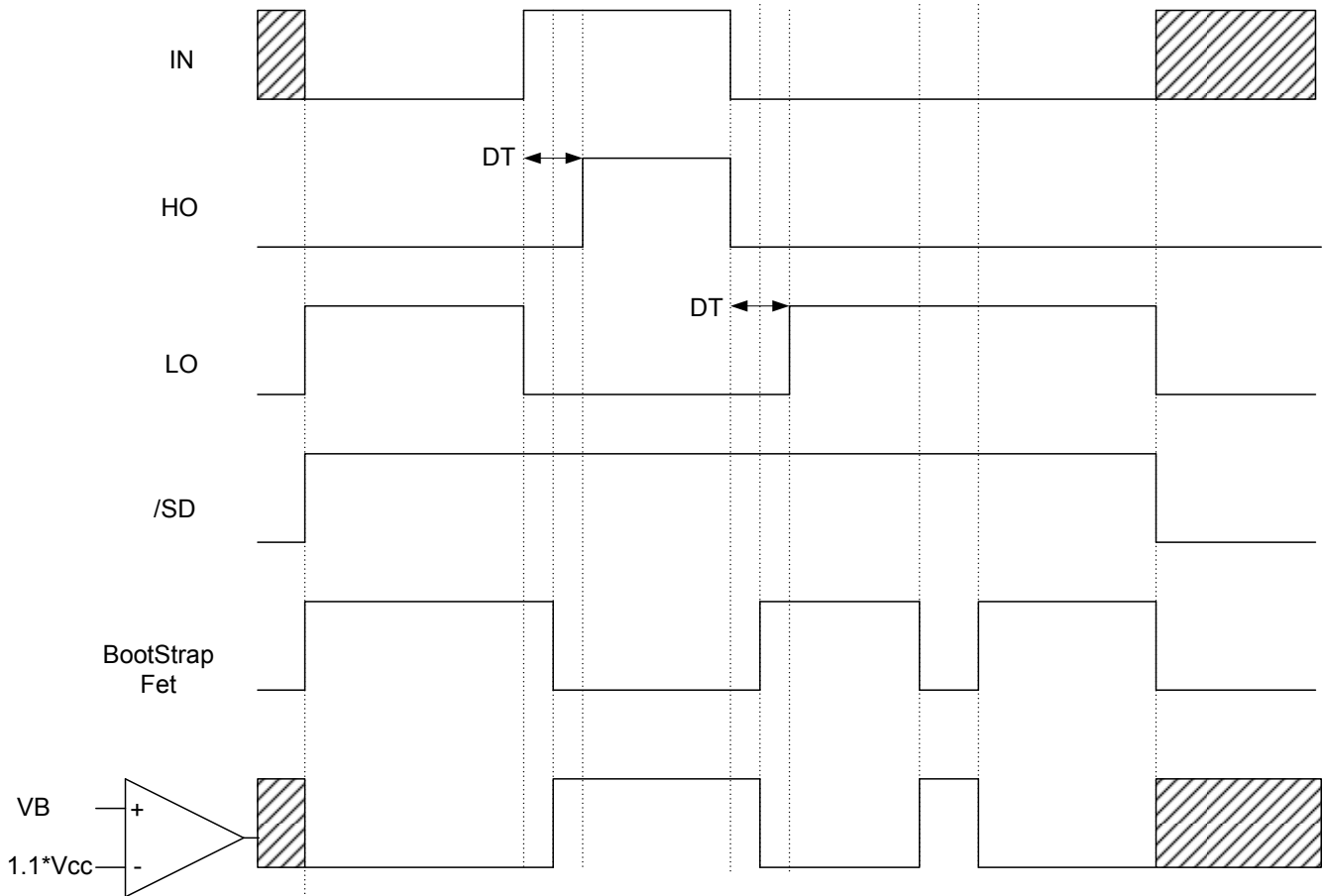


**Figure 10: Simplified BootFET connection**

The integrated bootstrap feature can be used either in parallel with the external bootstrap network (diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations at very high PWM duty cycle, corresponding to very short LIN pulses, due to the bootstrap FET equivalent resistance RBS.

The summary for the bootstrap state follows:

- **Bootstrap turns-off (immediately) or stays off when at least one of the following conditions are met:**
  - 1- /SD is low
  - 2- /SD is high, IN is low and  $V_B$  is high ( $> 1.1 \cdot V_{CC}$ )
  - 3- /SD is high, IN is high (DT period excluded)
  - 4- /SD is high, IN is high and  $V_B$  is high ( $> 1.1 \cdot V_{CC}$ ) (during DT period)
- **Bootstrap turns-on when:**
  - 1- /SD in high, IN is low and  $V_B$  is low ( $< 1.1(V_{CC})$ )
  - 2- /SD in high, IN is high and  $V_B$  is low ( $< 1.1(V_{CC})$ ) (during the DT period). Please refer to the BootFET timing diagram for more details.

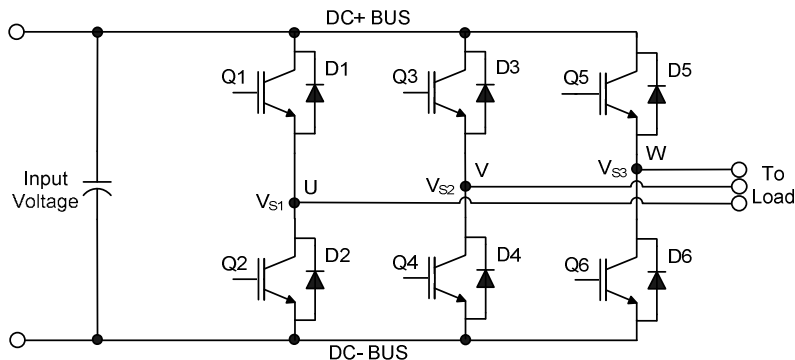


**Figure 11: BootFET timing diagram**

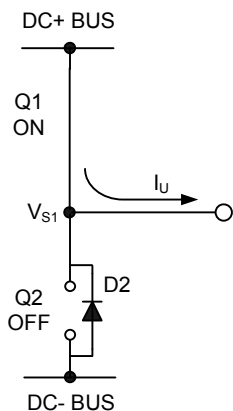
**Negative  $V_s$  Transient SOA**

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 12; here we define the power switches and diodes of the inverter.

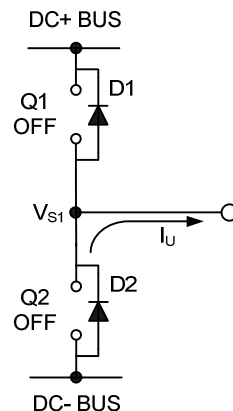
If the high-side switch (e.g., the IGBT Q1 in Figures 13 and 14) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node  $V_{s1}$ , swings from the positive DC bus voltage to the negative DC bus voltage.



**Figure 12: Three phase inverter**

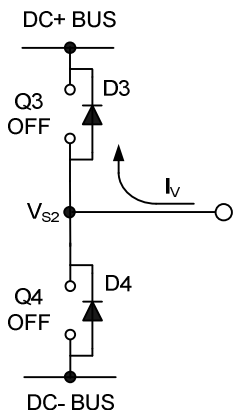


**Figure 13: Q1 conducting**

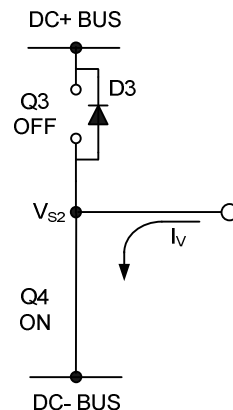


**Figure 14: D2 conducting**

Also when the V phase current flows from the inductive load back to the inverter (see Figures 15 and 16), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node,  $V_{s2}$ , swings from the positive DC bus voltage to the negative DC bus voltage.



**Figure 15: D3 conducting**



**Figure 16: Q4 conducting**

However, in a real inverter circuit, the  $V_S$  voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative  $V_S$  transient”.

The circuit shown in Figure 17 depicts one leg of the three phase inverter; Figures 18 and 19 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in  $L_C$  and  $L_E$  for each IGBT. When the high-side switch is on,  $V_{S1}$  is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to  $V_{S1}$  (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between  $V_{S1}$  and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the  $V_S$  pin).

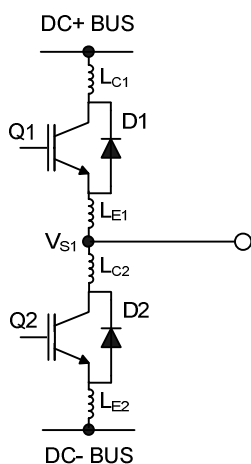


Figure 17: Parasitic Elements

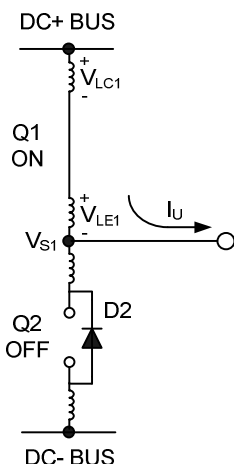


Figure 18:  $V_S$  positive

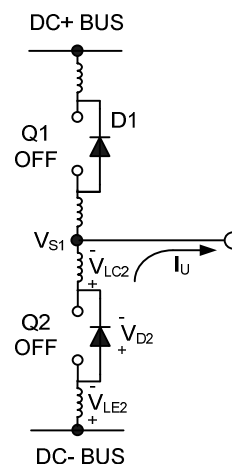


Figure 19:  $V_S$  negative

In a typical motor drive system,  $dV/dt$  is typically designed to be in the range of 3-5 V/ns. The negative  $V_S$  transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when  $di/dt$  is greater than in normal operation.

International Rectifier’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the IRS2609D’s robustness can be seen in Figure 20, where there is represented the IRS2609D Safe Operating Area at  $V_{BS}=15V$  based on repetitive negative  $V_S$  spikes. A negative  $V_S$  transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative  $V_S$  transients fall inside SOA.

At  $V_{BS}=15V$  in case of  $-V_S$  transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5  $\mu s$ .

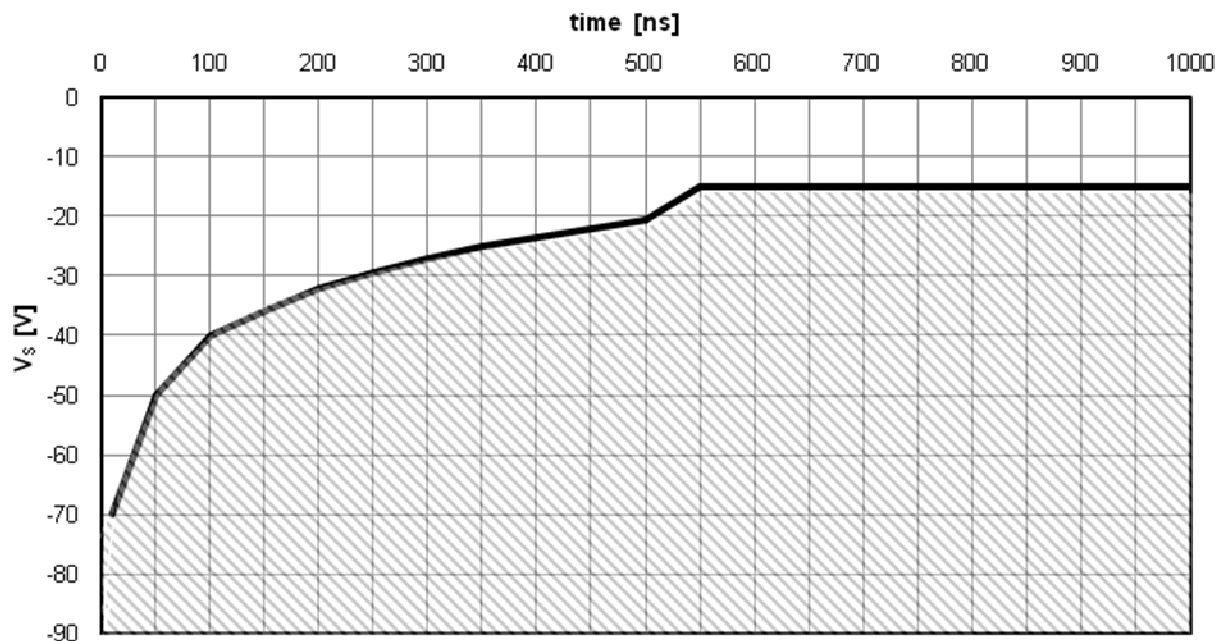


Figure 20: Negative V<sub>S</sub> transient SOA for IRS2608D @ V<sub>BS</sub>=15V

Even though the IRS2609D has been shown able to handle these large negative V<sub>S</sub> transient conditions, it is highly recommended that the circuit designer always limit the negative V<sub>S</sub> transients as much as possible by careful PCB layout and component use.

**PCB Layout Tips**

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V<sub>B</sub> and V<sub>S</sub>) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 21). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

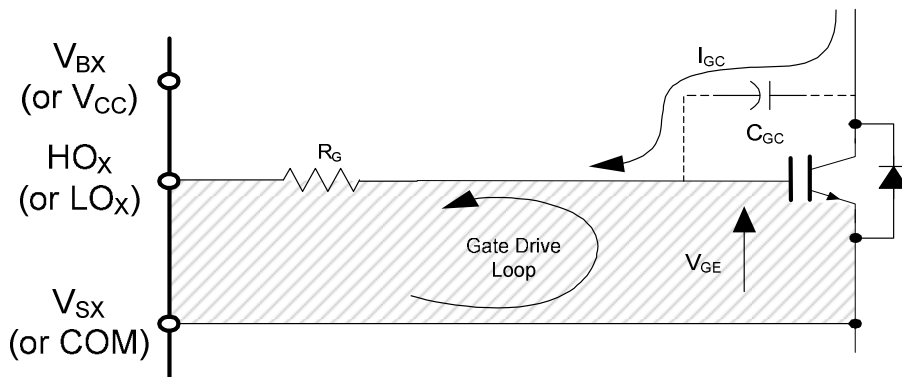
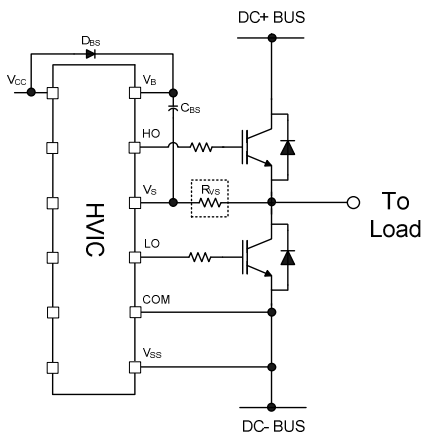


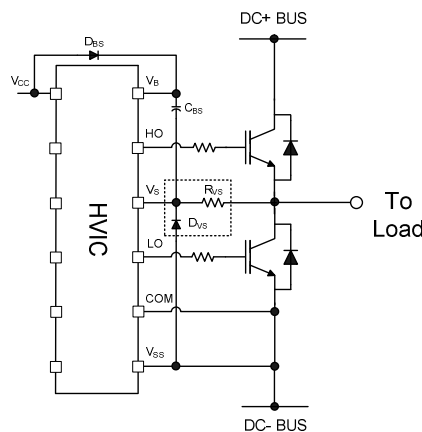
Figure 21: Antenna Loops

**Supply Capacitor:** It is recommended to place a bypass capacitor ( $C_{IN}$ ) between the  $V_{CC}$  and COM pins. A ceramic  $1\ \mu\text{F}$  ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

**Routing and Placement:** Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative  $V_S$  spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor ( $5\ \Omega$  or less) between the  $V_S$  pin and the switch node (see Figure 22), and in some cases using a clamping diode between COM and  $V_S$  (see Figure 23). See DT04-4 at [www.irf.com](http://www.irf.com) for more detailed information.



**Figure 22:  $V_S$  resistor**



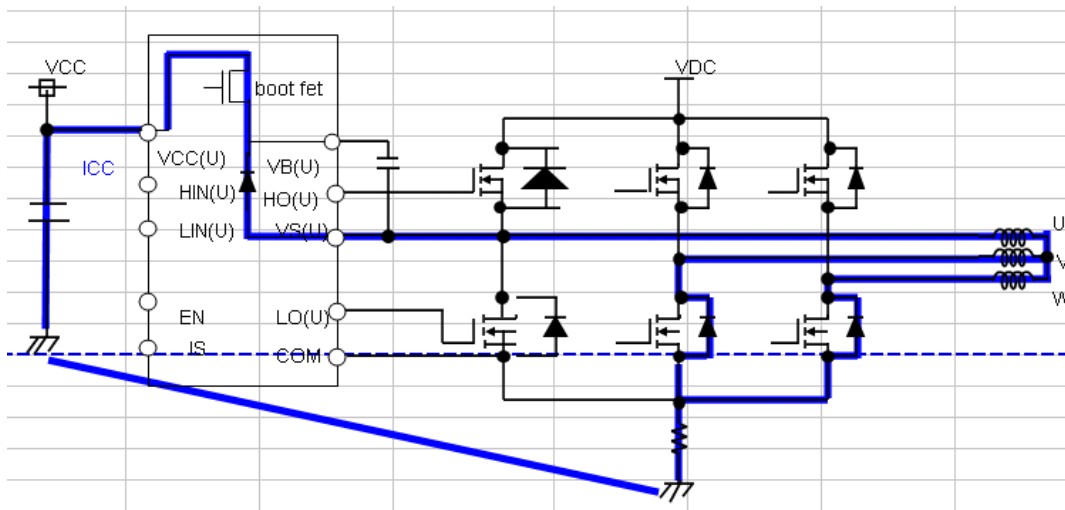
**Figure 23:  $V_S$  clamping diode**

**Integrated Bootstrap FET limitation**

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V**    **AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.24 below, resulting in power loss and possible damage to the HVIC.



**Figure 24: Current conduction path between VCC and VB pin**

Relevant Application Situations:

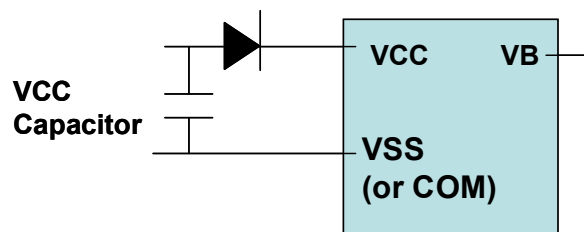


The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.25) prevents current conduction “out-of” VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.



**Figure 25: Diode insertion between VCC pin and VCC capacitor**

Note that the forward voltage drop on the diode ( $V_f$ ) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements.  $VCC\ pin\ Bias = VCC\ Supply\ Voltage - V_f\ of\ Diode$ .

**Additional Documentation**

Several technical documents related to the use of HVICs are available at [www.irf.com](http://www.irf.com); use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

- DT97-3: Managing Transients in Control IC Driven Power Stages
- AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
- DT04-4: Using Monolithic High Voltage Gate Drivers
- AN-978: HV Floating MOS-Gate Driver ICs

**Parameters trend in temperature**

Figures 26-49 provide information on the experimental performance of the IRS2609D(S) HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

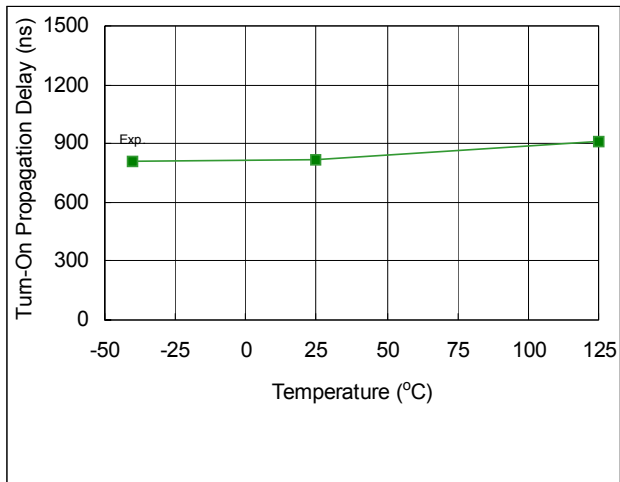


Fig. 26. Turn-on Propagation Delay vs. Temperature

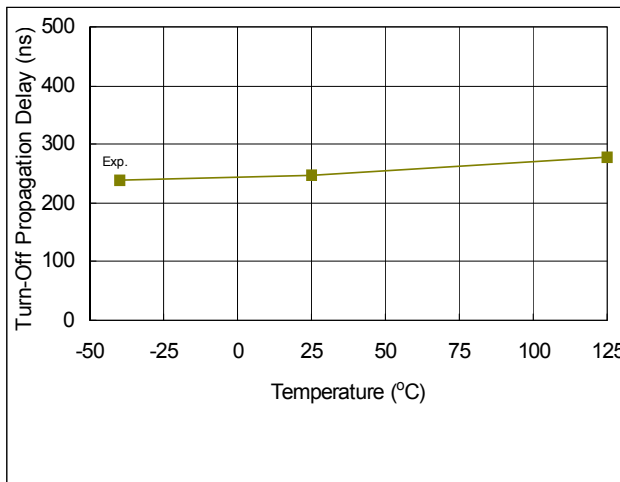


Fig. 27. Turn-off Propagation Delay vs. Temperature

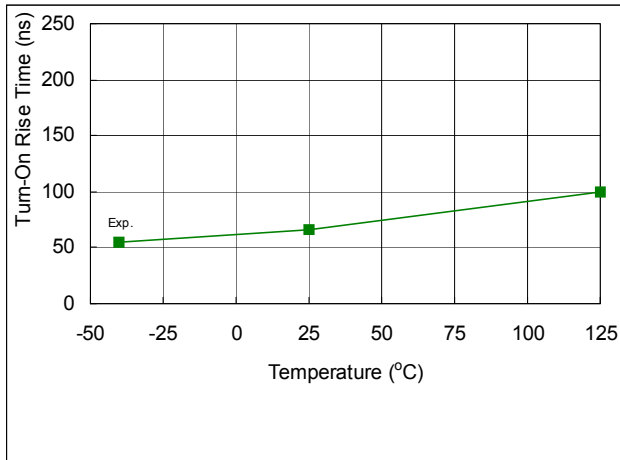


Fig. 28. Turn-on Rise Time vs. Temperature

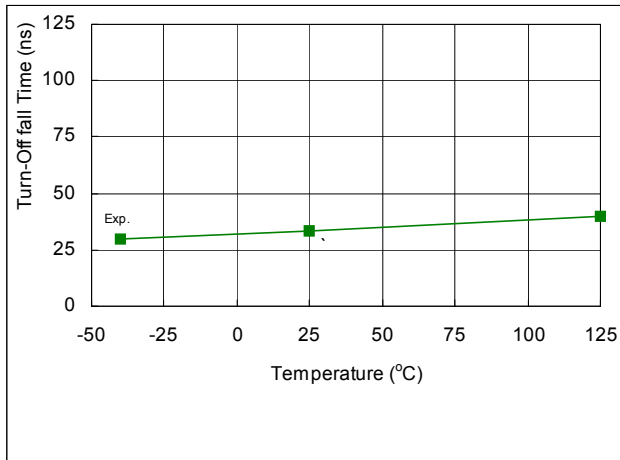


Fig. 29. Turn-off Rise Time vs. Temperature

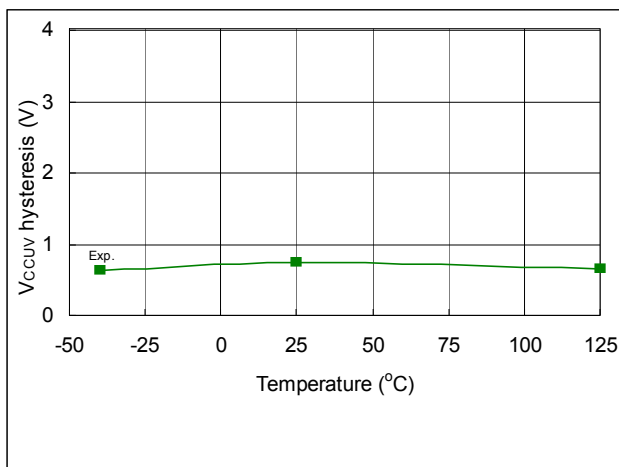


Fig. 30. V<sub>CC</sub> Supply UV Hysteresis vs. Temperature

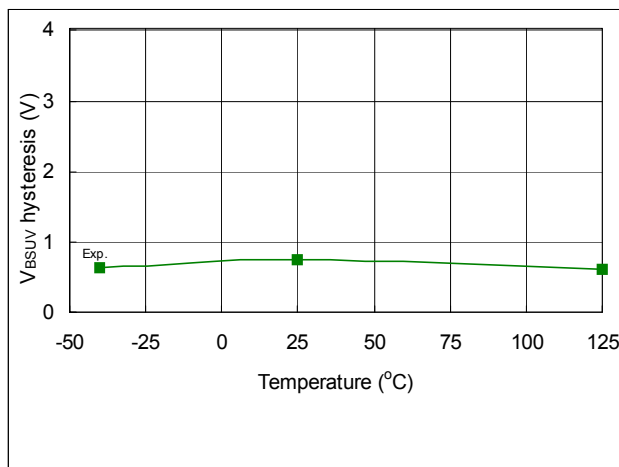


Fig. 31. V<sub>BS</sub> Supply UV Hysteresis vs. Temperature

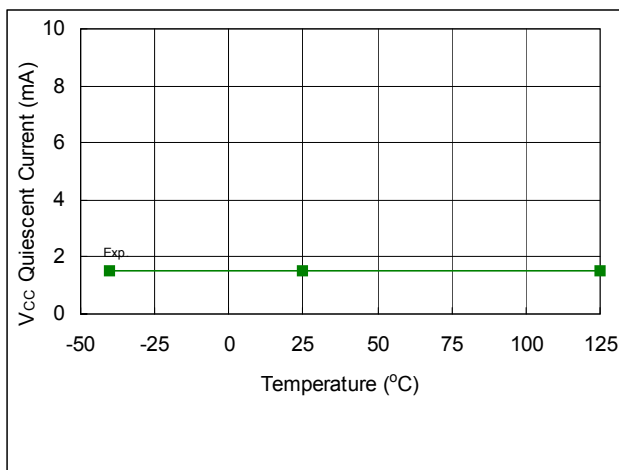


Fig. 32. V<sub>CC</sub> Quiescent Supply Current vs. Temperature

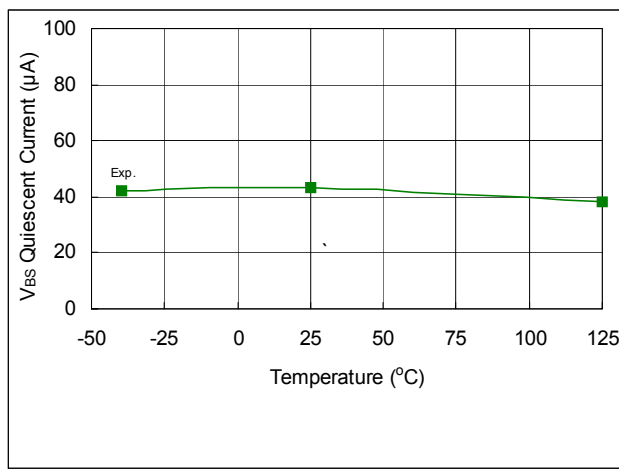


Fig. 33. V<sub>BS</sub> Quiescent Supply Current vs. Temperature

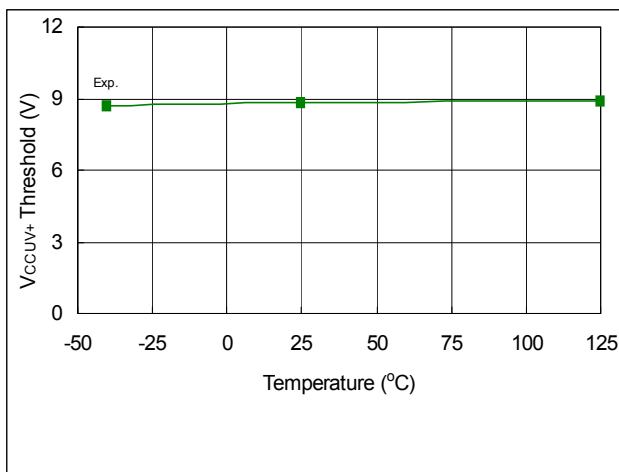


Fig. 35. V<sub>CCUV+</sub> Threshold vs. Temperature

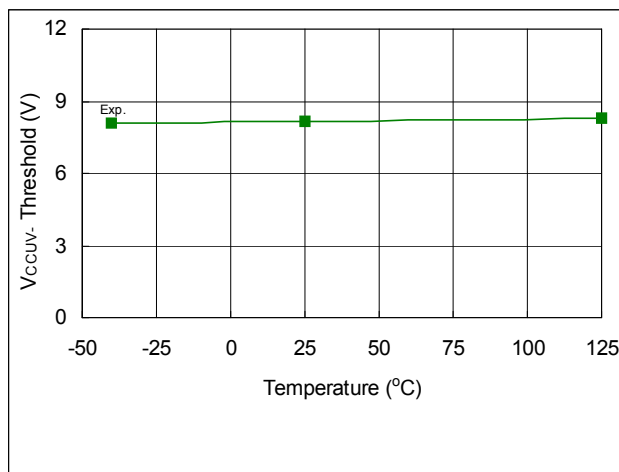


Fig. 36. V<sub>CCUV-</sub> Threshold vs. Temperature

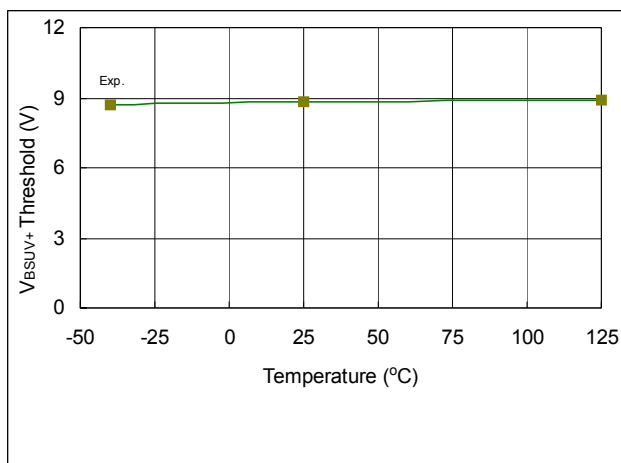


Fig. 37.  $V_{BSUV+}$  Threshold vs. Temperature

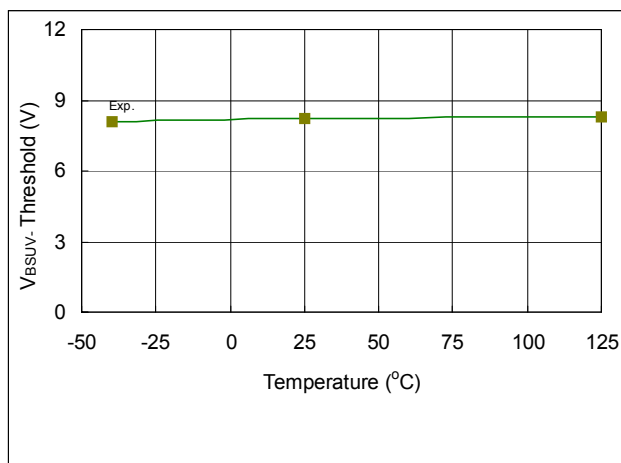


Fig. 38.  $V_{BSUV-}$  Threshold vs. Temperature

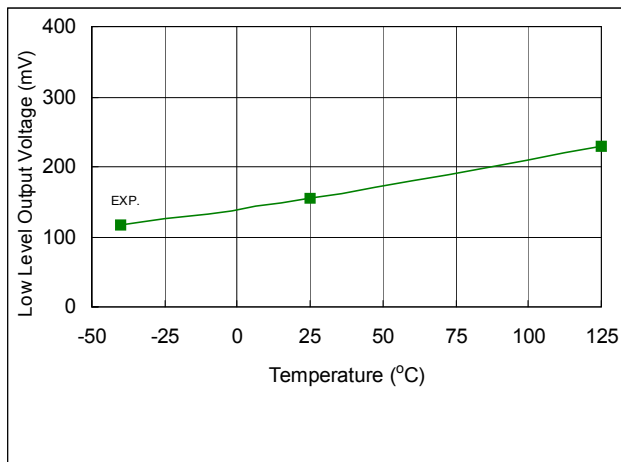


Fig. 38. Low Level Output Voltage vs. Temperature

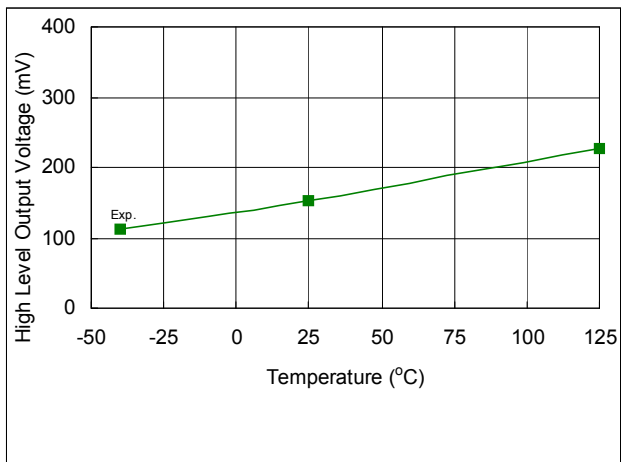


Fig. 39. High Level Output Voltage vs. Temperature

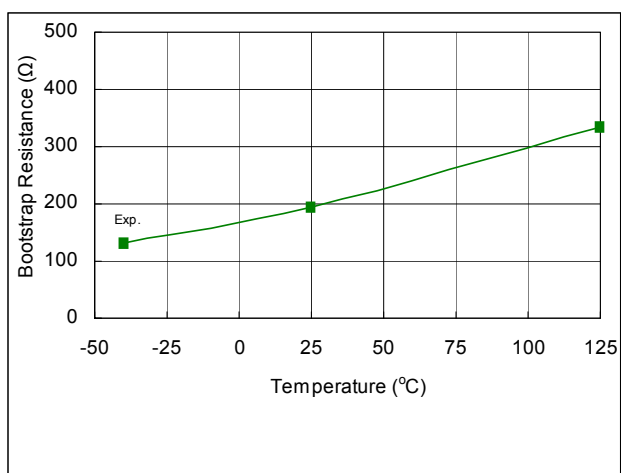


Fig. 40. Bootstrap Resistance vs. Temperature

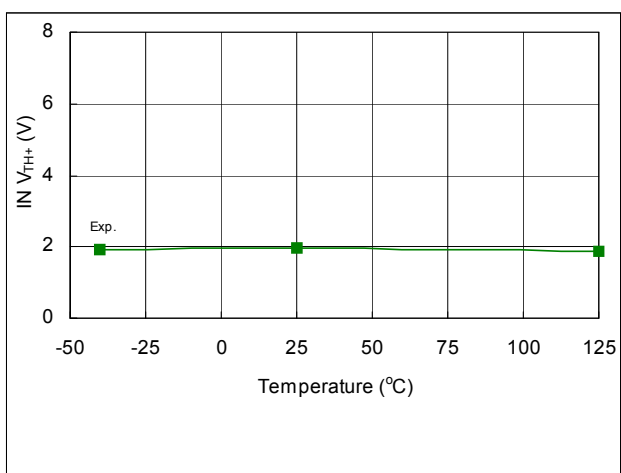


Fig. 41.  $I_N V_{TH+}$  vs. Temperature

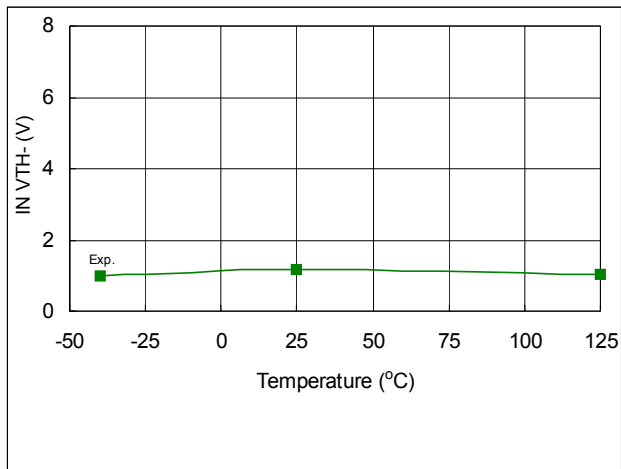


Fig. 42. LIN V<sub>TH-</sub> vs. Temperature

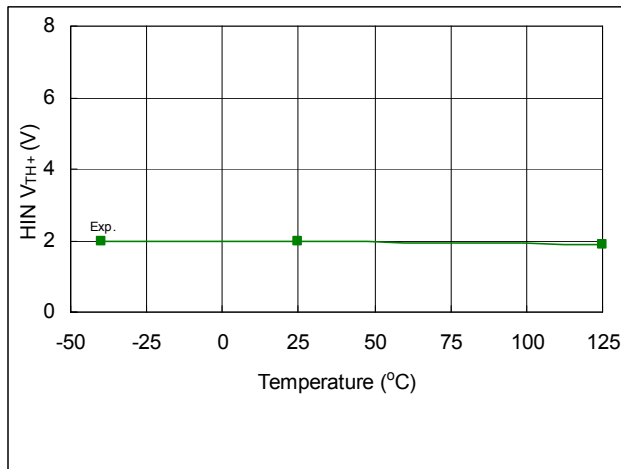


Fig. 43. HIN V<sub>TH+</sub> vs. Temperature

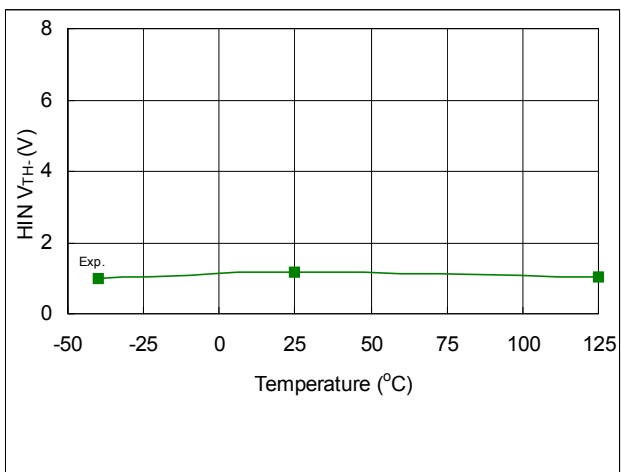


Fig. 44. HIN V<sub>TH-</sub> vs. Temperature

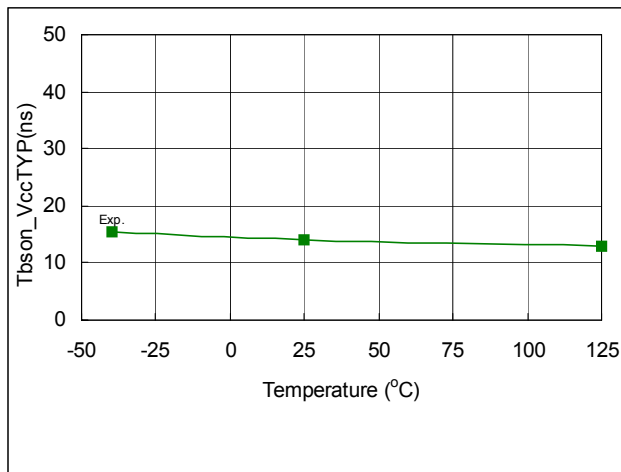


Fig. 45. T<sub>bson\_VccTYP</sub> vs. Temperature

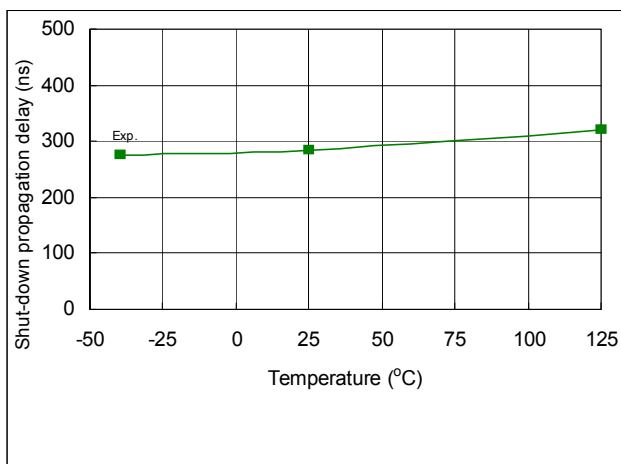


Fig. 46. Shut-down Propagation Delay vs. Temperature

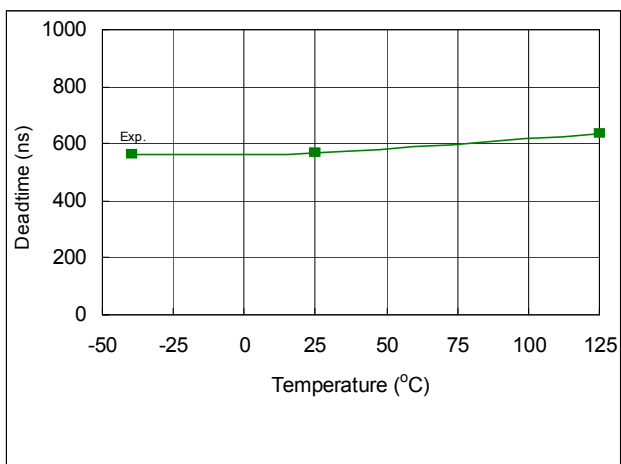


Fig. 47. Deadtime vs. Temperature

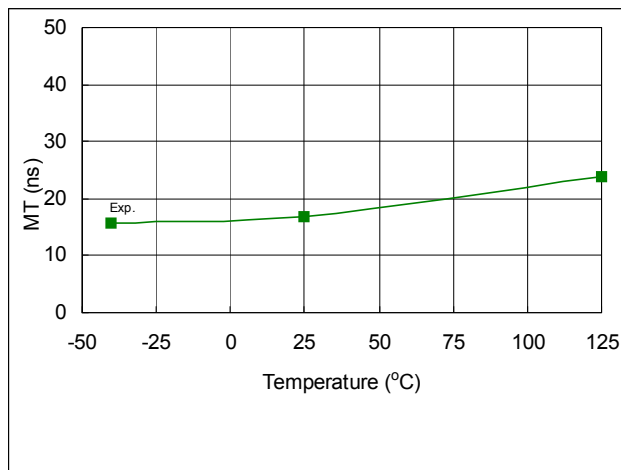


Fig. 48. Delay Matching vs. Temperature

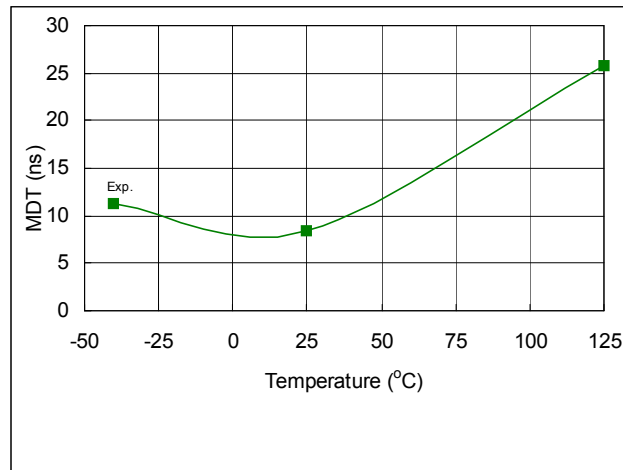
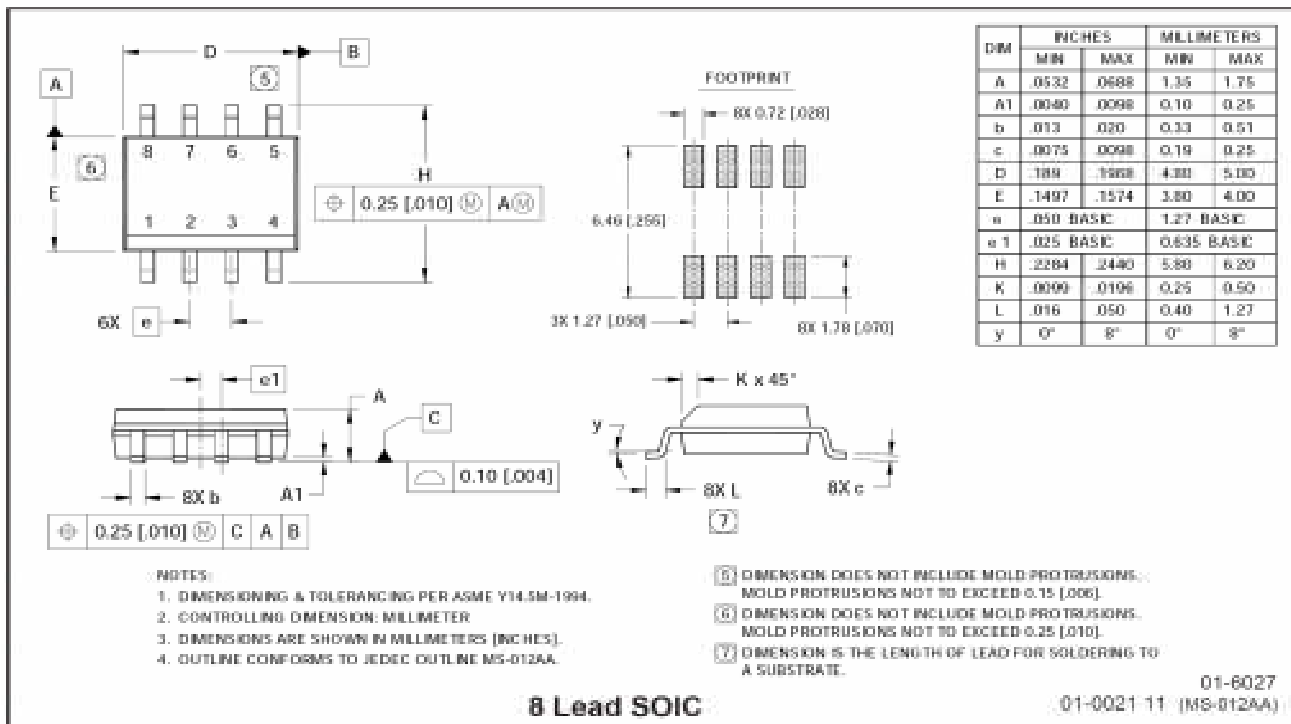
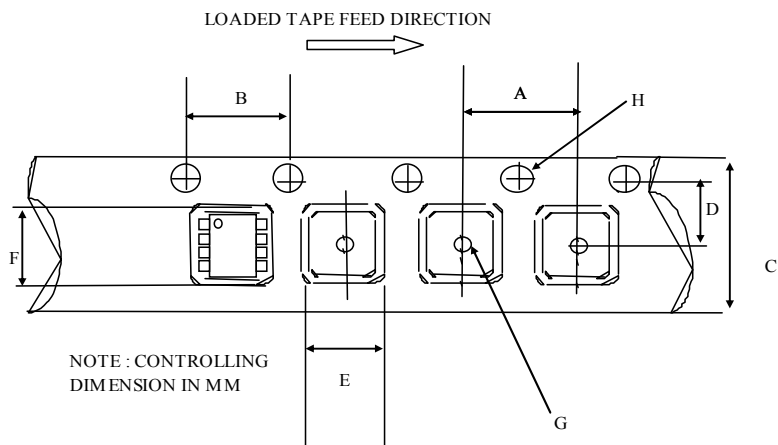


Fig. 49. Deadtime Matching vs. Temperature

**Case Outlines**

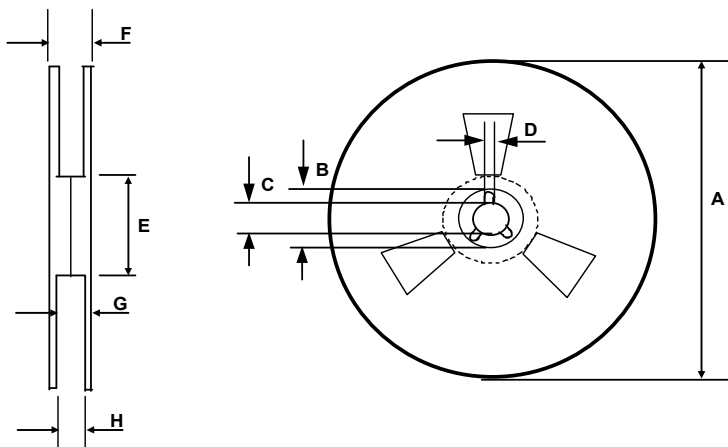


**Tape and Reel Details: 8L-SOIC**



**CARRIER TAPE DIMENSION FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

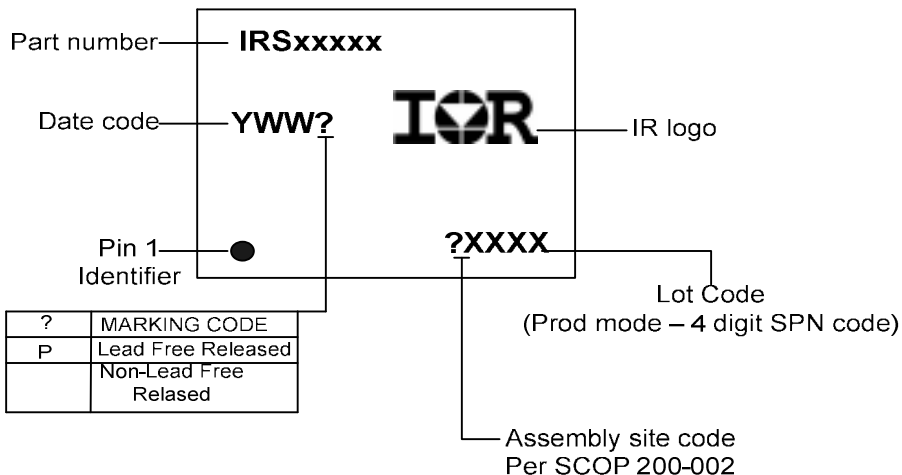


**REEL DIMENSIONS FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566



**LEAD-FREE PART MARKING INFORMATION**



**ORDER INFORMATION**

8-Lead SOIC IRS2609DSPbF

8-Lead SOIC Tape & Reel IRS2609DSTRPbF

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233 Kansas St., El Segundo, California 90245  
Tel: (310) 252-7105

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Comments/Changed items</b>
1.5	03-17-08	Added application note to include negative Vs curve
1.6	03-17-08	Added Qualification Information on Page 2, Disclaimer information on Page 25, and updated information on Pages 21-23
1.6a	03-21-08	Removed revision letter from JEDEC standards under Qualification Information table.
1.7	04-18-08	Added “RoHS compliant” statement to front page, Changed latch up level to A, added MT parameter.
	May 8, 08	Changed file name from using revision to using date, Page1: corrected IGBT, Page5: corrected p/n on lead assignment diagram to IRS2609DS
	06-18-08	Corrected internal dead time on front page to 530ns instead of 540ns.
	08-18-2009	Removed reference to trapezoidal modulation in Integrated Bootstrap Functionality section