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International
IOR Rectifier

Data Sheet No. PD 60321A

IRS26302DJPBF

FULLY PROTECTED 3-PHASE BRIDGE PLUS ONE GATE DRIVER

Features

- Floating channel designed for bootstrap operation, fully
- operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Full three phase gate driver plus one low side driver
- Undervoltage lockout for all channels
- Cross-conduction prevention logic
- Power-on reset
- Integrated bootstrap diode for floating channel supply
- Over current protection on: DC-(Itrip), DC+(Ground fault), PFCtrip/BRtrip (PFC/Brake protection).
- Single pin fault diagnostic function
- Diagnostic protocol to address fault register
- Self biasing for ground fault detection high voltage circuit
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- RoHS compliant

Typical Applications

- Air conditioners inverters
- Micro/Mini inverter drives
- General purpose inverter
- Motor control

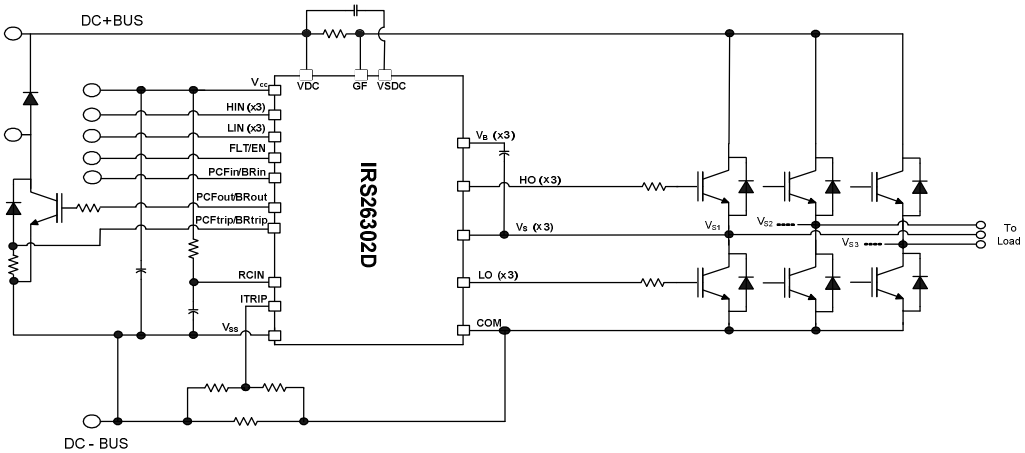
Product Summary

Topology	3 Phase
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	200 mA & 350 mA
Deadtime (typical)	290 ns

Package

44-Lead PLCC

Typical Connection Diagram



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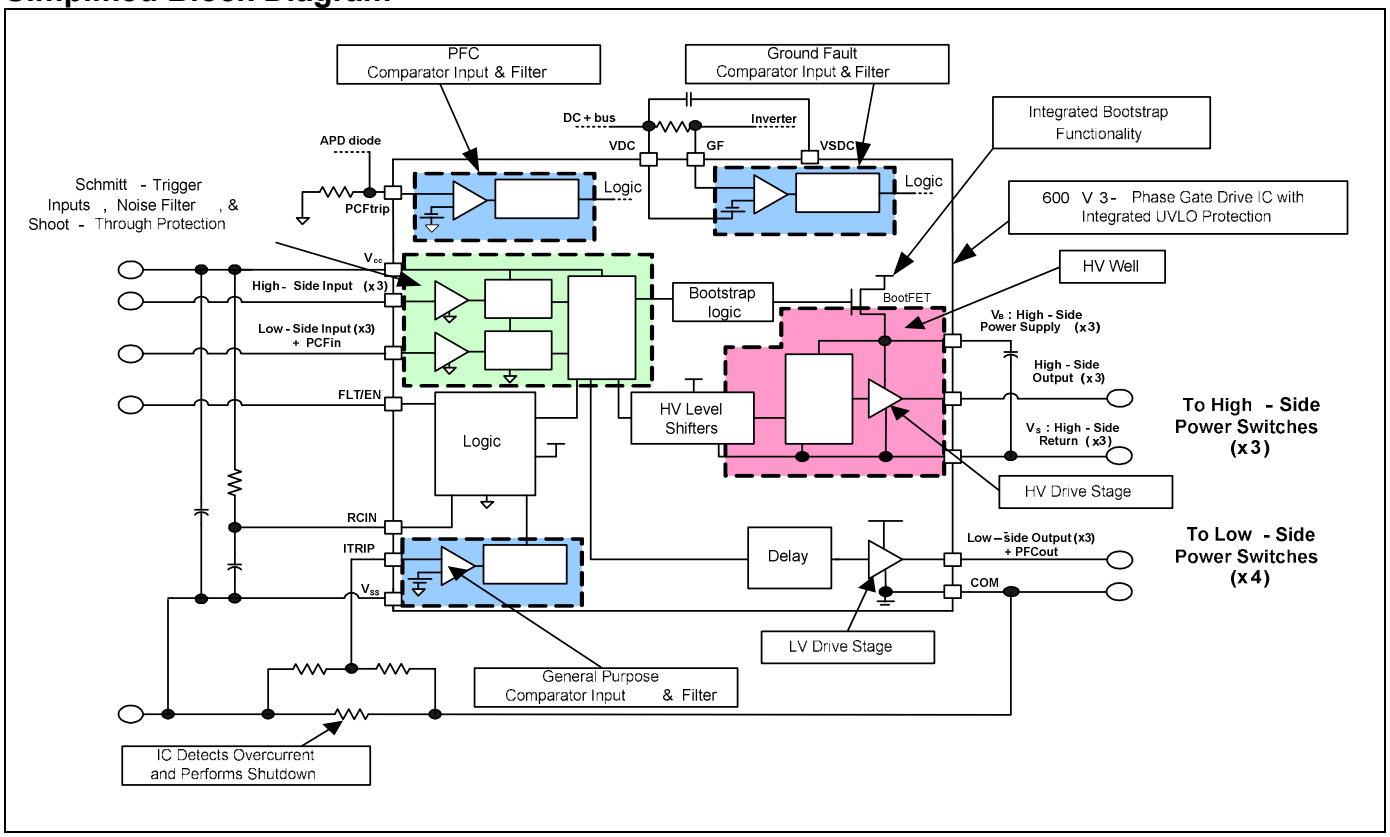
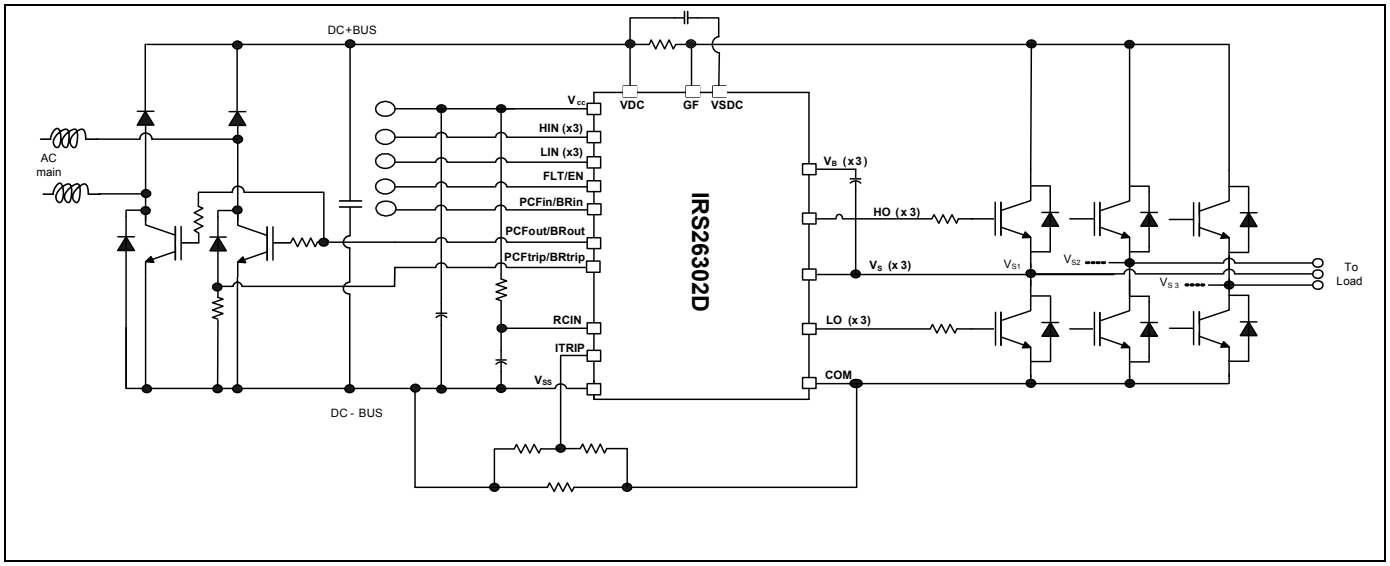
Description

The IRS26302DJPBF are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. An additional low side driver is included for PFC or Brake IGBT driving operation. Proprietary HVIC technology enables rugged monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. Three current trip functions that terminate all seven outputs can be derived from three external shunt resistors. Each overcurrent trip functions consists of detecting excess current across a shunt resistor on DC+ bus, on DC- bus and on Brake or PFC circuitry. An enable function is available to terminate all outputs simultaneously and is provided through a bidirectional pin combined with an open-drain FAULT pin. Fault signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after an externally programmed delay via an RC network connected to the RCIN input. A diagnostic feature can give back to the controller the fault cause (UVcc, DC- or DC- overcurrent) and address a fault register. The output drivers feature a high pulse current buffer stage. Propagation delays are matched to simplify use in high frequency applications designed for minimum driver cross conduction. The floating channel can be used to drive N-channel power MOSFET's or IGBT's in the high side configuration which operates up to 600 V.

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47E)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		PLCC44	MSL3††† (per IPC/JEDEC J-STD-020C)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A114D)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A115-A)	
	Charged Device Model	Class IV (per JEDEC standard JESD22-C101C)	
IC Latch-Up Test		Class I, Level A (per JESD78A)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20 V), and V_B & V_S (20 V).

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	-0.3	620	V
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
$V_{S1,2,3}$	High side offset voltage	$V_{B1,2,3}$ - 20	$V_{B\ 1,2,3}$ + 0.3	
VDC	DCbus Supply Voltage	-0.3	620	
GF	Input voltage for Ground Fault detection	VDC-20	VDC+0.3	
VSDC	High voltage return for Ground Fault circuit	VDC-20	VDC+0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20†	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage LO1,2,3, PFCout	-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN1,2,3, HIN1,2,3, ITRIP, PFCtrip, FLTEN, RCIN	-0.3	V_{CC} + 0.3	
$V_{PFCtrip}/V_{BRtrip}$	Input voltage $V_{PFCtrip}/V_{BRtrip}$	-2	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	—	4.6	W
R_{THJA}	Thermal resistance, junction to ambient	—	27	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC}-COM) = (V_B-V_S) = 15 V. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{HO\ 1,2,3}$	High side output voltage HO1,2,3	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{S\ 1,2,3}$	High side floating supply voltage †	Vss – 8	600	
$V_{St\ 1,2,3}$	Transient high side floating supply voltage ††	-50	600	
VDC	DCbus Supply Voltage	(TBD)	600	
GF	Input voltage for Ground Fault detection	VDC-5	VDC	
VSDC	High voltage return for Ground Fault circuit	VDC-12	VDC-11	
V_{CC}	Low side supply voltage	10	20	
$V_{LO1,2,3}$	Low side output voltage LO1,2,3, PFCout	0	V_{CC}	
COM	Power ground	-5	5	
V_{SCOM}	Negative transient Vs voltage	0	-20[1)]	
V_{FLT}	FAULT output voltage	0	V_{CC}	
V_{RCIN}	RCIN input voltage	0	V_{CC}	
$V_{HO\ 1,2,3}$	High side output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low side output voltage	COM	V_{CC}	
V_{ITRIP}	ITRIP input voltage	0	5	
PFC_{ITRIP} /BR_{ITRIP}	PFC_{ITRIP}/BR_{ITRIP} input voltage	-2	0	
V_{IN}	Logic input voltage LIN, HIN, PFCin, BRin, EN	V_{SS}	V_{SS} +5	
T_A	Ambient temperature	-40	125	ºC

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative V_S of V_{SS} - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. TA = 25°C unless otherwise specified. The VIN and IIN parameters are referenced to V_{SS} and are applicable to all six channels. The VO and IO parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S. The PFCIo/BRIo and VPFC/ VBR are referenced to V_{SS} and are applicable to PFCout/BRout lead.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VIH	Logic "1" input voltage	2.5	—	—	V	
VIL	Logic "0" input voltage	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	2.5		
$V_{IN,TH-}$	Input negative going threshold	0.8	1	—		
$V_{IT,TH+}$	Input positive going threshold	0.160	0.200	0.240		
$V_{IT,TH-}$	Input negative going threshold	0.144	0.180	0.216		
$V_{IT,HYS}$	ITRIP hysteresis	—	20	—	mV	
$V_{PFCT,TH+}$ $V_{BRT,TH+}$	PFC/BR positive going threshold	-0.144	-0.180	-0.216	V	
$V_{PFCT,TH-}$ $V_{BRT,TH-}$	PFC/BR negative going threshold	-0.160	-0.200	-0.240		
$V_{PFCT,HYS}$ $V_{BRT,HYS}$	PFC/BR hysteresis	—	20	—	mV	
$V_{GFT,TH+}$	GF positive going threshold	0.140	0.180	0.220	V	$V_{GFT} = V_{DC} - V_{GF}$
$V_{GFT,TH-}$	GF negative going threshold	0.150	0.200	0.240		
$V_{GFT,HYS}$	GF hysteresis	—	20	—	mV	
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—	V	
$V_{RCIN,HYS}$	RCIN hysteresis	—	3	—		
$V_{CC,UVTH+}$	V_{CC} supply undervoltage positive going threshold	10.2	11.1	12.0		
$V_{CC,UVTH-}$	V_{CC} supply undervoltage negative going threshold	10.0	10.9	11.8		
$V_{CC,UVHYS}$	V_{CC} supply undervoltage hysteresis	—	0.2	—		
$V_{BS,UVTH+}$	V_{BS} supply undervoltage positive going threshold	10.2	11.1	12.0		
$V_{BS,\ UVTH-}$	V_{BS} supply undervoltage negative going threshold	10.0	10.9	11.8		
$V_{BS,UVHS}$	V_{BS} supply undervoltage hysteresis	—	0.2	—		
ILK	Offset supply leakage current	—	—	50	µA	VB1,2,3 = VDC = GF =600 V, VDC - VDCS = 20 V
Iqbs	Quiescent VBS supply current	—	45	120		All input/output in off status
Iqcc	Quiescent VCC supply current	—	2.5	4	mA	All input/output in off status
Io+	Output high short circuit pulsed current, HO1,2,3	100	200	—		Vout = 0 V, PW </= 10 us
Io-	Output low short circuit pulsed current, HO1,2,3	190	350	—	mA	Vout = 15 V, PW </= 10 us
VOH	High level output voltage, VBIAS – VO, HO1,2,3	—	0.9	1.4	V	IO = 20 mA
VOL	Low level output voltage, VO, HO1,2,3	—	0.4	0.6		

Static Electrical Characteristics (continued)

(V_{CC}-COM) = (V_B-V_S) = 15 V. TA = 25°C unless otherwise specified. The VIN and IIN parameters are referenced to V_{SS} and are applicable to all six channels. The VO and IO parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S. The PFCIo/BRIo and VPFC/ VBR are referenced to V_{SS} and are applicable to PFCout/BRout lead.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$PFCI_{O+}$/ BRI_{O+}	Output high short circuit pulsed current, PFC_{OUT} /BR_{OUT}	120	250	—	mA	P_{FCOUT} = 0 V, PW </= 10 us
$PFCI_{O-}$/ BRI_{O-}	Output low short circuit pulsed current, PFC_{OUT}/BR_{OUT}	210	430	—		P_{FCOUT} = 15 V, PW </= 10 us
V_{PFCH} /V_{BRH}	High level output voltage, V_{BIAS} – V_O, PFC_{OUT}/BR_{OUT}	—	900	1400	mV	I_O = 20 mA
V_{PFCL} /V_{BRL}	low level output voltage, V_O, PFC_{OUT}/BR_{OUT}	—	400	600		
I_{IN+}	Input bias current LIN1,2,3, HIN1,2,3, PFC_{IN}/$BR_{IN,}$ (OUT=HI)	350	—	860	µA	V_{IN} = 3.3 V
I_{IN-}	Input bias current LIN1,2,3, HIN1,2,3, PFC_{IN}/$BR_{IN,}$ (OUT=LO)	—	0	1		V_{IN} = 0 V
I_{ITRIP+}	ITRIP input bias current	—	1	2		V_{ITRIP} = 1 V
I_{ITRIP-}	ITRIP input bias current	—	0	5		V_{ITRIP} = 0 V
$IPFC_{TRIP+}$/ IBR_{TRIP+}	PFC_{TRIP} /BR_{TRIP} input bias current	—	20	—		$V_{PFCTRIP}$ =-250 mV
$IPFC_{TRIP}$/ IBR_{TRIP-}	PFC_{TRIP} /BR_{TRIP} input bias current	—	0	5		$V_{PFCTRIP}$ = 0 V
I_{RCIN}	RCIN input bias current	—	0	5		V_{RCIN} = 15 V
IEN_{IN}	EN input bias current	—	0	1		V_{EN} = 3.3V
Ron_RCIN	RCIN low on resistance	—	50	100	Ω	I = 1.5 mA
R_{ON_FLT}	FLT low on resistance	—	50	100		I = 1.5 mA
RBS	Ron internal bootstrap diode	—	200	—		
IqVdcon	Quiescent VDC supply current on status	100	200	300	µA	VDC - Vgf = 250 mV, VDC+ = 40 -600 V
IqVdcoff	Quiescent VDC supply current off status	100	200	300		VDC = Vgf , VDC + = 40- 600 V

Dynamic Electrical Characteristics

V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
LO_{ton} , HO_{ton}	Turn-on propagation delay, LO1,2,3, HO1,2,3	320	—	710	ns	LIN = 0 V ≥ **3.3 V**, HIN = 0 V
LO_{toff} , HO_{toff}	Turn-off propagation delay, LO1,2,3, HO1,2,3	320	—	710		LIN = **3.3 V** ≥ 0 V, HIN = 0 V
LO_{tr} , HO_{tr}	Turn-on rise time LO1,2,3, HO1,2,3	—	125	190		C_{LOAD} = 1nF
LO_{tf} ,HO_{tf}	Turn-off fall time LO1,2,3, HO1,2,3	—	50	75		C_{LOAD} = 1nF
P_{FCton}/B_{Rton}	Turn-on propagation delay, PFC_{OUT}/BR_{OUT} (CL = 2200pF)	300	—	660		P_{FCIN} = 0 V ≥ **3.3 V**
P_{FCtoff}/B_{Rtoff}	Turn-off propagation delay, PFC_{OUT}/BR_{OUT} (CL = 2200pF)	300	—	660		P_{FCIN} = **3.3 V** ≥ 0 V
P_{FCtr}/B_{Rtr}	Turn-on rise time, PFC_{OUT}/BR_{OUT} (CL= 2200 pF)	—	180	—		C_{LOAD} = 2.2 nF
P_{FCtf}/B_{Rtf}	Turn-off rise time, PFC_{OUT}/BR_{OUT} (CL = 2200 pF)	—	60	—		C_{LOAD} = 2.2 nF
t_{EN}	ENABLE low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or **3.3 V**
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	800	—		V_{ITRIP} = **2 V**
$t_{ITRIPbl}$	ITRIP blanking time	250	400	600		V_{IN} = 0 V or **3.3 V** V_{ITRIP} = **2 V**
$t_{PFCtrip}$	PFC_{TRIP} to output shutdown propagation delay	—	800	—		
t_{PFCbl}/t_{BRbl}	PFC_{TRIP}/BR_{TRIP} blanking time	—	500	—		
t_{FILIN}	Input filter time † (HIN, LIN, PFC_{IN} /BR_{IN}, EN)	200	350	—		V_{IN} = 0 V & **3.3 V**
$t_{filterEn}$	Enable input filter time	100	200	—		
DT	Deadtime	190	290	420		LIN = **3.3 V** ≥ 0 V, HIN = 0 V ≥ **3.3 V**
MT	Ton, off matching time (on all six channels)	—	—	50		
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	60		
PM	Pulse width distortion ††	—	—	75		PW input = 10 us
t_{FLTCLR}	FAULT clear time RCIN: R=2meg, C=1nF	40	60	80	µs	R = 100 KΩ, C = 680 pF, on RCIN
$t_{ITRIPBLK}$	ITRIP blanking time	250	400	600	ns	
$t_{ITRIPFLT}$	ITRIP to fault time	800	1150	1500		V_{ITRIP} = 0 V ≥ **2 V** to FLT/En = **3.3 V** ≥ 0 V
$t_{ITRIPOUT}$	ITRIP to output shutdown propagation delay	500	720	950		V_{ITRIP} =0 V ≥ **2 V** to LOx/Hox = 15 V ≥ 0 V

† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.

†† PM is defined as PW_{IN} - PW_{OUT}.

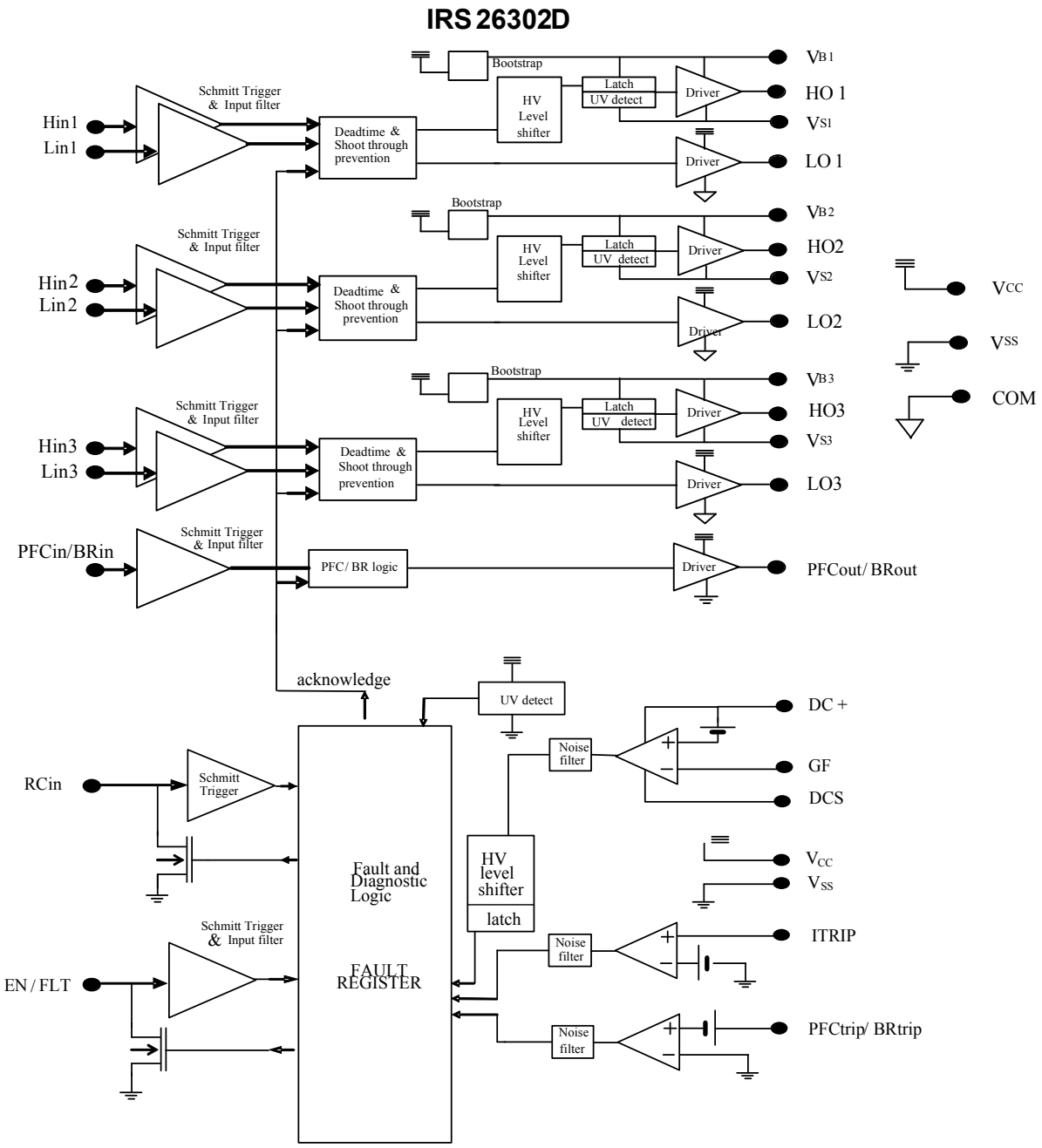
Dynamic Electrical Characteristics

V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25 °C, and C_L = 1000 pF unless otherwise specified.

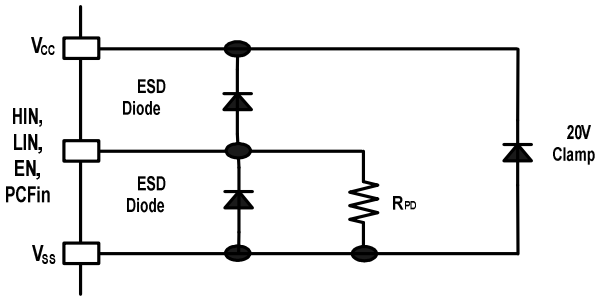
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{ITRIPPFC}/t_{ITRIPBR}$	ITRIP to PFCout/BRout shutdown propagation delay	400	620	850	ns	V_{ITRIP} = **-1 V** ≥ **2 V** to P_{FCOUT}/B_{ROUT} = 15 V ≥ 0 V
$t_{PFCTRIPFLT}$ /$t_{BRTRIPFLT}$	PFCTRIP/BRTRIP to fault time	700	1000	1500		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** V to FLT/En = **3.3 V** ≥ 0 V
$t_{PFCTRIPOUT}$ /$t_{BRTRIPOUT}$	PFCTRIP/BRTRIP to output shutdown propagation delay	400	600	950		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** to LOx/Hox = 15 V ≥ 0 V
$t_{PFCTRIPPFC}$ /$t_{BRTRIPPFC}$	PFCTRIP/BRTRIP to PFC output shutdown propagation delay	320	500	850		$V_{PFCTRIP}/V_{BRTRIP}$ = **1V** ≥ -**1.5 V** to P_{FCOUT} = 15 V ≥ 0 V
$t_{PFCTRIPBLK}$ /$t_{BRTRIPBLK}$	PFCTRIP/BRTRIP blanking time	150	450	750		
$t_{GFTRIPFLT}$	GFTRIP to fault time	1000	1400	1800		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to FLT/En = 15 V ≥ 0 V
$t_{GFTRIPOUT}$	GFTRIP to output shutdown propagation delay	700	1000	1300		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to LOx/Hox = 15 V ≥ 0 V
$t_{GFTRIPPFC}$	GFTRIP to PFC output shutdown propagation delay	600	900	1200		V_{GF} = V_{DC} ≥ **V_{DC} -1** V to P_{FCOUT} = 15 V ≥ 0 V
$t_{GFTRIPBLK}$	GFTRIP blanking time	150	300	550		
t_{ENOUT}	EN on to output propagation delay	300	400	500		V_{EN} = 0 V ≥ **3.3 V**, LINx/HINx = **3.3 V** to LOx/Hox = 0 V ≥ 15 V
t_{SDOUT}	EN off to output shutdown propagation delay	320	440	560		V_{EN} = **3.3 V** ≥ 0 V, LINx/HINx = **3.3 V** to LOx/Hox = 15 V ≥ 0 V
t_{ENPFC}/t_{ENBR}	EN on to PFC/Brake output propagation delay	200	320	500		V_{EN} = 0 V ≥ **3.3 V** , P_{FCIN}/B_{RIN} = **3.3 V** to P_{FCOUT}/B_{ROUT} = 0 V ≥ 15 V
t_{SDPFC}/t_{SDBR}	EN off to output shutdown PFC/Brake propagation delay	200	360	500		V_{EN} = **3.3 V** ≥ 0 V, P_{FCIN}/B_{RIN} = **3.3 V** to P_{FCOUT}/B_{ROUT} =15 V ≥ 0 V
$t_{HANDSHAKE}$	Input to Hand shake mode delay	300	500	700		See fault diagnostic state diagram
t_{DIAGIN}	Input to DIAG mode in delay					
$t_{DIAGOUT}$	Input to DIAG mode out delay					

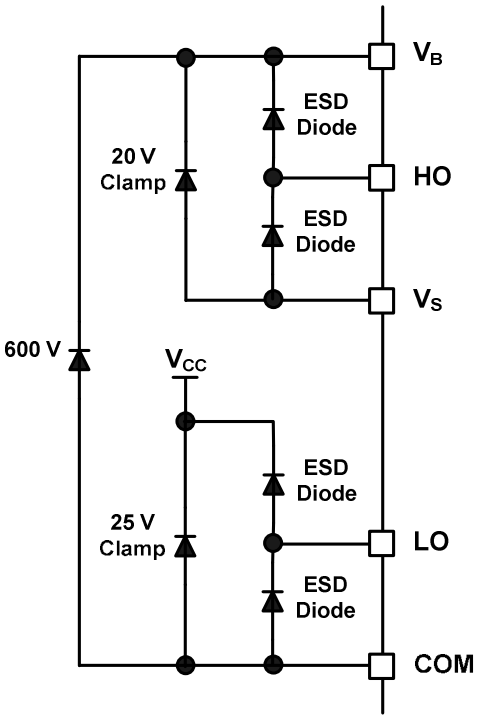
Note 1: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 2: U_{VCC} is not latched, when V_{CC} > U_{VCC}, FAULT return to high impedance.
Note 3: When ITRIP <V_{ITRIP}, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V_{CC} = 15 V)

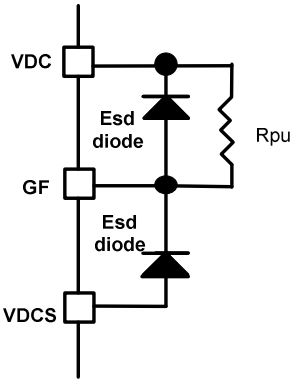
Functional Block Diagram

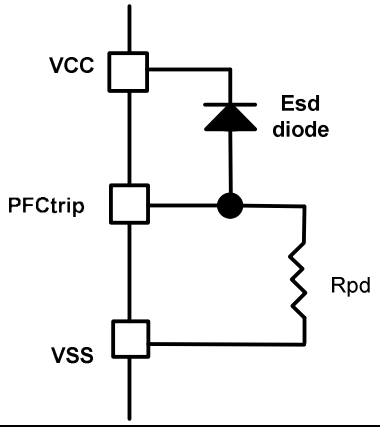


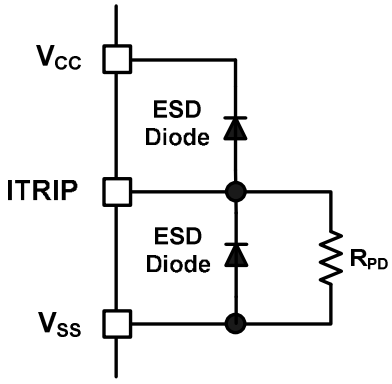
Input/Output Pin Equivalent Circuit Diagrams

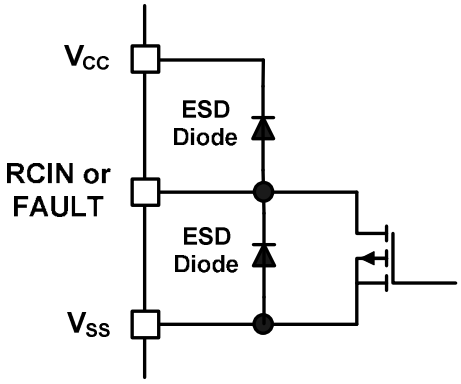








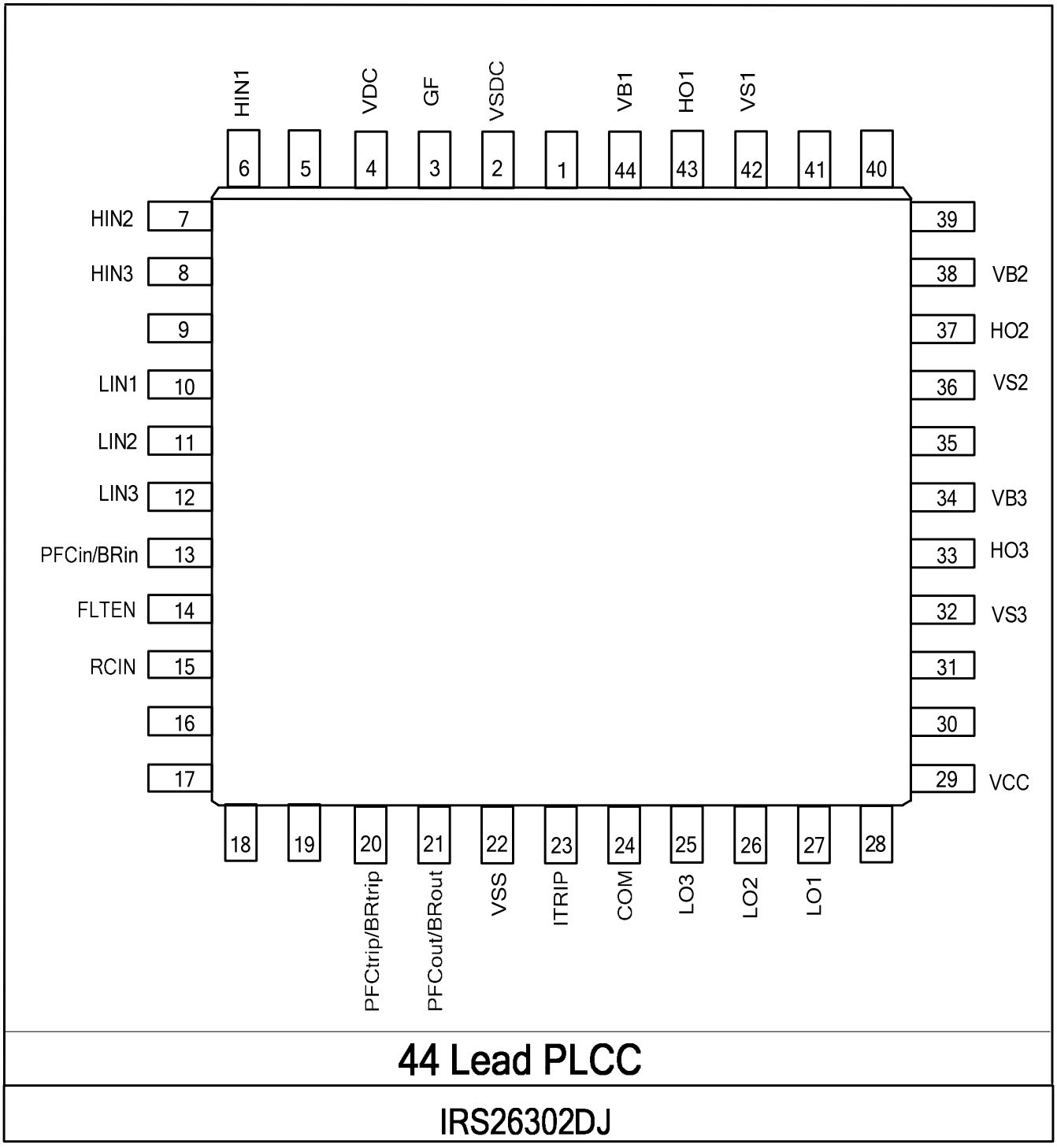




Lead Definitions

Symbol	Description
V_{SDC}	GF supply return
GF	GF analog input for DC + overcurrent shutdown. When active, GF shuts down outputs and activates FAULT and RCIN low. When GF becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
V_{DC}	GF comparator supply (DC bus)
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), in phase
LIN1,2,3	Logic input for low side gate driver outputs (LO1,2,3), in phase
P_{FCTRIP}/B_{RTRIP}	Analog input for PCF overcurrent shutdown. When active, GF shuts down outputs and activates FAULT and RCIN low. When P_{FCTRIP}/B_{RTRIP} becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
P_{FCOUT}/B_{ROUT}	PFC/Brake output
P_{FCIN}/B_{RIN}	Input, PFC/Brake, active high
FAULT/EN	Open Drain and input, act high
ITRIP	Analog input for DC – over-current shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into an open-drain high-impedance state.
V_{SS}	Logic ground
COM	Power ground & Analog input (ITRIP)
LO1,2,3	Low side driver outputs
V_{CC}	Low side supply voltage
$V_{S1,2,3}$	High voltage floating supply return
HO1,2,3	High side driver outputs
$V_{B1,2,3}$	High side floating supply

Lead Assignments



Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Over-Temperature Shutdown Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Diagnostics
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Tolerant to Negative V_S Transients
- PCB Layout Tips
- Integrated Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS26302DJ HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

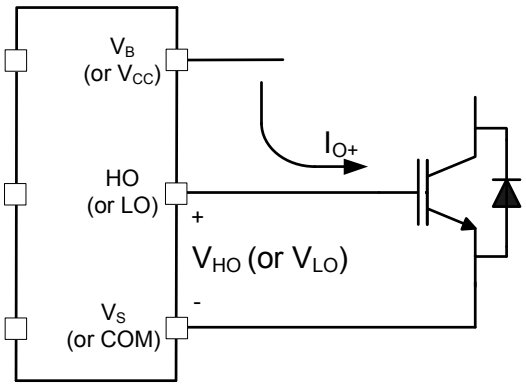


Figure 1: HVIC sourcing current

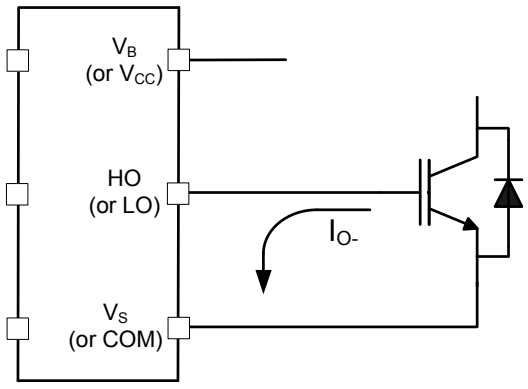


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS26302DJ are illustrated below in Figures 3. From this figure, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

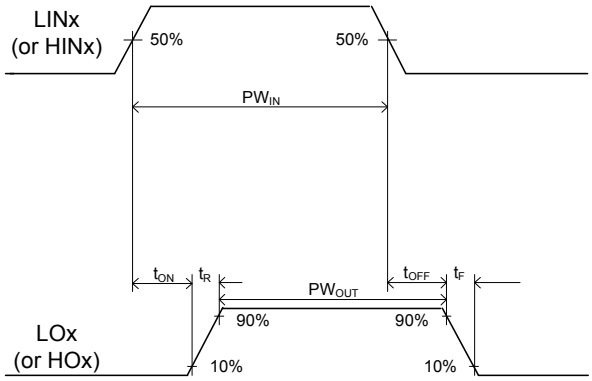


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the IRS26302DJ; this functionality is described in further detail later in this document.

During interval A of Figure 5, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 5 and 6 shows that the signal on the ITRIP, GF, PCFtrip input pin has gone from a not active to an active state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP, GF, PCFtrip input has returned to the not active state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to $V_{RCIN,TH}$ (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 5, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx) being held in the low state until the enable pin is pulled high.

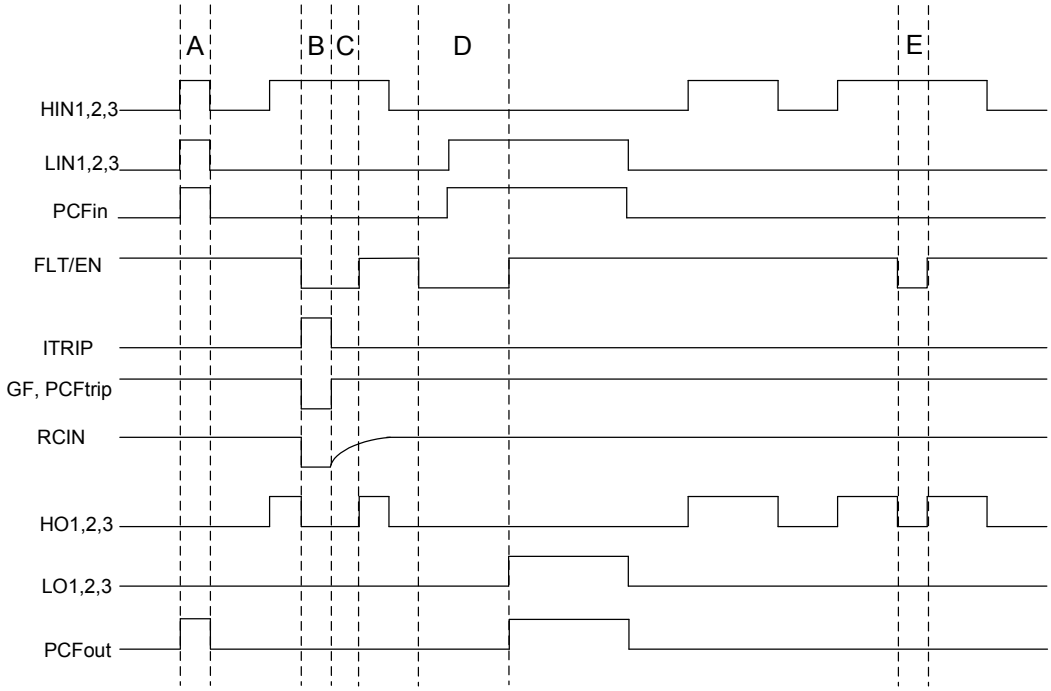


Figure 4: Input/output timing diagram

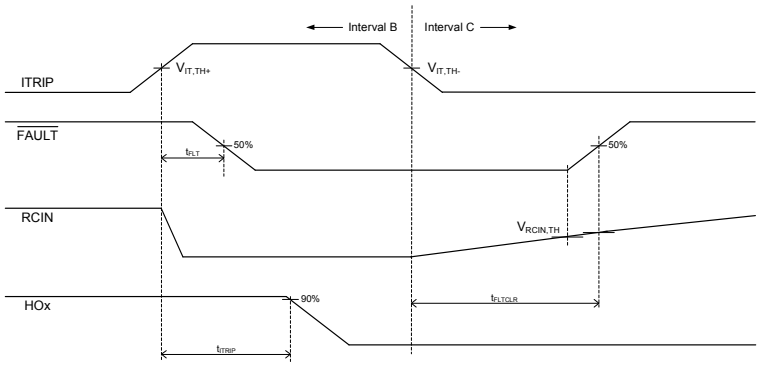


Figure 5: Detailed view of B & C intervals

Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 7 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS26302DJ is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched. Figure 7 defines the two deadtime parameters (i.e., DT_1 and DT_2) of a specific channel; the deadtime matching parameter (MDT) associated with the IRS26302DJ specifies the maximum difference between DT_1 and DT_2. The MDT parameter also applies when comparing the DT of one channel of the IRS26302DJ to that of another.

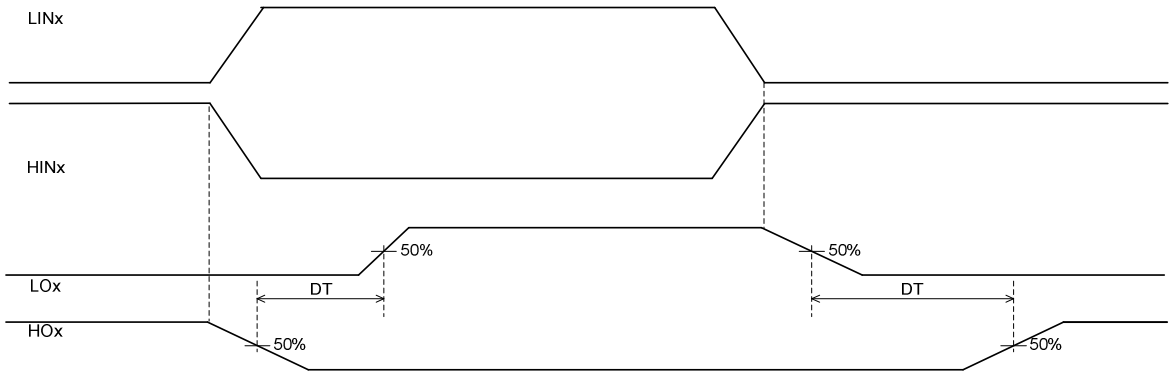


Figure 7: Illustration of deadtime

Matched Propagation Delays

The IRS26302DJ is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other; the MT specification applies as well. The propagation turn-on delay (t_{ON}) of the IRS26302DJ is matched to the propagation turn-on delay (t_{OFF}).

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS26302DJ has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the IRS26302DJ, its input threshold values, and the logic state of the IC as a result of the input signal.

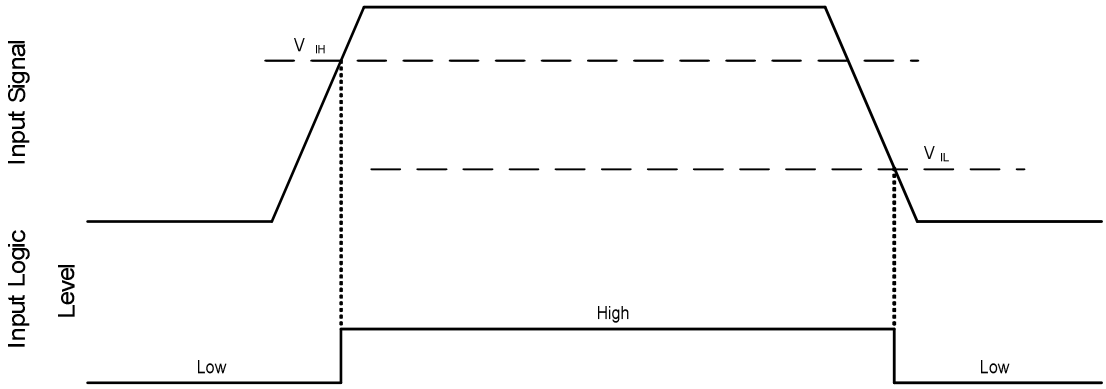


Figure 8: HIN & LIN input thresholds

Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 9 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

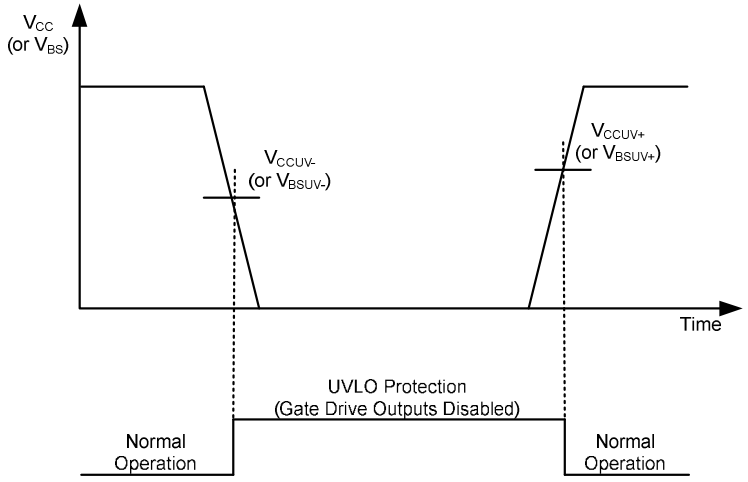


Figure 9: UVLO protection

Shoot-Through Protection

The IRS26302DJ is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table. Note that the IRS26302DJ has non-inverting inputs (the output is in-phase with its respective input).

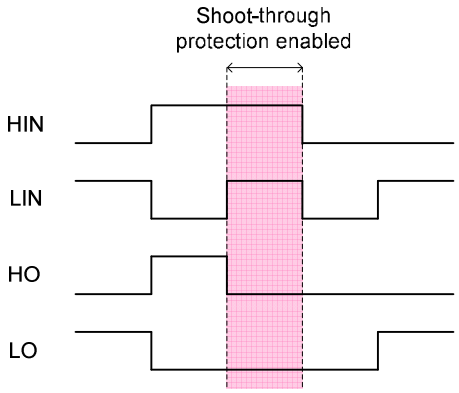


Figure 10: Illustration of shoot-through protection circuitry

HIN	LIN	HO	LO
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Table 1: Input/output truth table

Enable Input

The IRS26302DJ is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state. The enable circuitry of the IRS26302DJ features an input filter; the minimum input duration is specified by $t_{FILTER,EN}$. Please refer to the EN pin parameters $V_{EN,TH+}$, $V_{EN,TH-}$, and I_{EN} for the details of its use. Table 2 gives a summary of this pin's functionality and Figure 11 illustrates the outputs' response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table
(*assumes no other fault condition)

Figure 11: Output enable/disable timing waveform

Fault Reporting and Programmable Fault Clear Timer

The IRS26302DJ provides an integrated fault reporting output and an adjustable fault clear timer. There are several situations that would cause the HVIC to report a fault via the FAULT pin: an undervoltage condition of V_{CC} or ITRIP, Ground Fault (GF), PCFtrip pin recognizes an overcurrent. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 12 where we see that a fault condition has occurred (ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 13 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

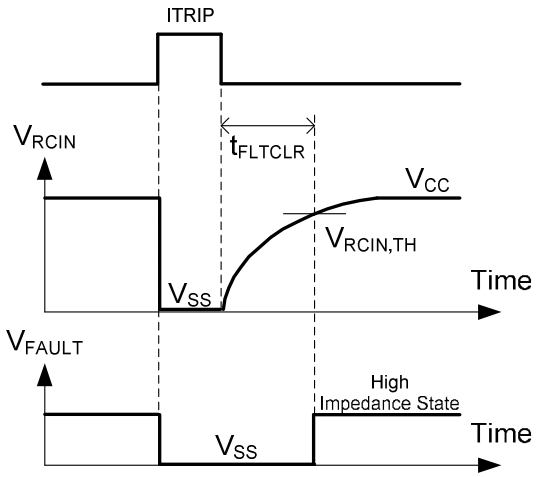


Figure 12: RCIN and FAULT pin waveforms

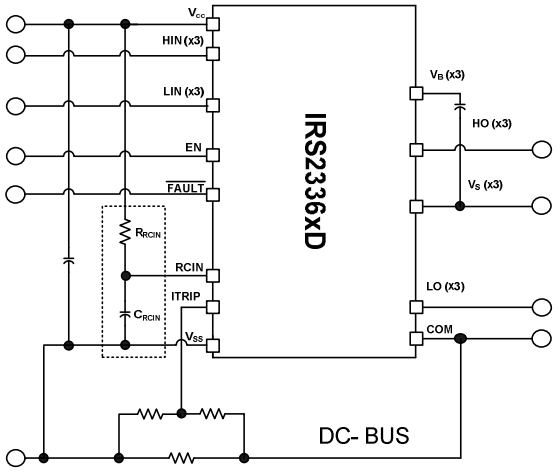


Figure 13: Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RCIN}	≤1 nF, ceramic
R_{RCIN}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RCIN}C_{RCIN})\ln(1-V_{RCIN,TH}/V_{CC})$$

Over-Current Protections

The IRS26302DJ HVICs are equipped with an ITRIP, GF and PFCtrip input pin. These functionality can be used to detect over-current events in the DC- bus, in the DC+ bus, in the PFC section and Ground related. Once the HVIC detects an over-current event, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to V_{SS}.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 14, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{IT,TH+}$) at that current level.

$$V_{IT,TH+} = R_0 I_{DC-}(R_1/(R_1+R_2))$$

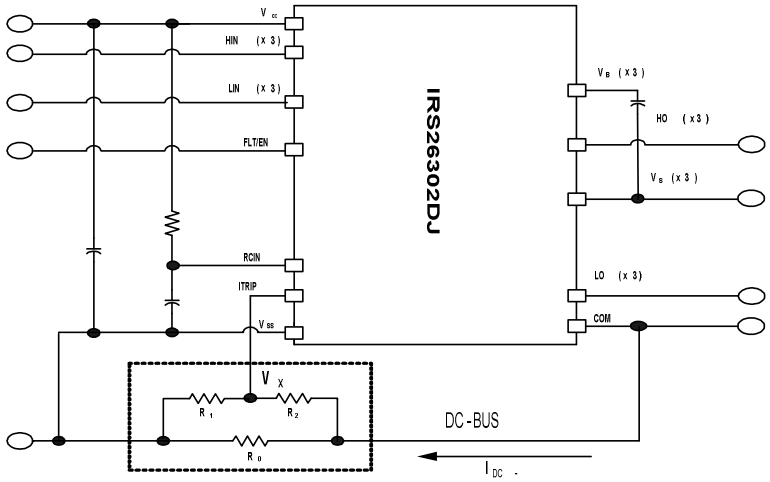


Figure 14: Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

The shunt resistor or resistor network for GF or PCFtrip can be determined according to GF, PCFtrip threshold and level of protection current. The GF pin should not be outside this range (VDC+0.3V, VDC-5V) and PCFtrip should not be outside (Vcc+0.3V, Vss-5V); if necessary, an external voltage clamp may be used.

Over-Temperature Shutdown Protection

The ITRIP input of the IRS26302DJ can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 15 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors R_3 and R_4. As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node V_X. The resistor values should

be selected such the voltage V_X should reach the threshold voltage ($V_{IT,TH+}$) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.

When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 16; the OR-ing diodes have been labeled D_1 and D_2.

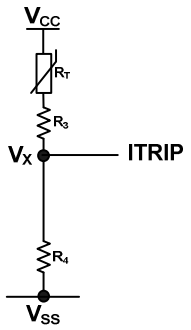


Figure 15: Programming over-temperature protection

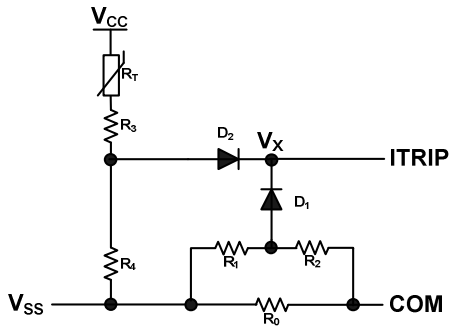


Figure 16: Using over-current protection and over-temperature protection

Truth Table: Undervoltage lockout, ITRIP, GF, PCFtrip and ENABLE

Table 4 provides the truth table for the IRS26302DJ. The first line shows that the UVLO for V_{CC} has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns to the high impedance state.

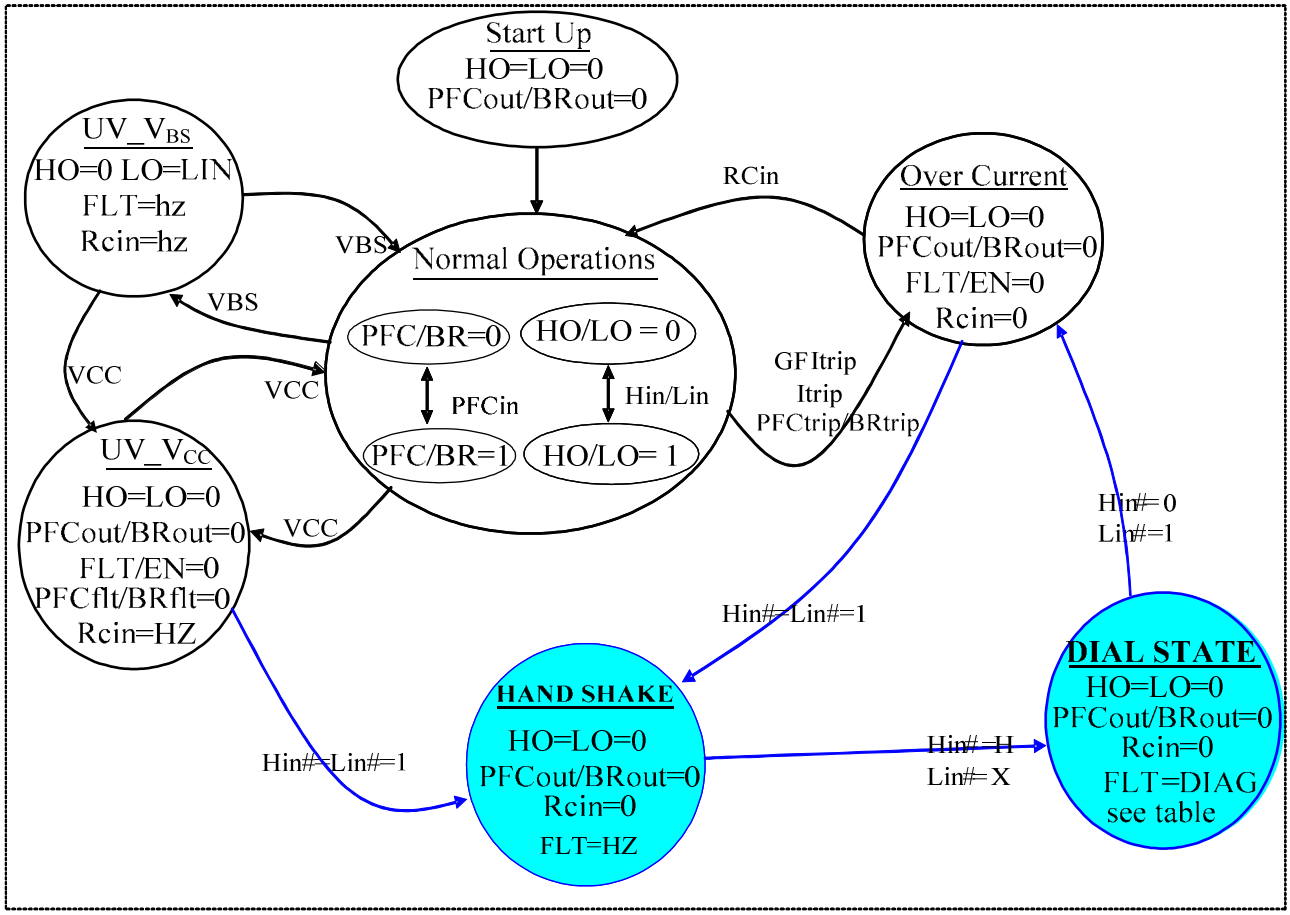
The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin. Same behavior if GF or PCFtrip threshold has been reached. In the last case, the HVIC has received a command through the EN input to shutdown; as a result, the gate drive outputs have been disabled.

	VCC	VBS	ITRIP	GF	PFC trip	EN	RCIN	FAULT	LO	HO	PCFout
UVLO V_{CC}	$<V_{CCUV}$	---	---	---	---	---	High	0	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	0 V	0 V	5 V	High	High Z	LIN	0	0
Normal operation	15 V	15 V	0 V	0 V	0 V	5 V	High	High Z	LIN	HIN	PCFIN
ITRIP fault	15 V	15 V	$>V_{ITRIP}$	0 V	0 V	5 V	Low	0	0	0	0
GF	15 V	15 V	0 V	< GFth	0 V	5 V	Low	0	0	0	0
PCFtrip	15 V	15 V	0 V	0 V	<PCF th	5 V	Low	0	0	0	0
EN	15 V	15 V	0 V	0 V	0 V	0 V	High	High Z	0	0	0

Table 4: IRS26302DJ UVLO, ITRIP, GF, PCFtrip, EN, RCIN, & FAULT truth table

Fault Diagnostic: DIAG STATE –State Diagram

After each fault event a diagnostic feature, if enable, can communicate to the controller which fault happened in the system (UVcc, ITRIP, GF, PCFtrip). If diagnostic is enabled forcing all HIN and all LIN = High the HVIC enters in handshake mode, all the outputs remain off, the automatic fault clear function is disabled and FLT/EN is in HZ (refer to Figure 17 for more details). The HVIC fault register is now ready for queries. A procedure to interrogate the fault register is depicted in the fault query routine (Figure 18).



FLT/EN pin and DIAG mode operation for all fault condition

LIN1,2,3	HIN1,2,3	PFCin/BRin	Condition	RCIN	Itrip	PFCtrip	GF	VCC fault	EN/FLT	Lox	Hox	PFCout/BRout
Linx	Hinx	PFCinx/BRinx		HZ	0	0		V_{CC} > UV_{CC}	HZ			
ALL=H	ALL H	PFCinx/BRinx	(^{0})	HZ	Fault register = 1 (**)				0-> HZ (^{0})	0	0	0
Linx	Hinx	PFCinx/BRinx		0	V > Vth (**)	X	X	X	0	0	0	0
Lin1=L Lin2, 3=H	ALL H	PFCinx/BRinx	(*)	0	V > Vth (**)	X	X	X	0	0	0	0
Lin1=L Lin2, 3=H	ALL H	PFCinx/BRinx	(*)	0	0	X	X	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		0	X	V > Vth (**)	X	X	0	0	0	0
Lin2=L Lin1, 3=H	ALL H	PFCinx/BRinx	(*)	0	X	V > Vth (**)	X	X	0	0	0	0
Lin2=L Lin1, 3=H	ALL H	PFCinx/BRinx	(*)	0	X	0	X	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		0	X	X	V > Vth (**)	X	0	0	0	0
Lin3=L Lin1,2=H	ALL H	PFCinx/BRinx	(*)	0	X	X	V > Vth (**)	X	0	0	0	0
Lin3=L Lin1,2=H	ALL H	PFCinx/BRinx	(*)	0	X	X	0	X	HZ	0	0	0
Linx	Hinx	PFCinx/BRinx		HZ	X	X	X	V_{CC} < UV_{CC}	0	0	0	0
Lin1,2=L Lin3=H	ALL H	PFCinx/BRinx	(*)	0	X	X	X	V_{CC} < UV_{CC}	0	0	0	0
Lin1,2=L Lin3=H	ALL H	PFCinx/BRinx	(*)	0	X	X	X	V_{CC} > UV_{CC}	HZ	0	0	0

(^{0}) HAND SHAKE SYNC
(*) Operation available only in DIAL MODE.
(**) Internal Register fault
DIAG MODE available when FLT=0
Set DIAG MODE: Hinx=Linx=H
During DIAG MODE operation Lox=Hox=0 PFCout/BRout=0 RCIN=0
Reset DIAG MODE: hold Linx=H Hinx=L

Figure 17: State Diagram