μIPM™

4A, 500V

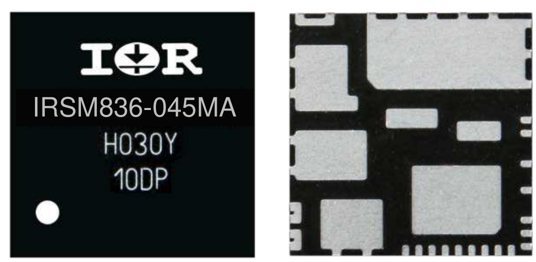
Integrated Power Module for Small Appliance Motor Drive Applications

Description

IRSM836-045MA is a 4A, 500V Integrated Power Module (IPM) designed for advanced appliance motor drive applications such as energy efficient fans and pumps. IR's technology offers an extremely compact, high performance AC motor-driver in an isolated package. This advanced IPM offers a combination of IR's low $R_{DS(on)}$ Trench MOSFET technology and the industry benchmark 3-phase high voltage, rugged driver in a small PQFN package. At only 12x12mm and featuring integrated bootstrap functionality, the compact footprint of this surface-mount package makes it suitable for applications that are space-constrained. Integrated over-current protection, fault reporting and under-voltage lockout functions deliver a high level of protection and fail-safe operation. IRSM836-045MA functions without a heat sink.

Features

- Integrated gate drivers and bootstrap functionality
- Open-source for leg-shunt current sensing
- Protection shutdown pin
- Low $R_{DS(on)}$ Trench FREDFET
- Under-voltage lockout for all channels
- Matched propagation delay for all channels
- Optimized dV/dt for loss and EMI trade offs
- 3.3V Schmitt-triggered active high input logic
- Cross-conduction prevention logic
- Motor power range up to ~130W, without heat sink
- Isolation 1500VRMS min

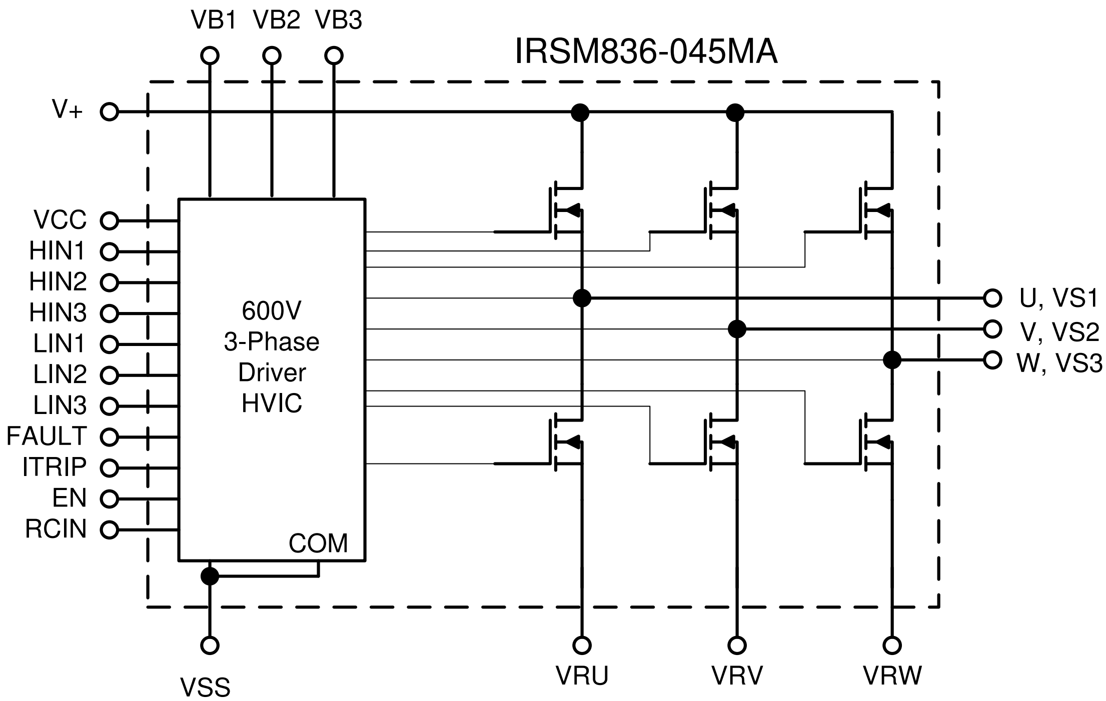


Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRSM836-045MA	37L PQFN 12 x 12 mm	Tape and Reel	2000	IRSM836-045MATR
		Tray	800	IRSM836-045MA

All part numbers are PbF

Photo shown is generic. Refer to final pages of datasheet for accurate module drawings

Internal Electrical Schematic



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table.

Symbol	Description	Min	Max	Unit
BV_{DSS}	MOSFET Blocking Voltage	---	500	V
I_O @ T=25°C	DC Output Current per MOSFET	---	4	A
I_{OP}	Pulsed Output Current (Note 1)	---	35	
P_d @ T_C=25°C	Maximum Power Dissipation per MOSFET	---	24	W
V_{ISO}	Isolation Voltage (1min) (Note 2)	---	1500	V_{RMS}
T_J	Operating Junction Temperature	-40	150	°C
T_L	Lead Temperature (Soldering, 30 seconds)	---	260	°C
T_S	Storage Temperature	-40	150	°C
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	$V_{B1,2,3}$ - 20	$V_{B1,2,3}$ +0.3	V
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	500	V
V_{CC}	Low Side and Logic Supply voltage	-0.3	20	V
V_{IN}	Input Voltage of LIN, HIN, I_{TRIP}, EN, RCIN, FLT	V_{SS} -0.3	V_{CC}+0.3	V

Note 1: Pulse Width = 100µs, TC =25°C, Duty=1%.
Note 2: Characterized, not tested at manufacturing

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V+	Positive DC Bus Input Voltage	---	400	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	(Note 3)	400	V
$V_{B1,2,3}$	High Side Floating Supply Voltage	V_S+12	V_S+20	V
V_{CC}	Low Side and Logic Supply Voltage	13.5	16.5	V
V_{IN}	Input Voltage of LIN, HIN, I_{TRIP}, EN, FLT	0	5	V
F_p	PWM Carrier Frequency	---	20	kHz

The Input/Output logic diagram is shown in Figure 1. For proper operation the module should be used within the recommended conditions. All voltages are absolute referenced to COM. The V_S offset is tested with all supplies biased at 15V differential.

Note 3: Logic operational for V_s from COM-5V to COM+250V. Logic state held for V_s from COM-5V to COM-V_{BS}.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Symbol	Description	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	---	---	V	T_J=25°C, I_{LK}=250µA
I_{LKH}	Leakage Current of High Side FET's in Parallel		10		µA	T_J=25°C, V_{DS}=500V
I_{LKL}	Leakage Current of Low Side FET's in Parallel Plus Gate Drive IC		15		µA	T_J=25°C, V_{DS}=500V
$R_{DS(ON)}$	Drain to Source ON Resistance	---	1.5	1.7	Ω	T_J=25°C, V_{CC}=15V, Id = 2A
$V_{IN,th+}$	Positive Going Input Threshold	2.5	---	---	V	
$V_{IN,th-}$	Negative Going Input Threshold	---	---	0.8	V	
V_{CCUV+}, V_{BSUV+}	V_{CC} and V_{BS} Supply Under-Voltage, Positive Going Threshold	8	8.9	9.8	V	
V_{CCUV-}, V_{BSUV-}	V_{CC} and V_{BS} supply Under-Voltage, Negative Going Threshold	7.4	8.2	9	V	
V_{CCUVH}, V_{BSUVH}	V_{CC} and V_{BS} Supply Under-Voltage Lock-Out Hysteresis	---	0.7	---	V	
I_{QBS}	Quiescent V_{BS} Supply Current V_{IN}=0V	---	---	125	µA	
I_{QCC}	Quiescent V_{CC} Supply Current V_{IN}=0V	---	---	3.35	mA	
$I_{QCC, ON}$	Quiescent V_{CC} Supply Current V_{IN}=4V	---	---	10	mA	
I_{IN+}	Input Bias Current V_{IN}=4V	---	100	160	µA	
I_{IN-}	Input Bias Current V_{IN}=0V	---	--	1	µA	
I_{TRIP+}	I_{TRIP} Bias Current V_{ITRIP}=4V	---	5	40	µA	
I_{TRIP-}	I_{TRIP} Bias Current V_{ITRIP}=0V	---	--	1	µA	
$V_{IT, TH+}$	I_{TRIP} Threshold Voltage	0.37	0.46	0.55	V	
$V_{IT, TH-}$	I_{TRIP} Threshold Voltage	---	0.4	---	V	
$V_{IT, HYS}$	I_{TRIP} Input Hysteresis	---	0.06	---	V	

R_{BR}	Internal Bootstrap Equivalent Resistor Value	---	200	---	Ω	T_J=25°C
$V_{RCIN,TH}$	RCIN Positive Going Threshold	---	8	---	V	
$R_{ON,FAULT}$	FAULT Open-Drain Resistance	---	50	100	Ω	

Note 4: Characterized, not tested at manufacturing

Dynamic Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output Propagation Turn-On Delay Time	---	0.8	1.5	µs	I_D=1mA, V^+=50V See Fig.2
T_{OFF}	Input to Output Propagation Turn-Off Delay Time	---	0.8	1.5	µs	
$T_{FIL,IN}$	Input Filter Time (HIN, LIN)	200	360	---	ns	V_{IN}=0 & V_{IN}=4V
$T_{FIL,EN}$	Input Filter Time (EN)	200	360	---	ns	V_{IN}=0 & V_{IN}=4V
$T_{BLT-ITRIP}$	I_{TRIP} Blanking Time	200	360		ns	V_{IN}=0 & V_{IN}=4V, $V_{I/Trip}$=5V
T_{FAULT}	Itrip to Fault	---	600	950	ns	V_{IN}=0 & V_{IN}=4V
T_{EN}	EN Falling to Switch Turn-Off		680	950	ns	V_{IN}=0 & V_{IN}=4V
T_{ITRIP}	I_{TRIP} to Switch Turn-Off Propagation Delay	---	900	1200	ns	I_D=1A, V^+=50V, See Figure 3

MOSFET Avalanche Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
EAS	Single Pulse Avalanche Energy	---	209	---	mJ	T_J=25°C, L=9.53mH, VDD=150V, I_{TEST}=6.7A

Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{th(J-CT)}$	Total Thermal Resistance Junction to Case Top (Note 5)	---	25	---	°C/W	One device
$R_{th(J-CB)}$	Total Thermal Resistance Junction to Case Bottom (Note 5)	---	1.7	---	°C/W	One device

Note 5: Calculated

Qualification Information†

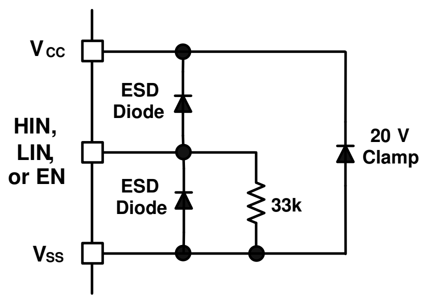
Qualification Level		Industrial[††] (per JEDEC JESD 47E)
Moisture Sensitivity Level		MSL3[†††] (per IPC/JEDEC J-STD-020C)
ESD	**Machine Model**	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per standard ESDA/JEDEC JS-001-2012)
RoHS Compliant		Yes

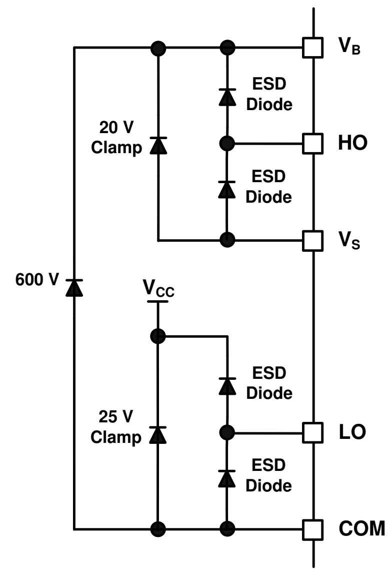
† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

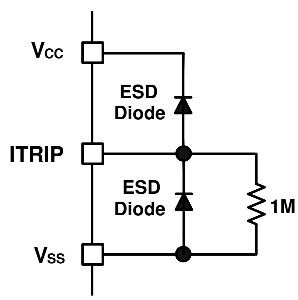
†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

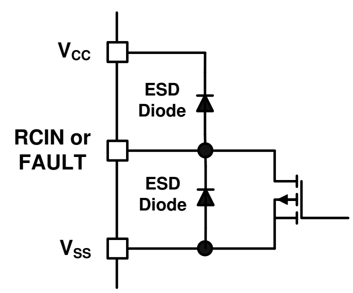
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Input/Output Pin Equivalent Circuit Diagrams

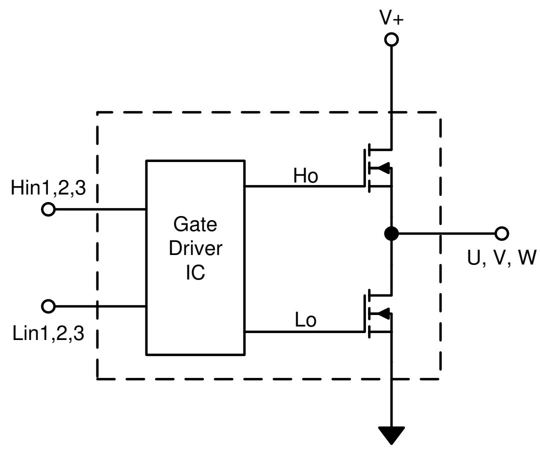








Input-Output Logic Level Table



EN	Itrip	Hin1,2,3	Lin1,2,3	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	off
1	1	X	X	off
0	X	X	X	off

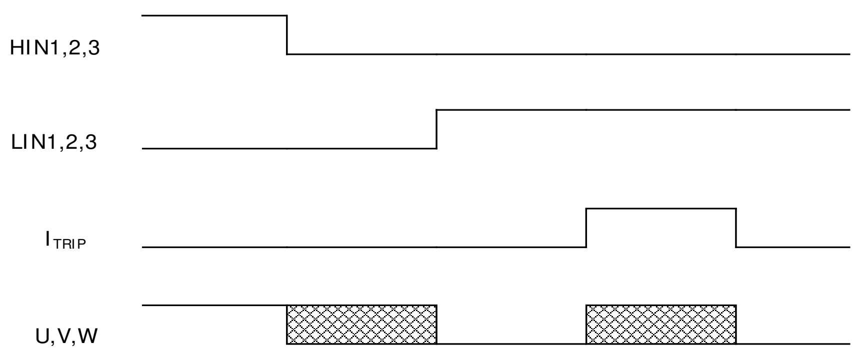


Figure 1: Input/Output Logic Diagram

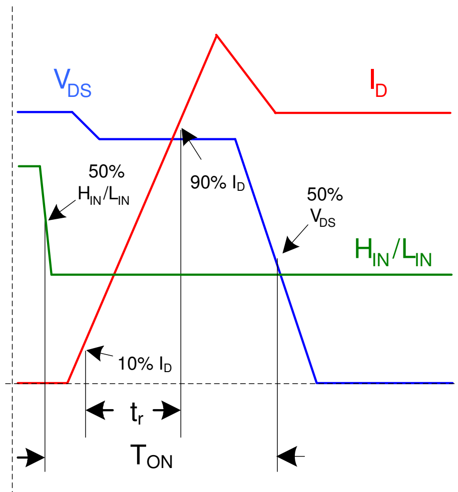


Figure 2a: Input to Output propagation turn-on delay time.

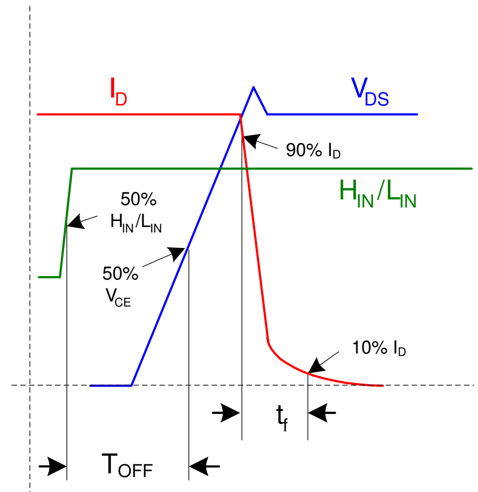


Figure 2b: Input to Output propagation turn-off delay time.

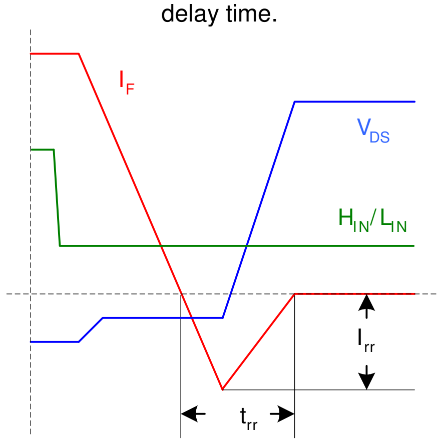


Figure 2c: Diode Reverse Recovery.

Figure 2: Switching Parameter Definitions

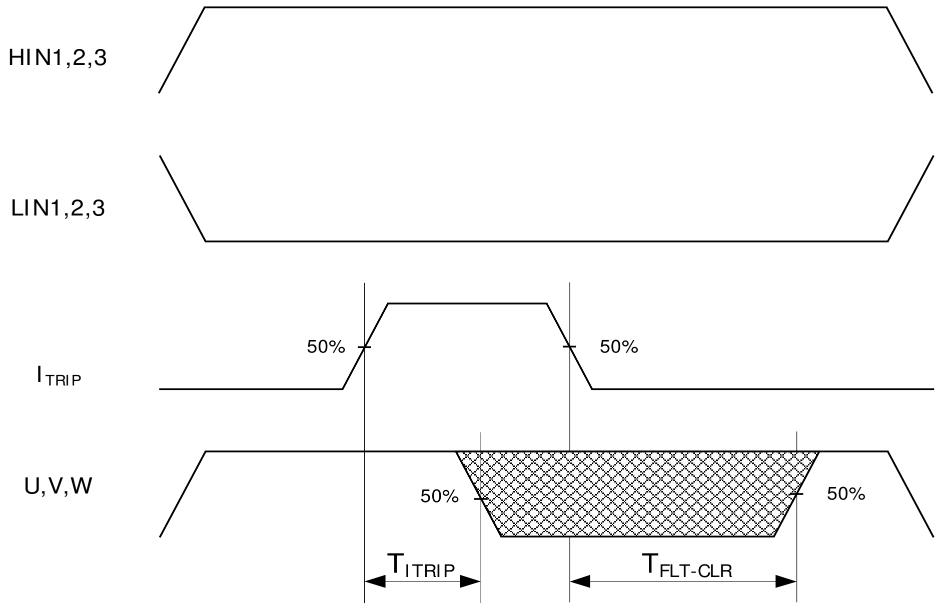
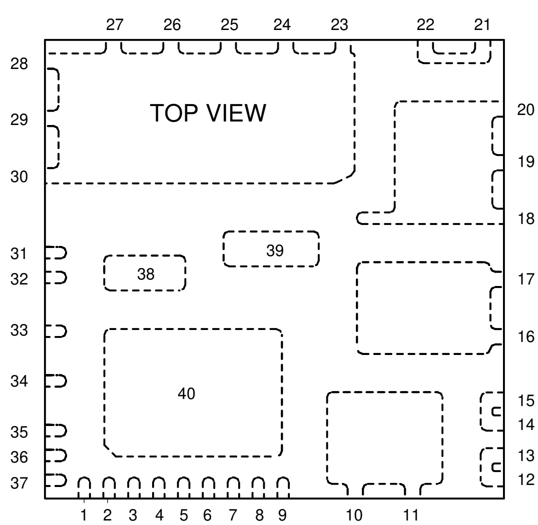


Figure 3: I_{TRIP} Timing Waveform

Module Pin-Out Description

Pin	Name	Description
1	HIN3	Logic Input for High Side Gate Driver - Phase 3
2	LIN1	Logic Input for Low Side Gate Driver - Phase 1
3	LIN2	Logic Input for Low Side Gate Driver - Phase 2
4	LIN3	Logic Input for Low Side Gate Driver - Phase 3
5	/FLT	Fault Output Pin
6	I_{TRIP}	Over-Current Protection Pin
7	EN	Enable Pin
8	RCIN	Reset Programming Pin
9, 40	VSS, COM	Ground for Gate Drive IC and Low Side Gate Drive Return
10, 11, 31, 38	U, VS1	Output 1, High Side Floating Supply Offset Voltage
12, 13	VR1	Phase 1 Low Side FET Source
14, 15	VR2	Phase 2 Low Side FET Source
16, 17, 39	V, VS2	Output 2, High Side Floating Supply Offset Voltage
18, 19, 20	W, VS3	Output 3, High Side Floating Supply Offset Voltage
21, 22	VR3	Phase 3 Low Side FET Source
23-30	V+	DC Bus Voltage Positive
32	VB1	High Side Floating Supply Voltage 1
33	VB2	High Side Floating Supply Voltage 2
34	VB3	High Side Floating Supply Voltage 3
35	VCC	15V Supply
36	HIN1	Logic Input for High Side Gate Driver - Phase 1
37	HIN2	Logic Input for High Side Gate Driver - Phase 2



Notes

Pins 38 and 39 are not required to be connected electrically on the PCB

All pins with the same name are connected internally. Thus, pins 10, 11, 31 and 38 are internally connected

Fault Reporting and Programmable Fault Clear Timer

The IRSM836-045MA provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the IRSM836-045MA to report a fault via the FAULT pin. The first is an under-voltage condition of V_{CC} and the second is when the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 4 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 5 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

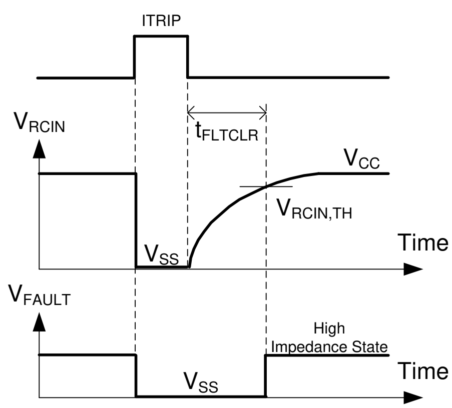


Figure 4: RCIN and FAULT pin waveforms

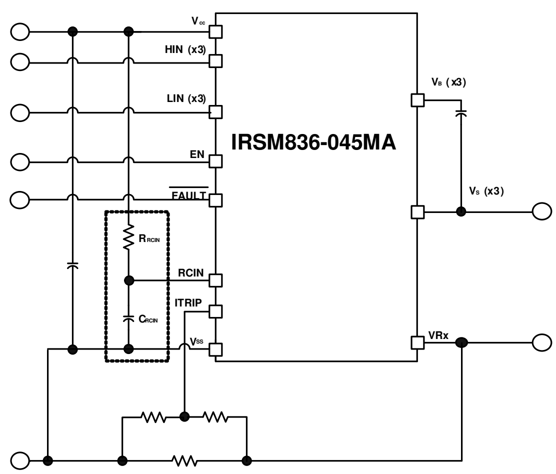


Figure 5: Programming the fault clear timer

The design guidelines for this network are shown in Table 1.

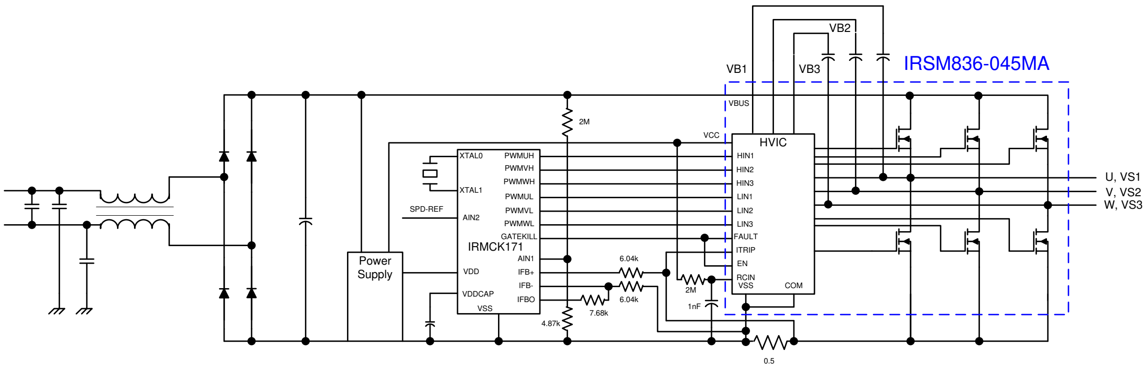
C_{RCIN}	≤1 nF
	Ceramic
R_{RCIN}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 1: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$t_{FLTCLR} = -(R_{RCIN} C_{RCIN}) \ln\left(1 - \frac{V_{RCIN,TH}}{V_{CC}}\right)$$

Typical Application Connection IRSM836-045MA



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide good decoupling between VCC-VSS and VB1,2,3-VS1,2,3 terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on application note AN-1044.
4. PWM generator must be disabled within Fault duration to guarantee shutdown of the system. Over-current condition must be cleared before resuming operation.

Current Capability in a Typical Application

Figure 6 shows the current capability for this module at specified conditions. The current capability of the module is affected by application conditions including the PCB layout, ambient temperature, maximum PCB temperature, modulation scheme, PCB copper thickness and so on. The curves below were obtained from measurements carried out on the IRMCS1471X_R4-1 reference design board which includes the IRSM836-045MA and IR's IRMCK171 digital control IC.

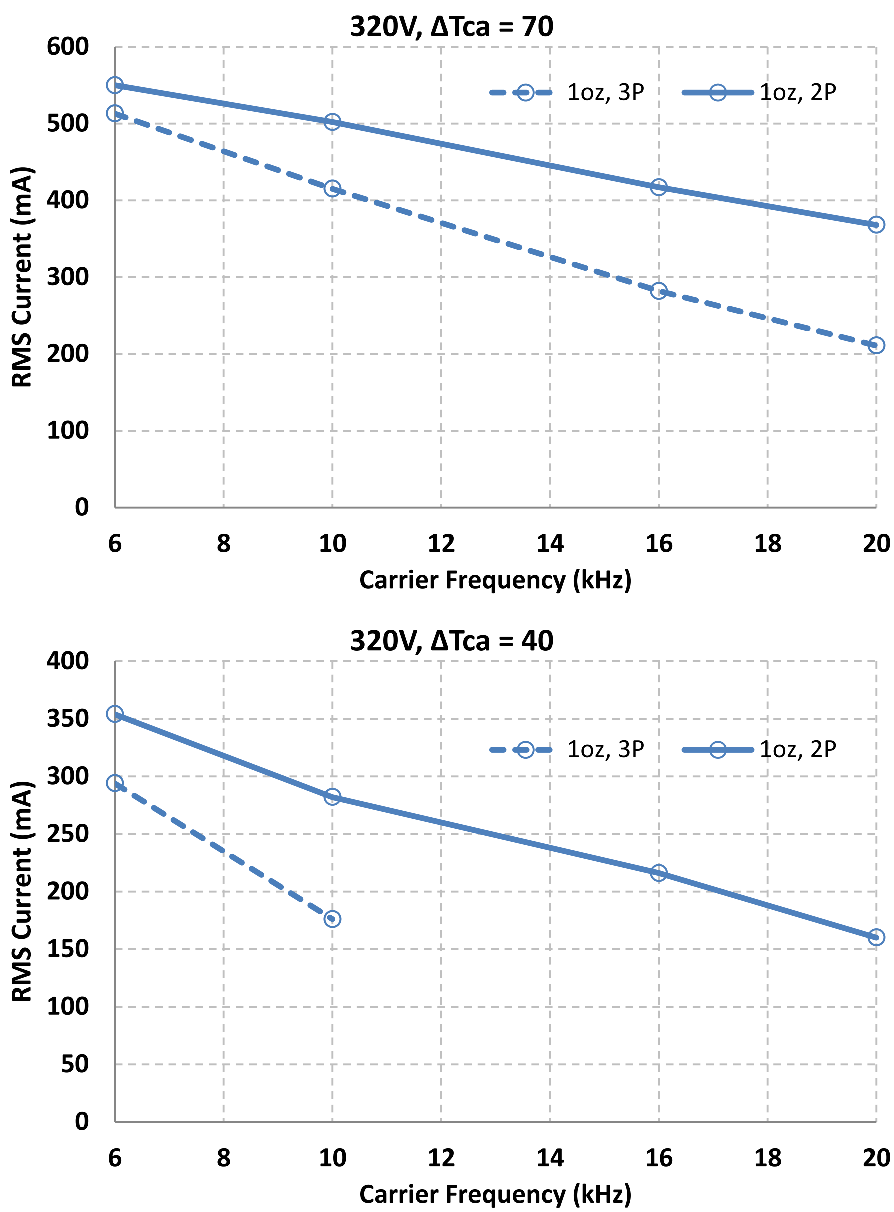


Figure 6: Maximum Sinusoidal Phase Current vs. PWM Switching Frequency
Sinusoidal Modulation, V^{+}=320V, PF=0.98

PCB Example

Figure 7 below shows an example layout for the application PCB. The effective area of the V+ top-layer copper plane is ~3cm² in this example. For an FR4 PCB with 1oz copper, $R_{th(J-A)}$ is about 40°C/W. A lower $R_{th(J-A)}$ can be achieved using thicker copper and/or additional layers.

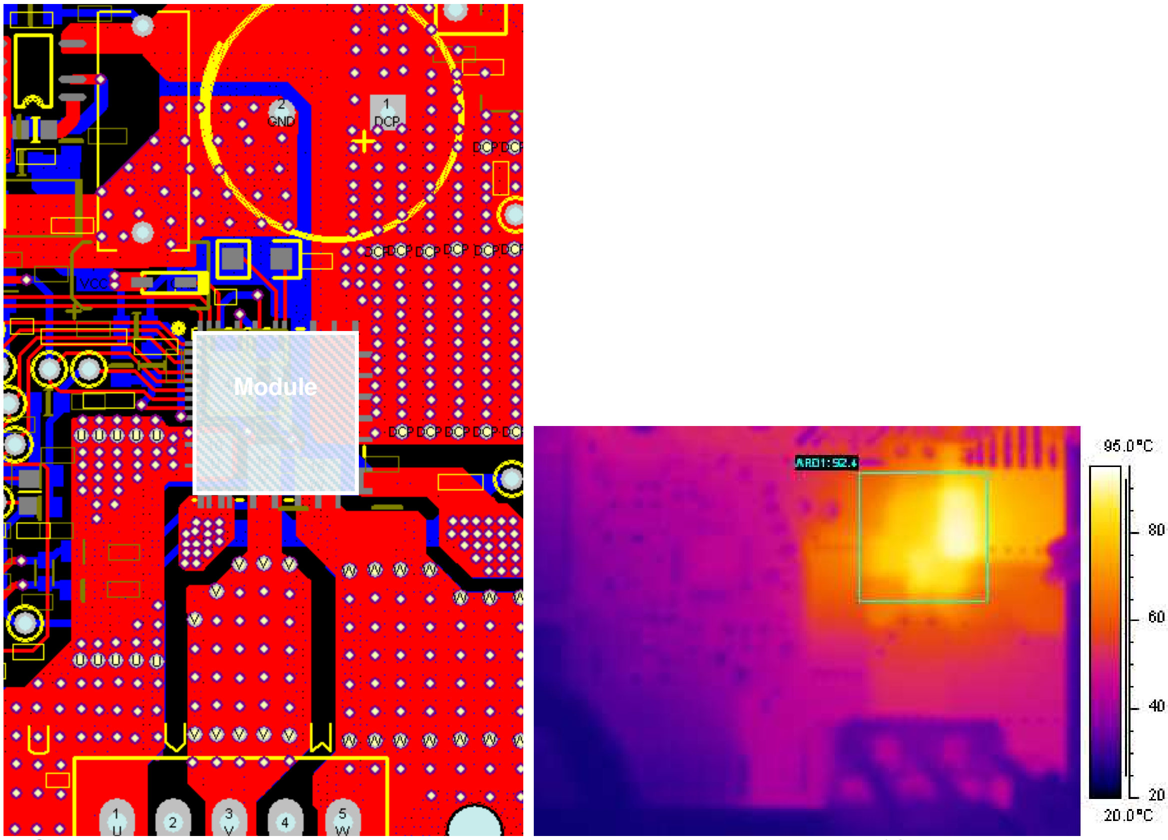
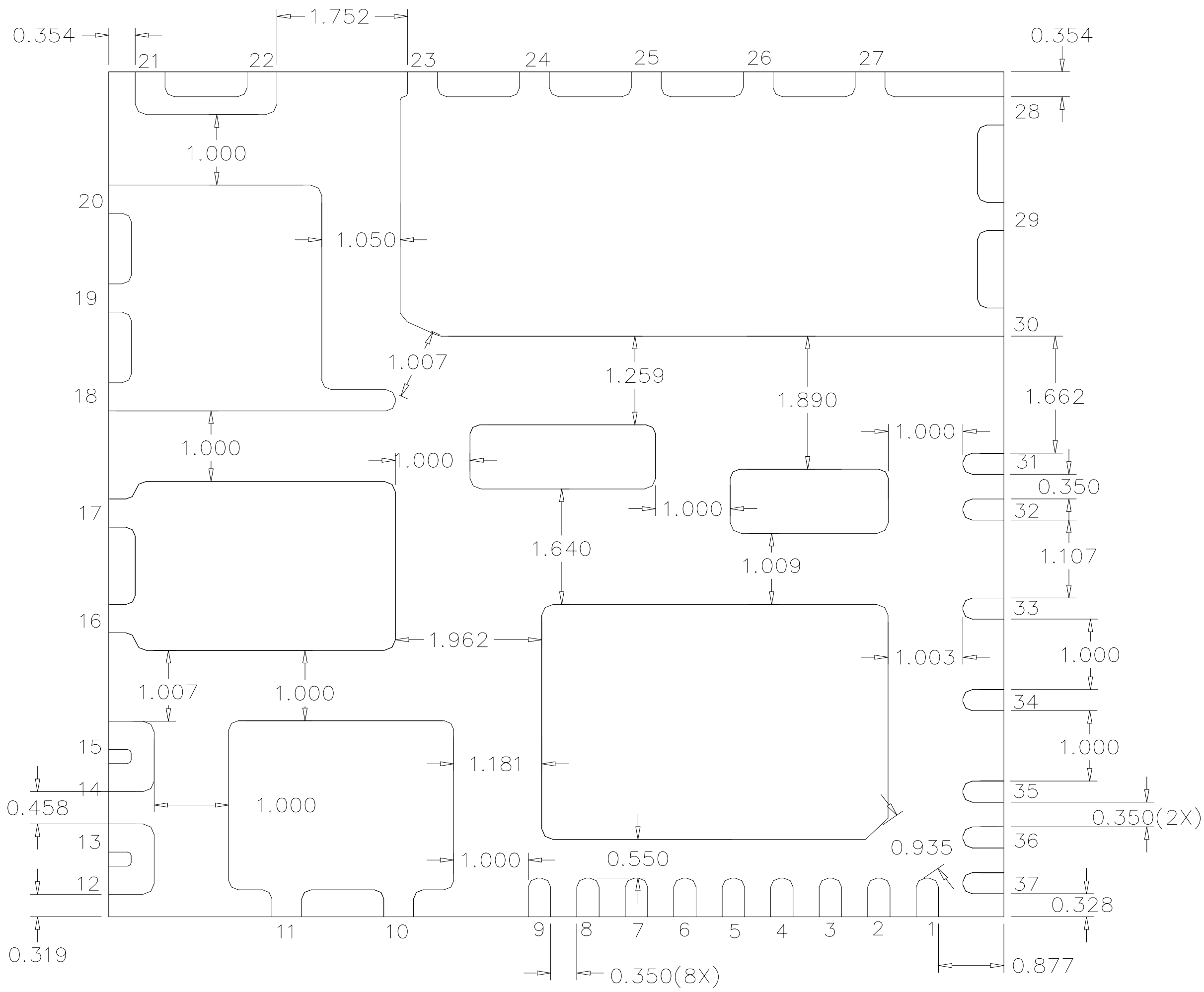


Figure 7: PCB layout example and corresponding thermal image (16kHz, 2P, 1oz, ∆Tca=70°C, V+ = 320V, Iu = 417mArms, Po = 93W)

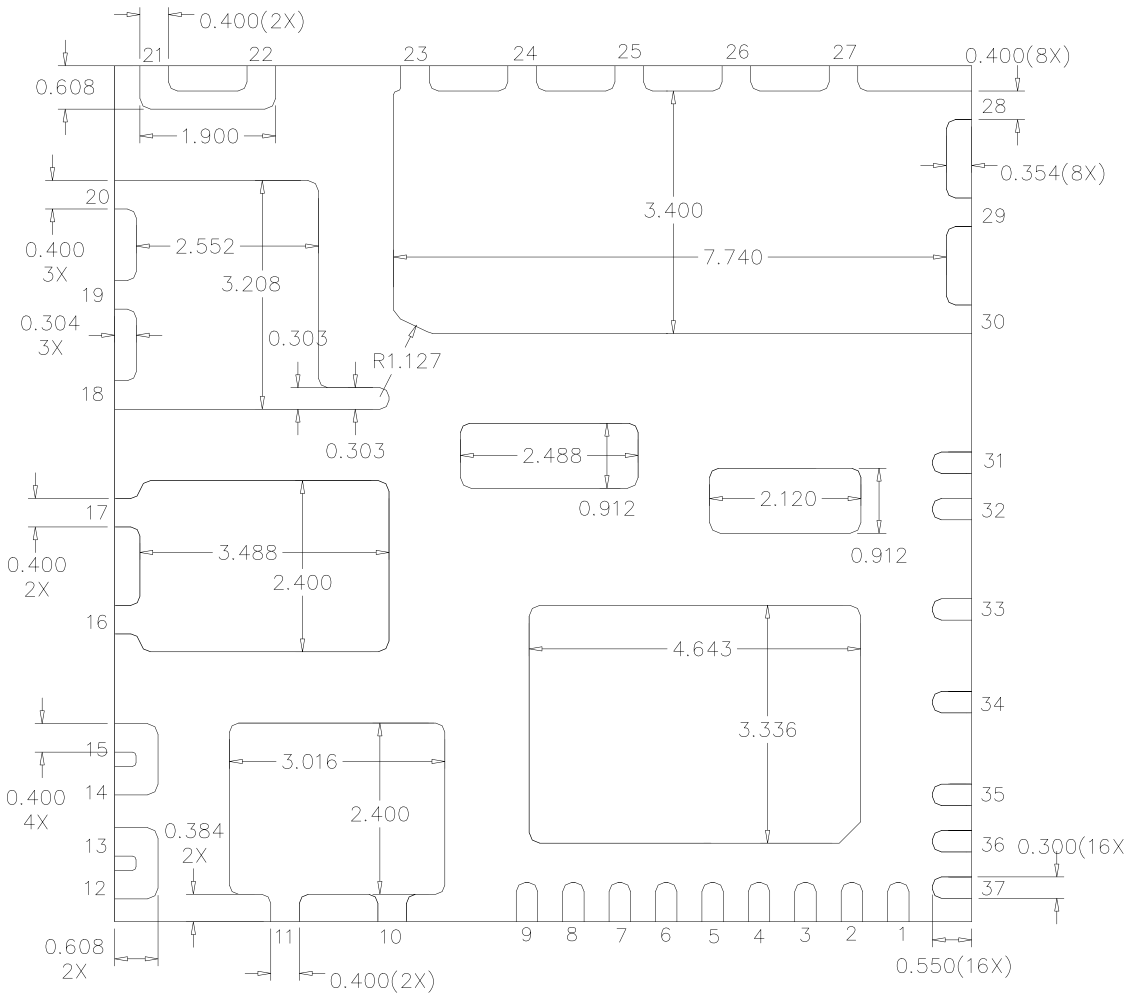
At the module's typical operating conditions, dV/dt of the phase node voltage is influenced by the load capacitance which includes parasitic capacitance of the PCB, MOSFET output capacitance and motor winding capacitance. To turn off the MOSFET, the load capacitance needs to be charged by the phase current. For the IRMCS1171 reference design, turn-off dV/dt ranges from 2 to 5 V/ns depending on the phase current magnitude. Turn-on dV/dt is influenced by PCB parasitic capacitance and motor winding capacitance and typically ranges from 4 to 6 V/ns. The MOSFET turn-on loss combined with the complimentary body diode reverse recovery loss comprises the majority of the total switching losses. Two-phase modulation can be used to reduce switching losses and run the module at higher phase currents.

37L Package Outline IRSM836-045MA (Bottom View)



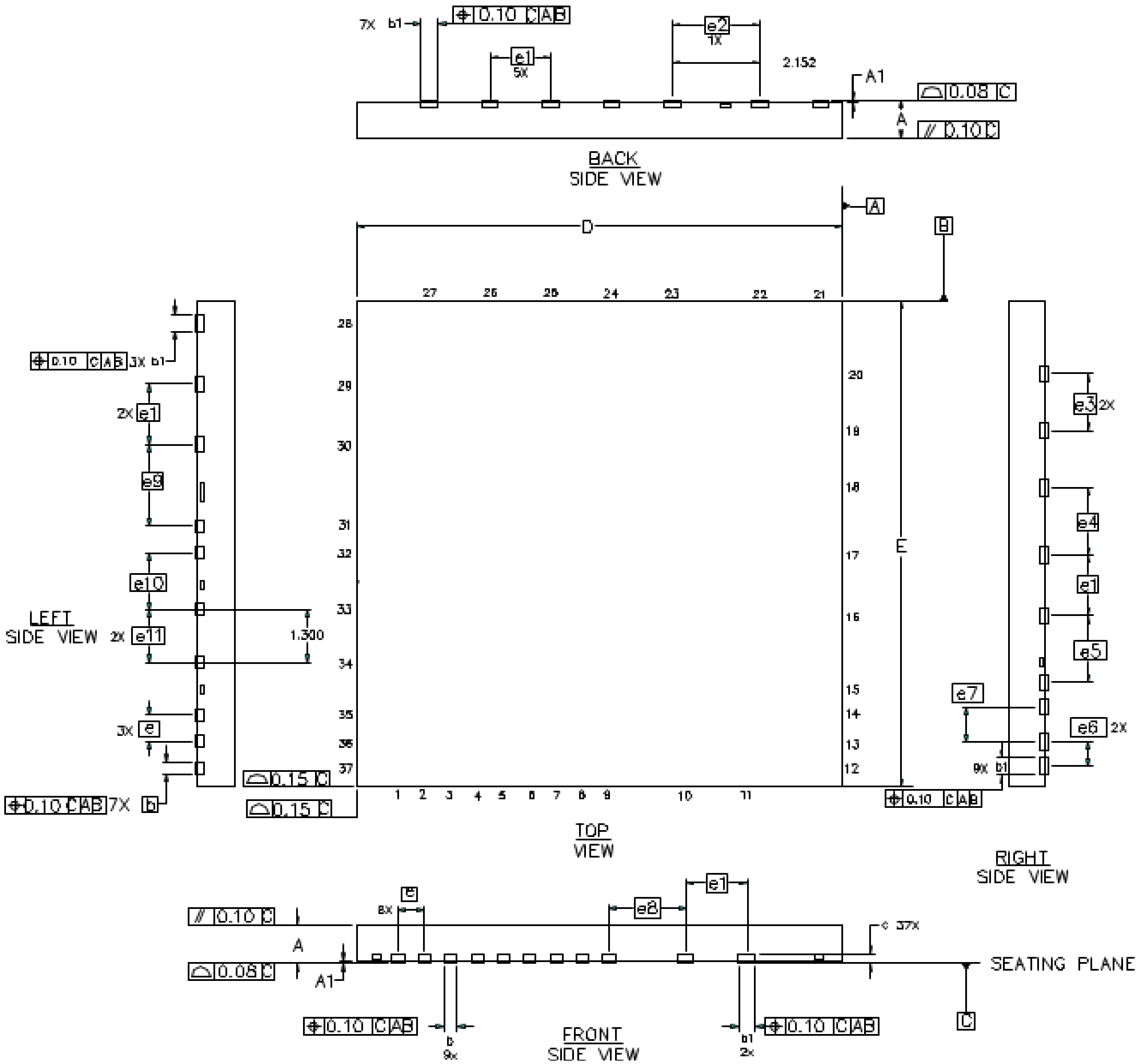
Dimensions in mm

37L Package Outline IRSM836-045MA (Bottom View)



Dimensions in mm

37L Package Outline IRSM836-045MA (Top and Side View)

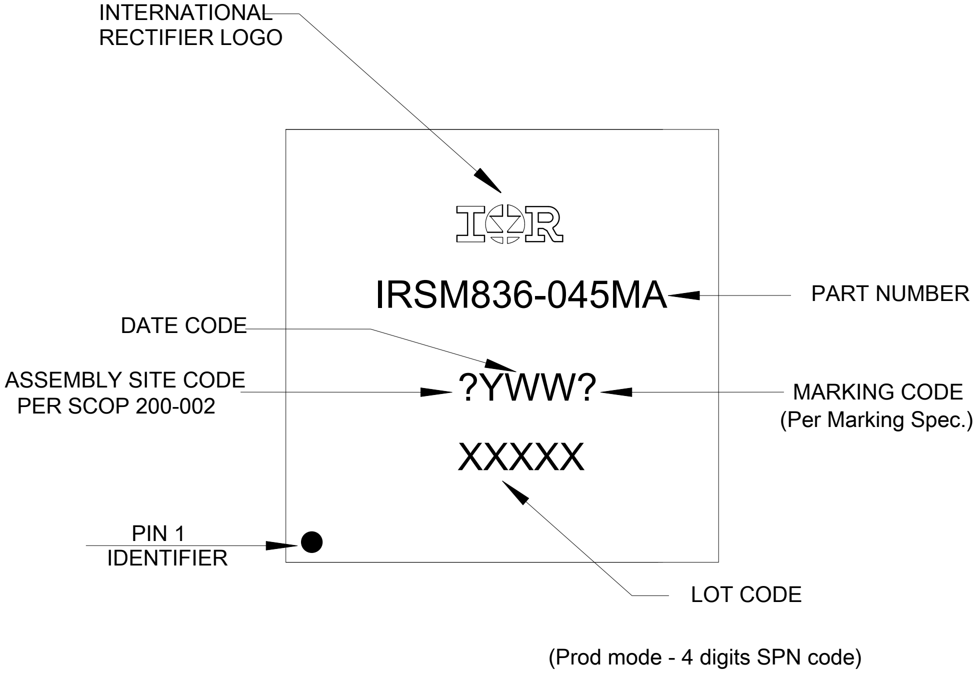


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	-	0.050
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
c	0.203 REF.		
D	11.900	12.000	12.100

DIM	MILLIMETERS		
	MIN	NOM	MAX
E	11.900	12.000	12.100
e	0.650 BASIC		
e1	1.500 BASIC		
e2	2.152 BASIC		
e3	1.404 BASIC		
e4	1.650 BASIC		
e5	1.657 BASIC		

DIM	MILLIMETERS		
	MIN	NOM	MAX
e6	0.600 BASIC		
e7	0.858 BASIC		
e8	1.908 BASIC		
e9	2.012 BASIC		
e10	1.407 BASIC		
e11	1.300 BASIC		

Top Marking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RECTIFIER LOGO
IRSM836-045MA
PART NUMBER
DATE CODE
ASSEMBLY SITE CODE
PER SCOP 200-002
?YWW?
MARKING CODE
(Per Marking Spec.)
XXXXX
PIN 1
IDENTIFIER
LOT CODE
(Prod mode - 4 digits SPN code)

Revision History

January 18, 2013	Formatting corrections; corrected package drawings; added notes about what pins are internally connected; updated ordering table stating all parts are PbF.

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