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IS25LP064A

64Mb

3V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

DATA SHEET

64Mb
3V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

FEATURES

- **Industry Standard Serial Interface**
  - IS25LP064A: 64Mbit/8Mbyte
  - 256 bytes per Programmable Page
  - Supports standard SPI, Fast, Dual, Dual I/O, Quad, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
  - Supports Double Transfer Rate (DTR)
  - Supports Serial Flash Discoverable Parameters (SFDP)(4)

- **High Performance Serial Flash (SPI)**
  - 133Mhz Fast Read at Vcc=2.7V to 3.6V
  - 104Mhz Fast Read at Vcc=2.3V to 3.6V
  - 532MHz equivalent at QPI operation
  - 50MHz Normal Read
  - DTR (Dual Transfer Rate) up to 66MHz
  - Selectable dummy cycles
  - Configurable drive strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles
  - More than 20-year data retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 bytes per page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous Read 8/16/32/64-Byte burst Wrap
  - Selectable burst length
  - QPI for reduced instruction overhead

- **Low Power with Wide Temp. Ranges**
  - Single 2.3V to 3.6V Voltage Supply
  - 5 mA Active Read Current (typ.)
  - 10 µA Standby Current (typ.)
  - 5 µA Deep Power Down (typ.)
  - Temp Grades:
    Extended: -40°C to +105°C
    Auto Grade (A3): -40°C to +125°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Power Supply lock protect
  - 4x256-Byte dedicated security area with OTP user-lockable bits
  - 128 bit Unique ID for each device (Call Factory)

- **Industry Standard Pin-out & Packages(1),(2)**
  - B = 8-pin SOIC 208mil
  - T = 8-contact USON 4x3mm
  - E = 8-contact XSON 4x4mm
  - K = 8-contact WSON 6x5mm
  - L = 8-contact WSON 8x6mm
  - M = 16-pin SOIC 300mil(3)
  - G= 24-ball TFBGA 6x8mm 4x6(3)
  - H = 24-ball TFBGA 6x8mm 5x5 (Call Factory)(3)
  - KGD (Call Factory)

Notes:
1. Call Factory for other package options available.
2. For the RESET# pin option instead of HOLD# pin, call Factory.
3. For the dedicated RESET# option, see the Ordering Information

GENERAL DESCRIPTION

The IS25LP064A Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash are for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66Mbytes/s of data throughput. The IS25xP series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256-bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

GLOSSARY

Standard SPI

In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Instructions are sent via the SI pin to encode instructions, addresses, or input data to the device on the rising edge of SCK. The SO pin is used to read data or to check the status of the device. This device supports SPI bus operation modes (0,0) and (1,1).

Multi I/O SPI

Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, Quad Output, and Quad Input and Output capability. Executing these instructions through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

QPI

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the enter QPI (35h) instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the instruction code thus requiring only two serial clocks. This can significantly reduce the SPI instruction overhead and improve system performance. Only QPI mode or SPI/Dual/Quad mode can be active at any given time. Enter QPI (35h) and Exit QPI (F5h) instructions are used to switch between these two modes, regardless of the non-volatile Quad Enable (QE) bit status in the Status Register. Power Reset or Hardware/Software Reset will return the device into the standard SPI mode. SI and SO pins become bidirectional I/O0 and I/O1, and WP# and HOLD# pins become I/O2 and I/O3 respectively during QPI mode.

DTR

In addition to SPI and QPI features, the device also supports Fast READ DTR operation, which allows high data throughput while running at lower clock frequencies. DTR READ mode uses both rising and falling edges of the clock to drive output, resulting in reducing input and output cycles by half.

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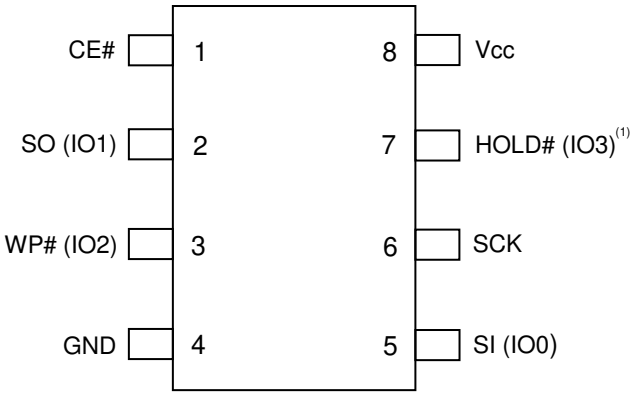
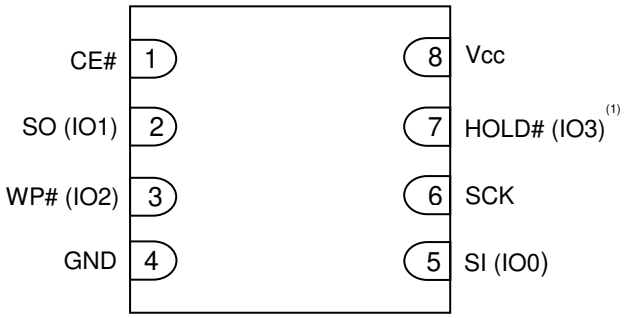
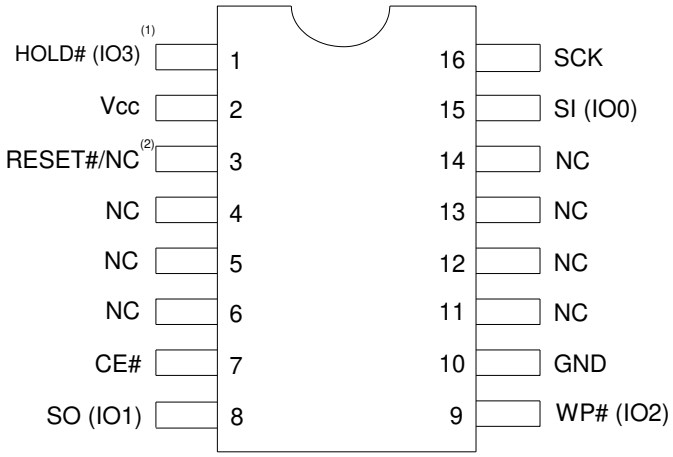
1. PIN CONFIGURATION



8-pin SOIC 208mil

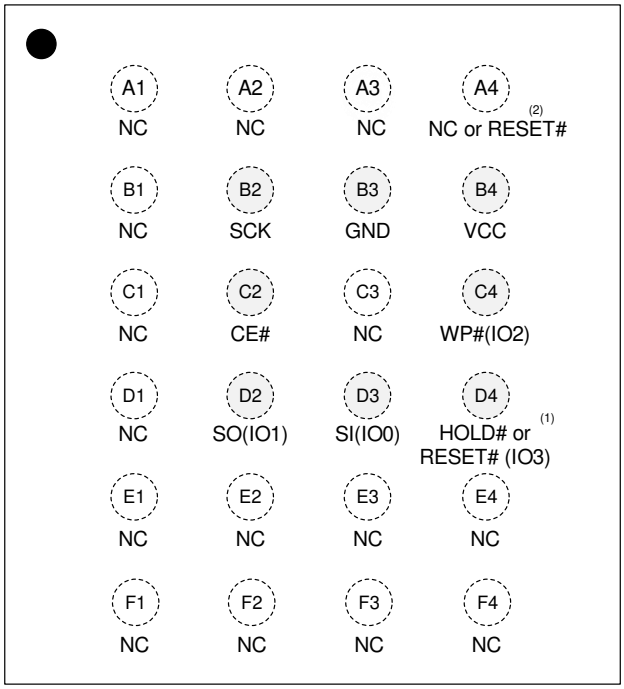


8-contact WSON 6x5mm
8-contact WSON 8x6mm
8-contact XSON 4x4mm
8-contact USON 4x3mm



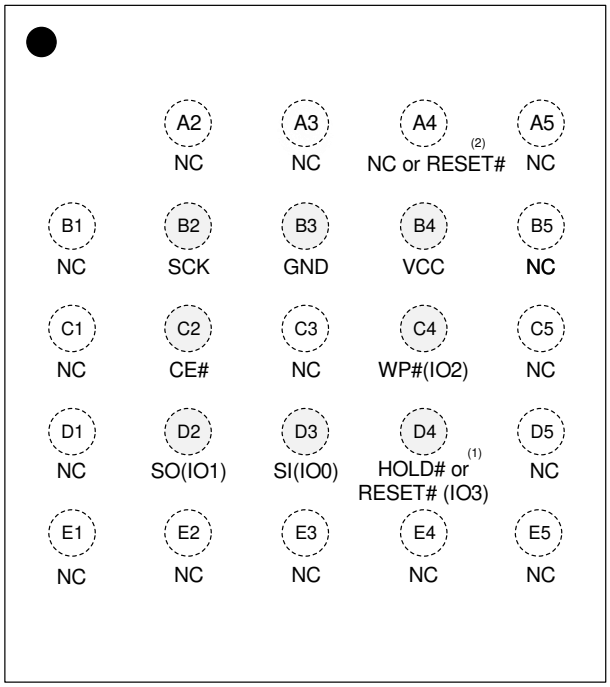
16-pin SOIC 300mil

Top View, Balls Facing Down



24-ball TFBGA, 4x6 Ball Array (Package:G)

Top View, Balls Facing Down



24-ball TFBGA, 5x5 Ball Array (Package:H)

Notes:

1. **For RESET# (IO3) pin (or ball) option instead of HOLD# (IO3) pin (or ball), call Factory.**
2. **In case of 16-pin SOIC and 24-ball TFBGA packages, pin3/ball A4 will become NC or RESET# based on part number. Below is the summary. Also see the Ordering Information.**

	Standard(1)	Dedicated RESET#(2)
Pin3 or Ball A4	**NC**	**RESET#**
Pin1or Ball D4	**Hold#(IO3) or RESET#(IO3)**	**Hold#(IO3)**
Part Number Option	**J or S**	**R or P**

2. PIN DESCRIPTIONS

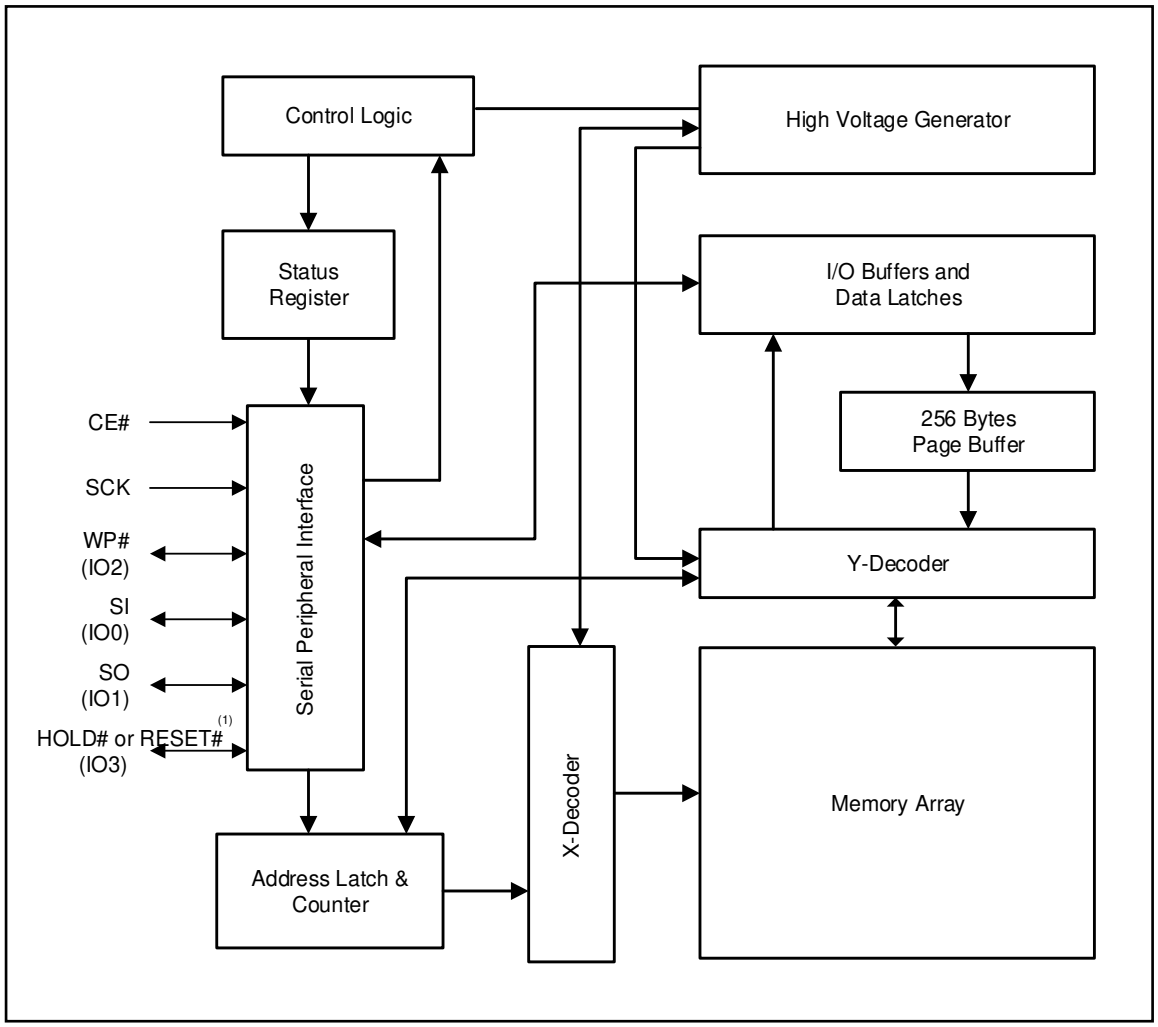
For the device without dedicated RESET#

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to "1" and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to "0", the Status Register is not write-protected regardless of WP# state. When the QE bit is set to "1", the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3) or RESET# (IO3)	INPUT/OUTPUT	**HOLD# (IO3) or RESET#/ (IO3):** When the QE bit of Status Register is set to "1", HOLD# pin or RESET# is not available since it becomes IO3. When QE=0 the pin acts as HOLD# or RESET#. **The pin defaults HOLD#.** **RESET# (IO3) pin instead of HOLD# (IO3) can be supported by optional part (Call Factory).** The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. In optional device, RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled "NC" stand for "No Connect" and should be left uncommitted.

For the device with dedicated RESET#

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Same as the description in previous page
SI (IO0), SO (IO1)	INPUT/OUTPUT	Same as the description in previous page
WP# (IO2)	INPUT/OUTPUT	Same as the description in previous page
HOLD# (IO3)	INPUT/OUTPUT	**Hold/Serial Data IO (IO3):** When the QE bit of Status Register is set to "1", HOLD# pin is not available since it becomes IO3. When QE=0 the pin acts as HOLD#. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state.
RESET#	INPUT/OUTPUT	**RESET:** Dedicated RESET# function is available only for specific parts. The RESET# pin (or ball) will be independent of the QE bit of Status Register. The RESET# is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. It has an internal pull-up resistor and may be left floating if not used.
SCK	INPUT	Same as the description in previous page
Vcc	POWER	Same as the description in previous page
GND	GROUND	Same as the description in previous page
NC	Unused	Same as the description in previous page

3. BLOCK DIAGRAM



Note1: For RESET# (IO3) pin option instead of HOLD# (IO3) pin, call Factory. In case of device with dedicated RESET# function, RESET# is on pin3/ball A4. See the Ordering Information for the dedicated RESET# option.

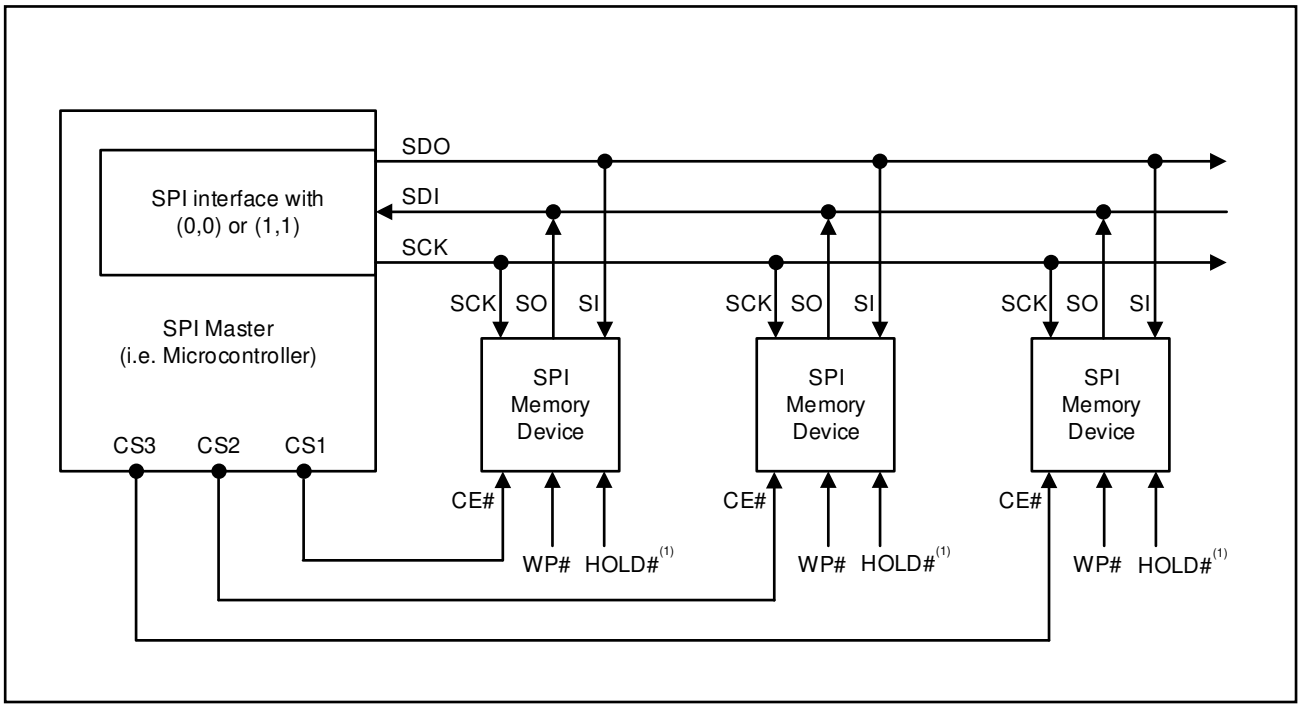
4. SPI MODES DESCRIPTION

Multiple IS25LP064A devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:
1. **For RESET# (IO3) option instead of HOLD# (IO3), call Factory.**
2. **SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during QPI mode.**

Figure 4.2 SPI Mode Support

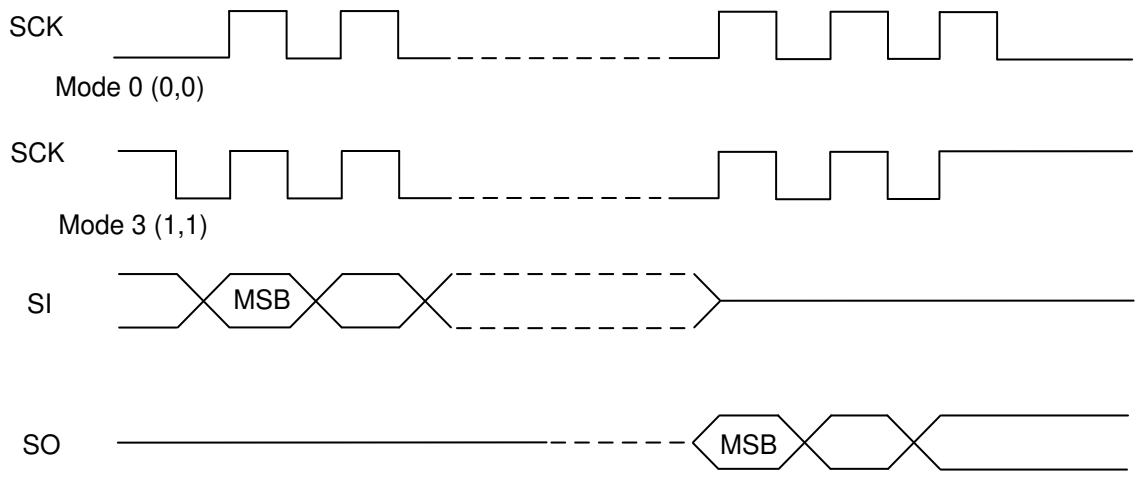
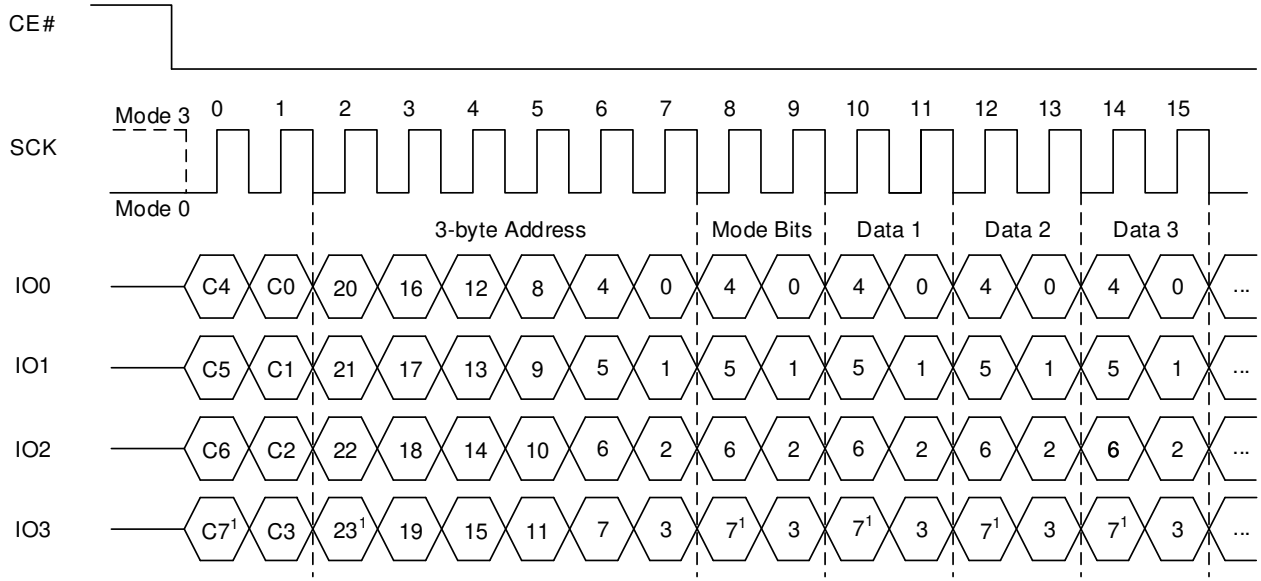


Figure 4.3 QPI Mode Support



Note1: MSB (Most Significant Bit)

5. SYSTEM CONFIGURATION

The memory array of the IS25LP064A is divided into uniform 4 Kbyte sectors or uniform 32/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses of IS25LP064A/032A

Memory Density	Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
64Mb	Block 0	Block 0	Sector 0	4	000000h – 000FFFh
			:	:	:
		Block 1	:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Block 2	Sector 16	4	010000h – 010FFFh
			:	:	:
		Block 3	:	:	:
			Sector 31	4	01F000h - 01FFFFh
	Block 2	Block 4	Sector 32	4	020000h – 020FFFh
			:	:	:
		Block 5	:	:	:
			Sector 47	4	02F000h – 02FFFFh
	:	:	:	:	:
	Block 63	Block 126	Sector 1008	4	3F0000h – 3F0FFFh
			:	:	:
		Block 127	:	:	:
			Sector 1023	4	3FF000h – 3FFFFFh
	:	:	:	:	:
	Block 127	Block 254	Sector 2032	4	7F0000h – 7F0FFFh
			:	:	:
		Block 255	:	:	:
			Sector 2047	4	7FF000h – 7FFFFFh

6. REGISTERS

The device has various sets of Registers: Status, Function, and Read.
When the register is read continuously, the same byte is output repeatedly until CE# goes HIGH.

6.1 STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Table 6.1 & Table 6.2.

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W[1]	Volatile
Bit 2	BP0	Block Protection Bit: (See Table 6.4 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Non-Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Non-Volatile
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Non-Volatile

Note1: WEL bit can be written by WREN and WRDI commands, but cannot by WRSR command.

The BP0, BP1, BP2, BP3, QE, and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP0, BP1, BP2, BP3, QE, and SRWD bits were set to “0” at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for write Status Register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled and the write operations described in Table 6.3 are inhibited. When the WEL bit is “1”, the write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction except for Set Read Register must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any write operation.

Table 6.3 Instructions requiring WREN instruction ahead

Instructions must be preceded by the WREN instruction		
Name	**Hex Code**	**Operation**
PP	02h	Serial Input Page Program
PPQ	32h/38h	Quad Input Page Program
SER	D7h/20h	Sector Erase
BER32 (32Kb)	52h	Block Erase 32K
BER64 (64Kb)	D8h	Block Erase 64K
CER	C7h/60h	Chip Erase
WRSR	01h	Write Status Register
WRFR	42h	Write Function Register
IRER	64h	Erase Information Row
IRP	62h	Program Information Row

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the Status Register that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD# pin is tied directly to the power supply.

Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits

Status Register Bits				Protected Memory Area (IS25LP064A, 128Blocks)	
BP3	**BP2**	**BP1**	**BP0**	**TBS(T/B selection) = 0, Top area**	**TBS(T/B selection) = 1, Bottom area**
0	0	0	0	0(None)	0(None)
0	0	0	1	1(1 block : 127th)	1(1 block : 0th)
0	0	1	0	2(2 blocks : 126th and 127th)	2(2 blocks : 0th and 1st)
0	0	1	1	3(4 blocks : 124th to 127th)	3(4 blocks : 0th to 3rd)
0	1	0	0	4(8 blocks : 120th to 127th)	4(8 blocks : 0th to 7th)
0	1	0	1	5(16 blocks : 112nd to 127th)	5(16 blocks : 0th to 15th)
0	1	1	0	6(32 blocks : 96th to 127th)	6(32 blocks : 0th to 31st)
0	1	1	1	7(64 blocks : 64th to 127th)	7(64 blocks : 0th to 63rd)
1	x	x	x	8~15(128 blocks : 0th to 127th) All blocks	8~15(128 blocks : 0th to 127th) All blocks

Note: x is don't care

6.2 FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and Table 6.6.

Table 6.5 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0	ESUS	PSUS	TBS	Reserved
Default	0	0	0	0	0	0	0	0

Table 6.6 Function Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	Reserved	Reserved	R	Reserved
Bit 1	Top/Bottom Selection	Top/Bottom Selection. (See Table 6.4 for details) “0” indicates Top area. “1” indicates Bottom area.	R/W	OTP
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	Volatile
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
Bit 4	IR Lock 0	Lock the Information Row 0: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 5	IR Lock 1	Lock the Information Row 1: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 6	IR Lock 2	Lock the Information Row 2: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 7	IR Lock 3	Lock the Information Row 3: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP

Note: Once OTP bits of Function Register are written to “1”, it cannot be modified to “0” any more.

Top/Bottom Selection: BP0~3 area assignment can be changed from Top (default) to Bottom by setting TBS bit to “1”. However, once Bottom is selected, it cannot be changed back to Top since TBS bit is OTP. See Table 6.4 for details

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to “1” after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to “0”.

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is “1” after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to “0”.

IR Lock bit 0 ~ 3: The default is “0” so that the Information Row can be programmed. If the bit set to “1”, the Information Row can’t be programmed. Once it set to “1”, it cannot be changed back to “0” since IR Lock bits are OTP.

6.3 READ REGISTER

Read Register format and Bit definitions pertaining to QPI mode are described below.

READ PARAMETER BITS

Table 6.7 defines all bits that control features in SPI/QPI modes. The ODS2, ODS1, ODS0 (P7, P6, P5) bits provide a method to set and control driver strength. The Dummy Cycle bits (P4, P3) define how many dummy cycles are used during various READ modes. The wrap selection bits (P2, P1, P0) define burst length with wrap around.

The SET READ PARAMETERS Operation (SRP, C0h) is used to set all the Read Register bits, and can thereby define the output driver strength, number of dummy cycles used during READ modes, burst length with wrap around.

Table 6.7 Read Parameter Table

	P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
	ODS2	ODS1	ODS0	Dummy Cycles	Dummy Cycles	Wrap Enable	Burst Length	Burst Length
Default (Volatile)	1	1	1	0	0	0	0	0

Table 6.8 Burst Length Data

	P1	**P0**
8 bytes	0	0
16 bytes	0	1
32 bytes	1	0
64 bytes	1	1

Table 6.9 Wrap Function

Wrap around boundary	**P2**
Whole array regardless of P1 and P0 value	0
Burst Length set by P1 and P0	1

Table 6.10 Read Dummy Cycles vs Max Frequency

Read Modes	P4,P3 = 00 (Default)	P4,P3 = 01	P4,P3 = 10	P4,P3 = 11	Remark	Mode
Normal Read 03h	0	0	0	0	Max. 50MHz	SPI
Fast Read [2] 0Bh	8	8	8	8	Max. 133MHz[1]	SPI
	6 (104MHz)	4 (84MHz)	8[1] (133MHz)	10[1] (133MHz)		QPI
Fast Read DTR 0Dh	4	4	4	4	Max.66MHz	SPI
	3 (51MHz)	2 (38MHz)	4 (64MHz)	5 (66MHz)		QPI
Fast Read Dual Output 3Bh	8	8	8	8	Max. 133MHz[1]	SPI
Fast Read Dual IO BBh	4 (104MHz)	4 (104MHz)	8[1] (133MHz)	8[1] (133MHz)		SPI
Fast Read Dual IO DTR BDh	2 (52MHz)	2 (52MHz)	4 (66MHz)	4 (66MHz)		SPI
Fast Read Quad Output 6Bh	8	8	8	8	Max. 133MHz[1]	SPI
Fast Read Quad IO EBh	6 (104MHz)	4 (84MHz)	8[1] (133MHz)	10[1] (133MHz)		SPI , QPI
Fast Read Quad IO DTR EDh	3 (51MHz)	2 (38MHz)	4 (64MHz)	5 (66MHz)		SPI , QPI

Notes:

1. **Max frequency is 133 MHz at Vcc=2.7V~3.6V and 104MHz at Vcc=2.3V~3.6V.**
2. **RDUID, RDSFDP, IRRD instructions are also applied.**
3. **Dummy cycles in the table are including Mode bit cycles.**
4. **Must satisfy bus I/O contention. For instance, if the number of dummy cycles and AX bit cycles are same, then X must be Hi-Z.**

Table 6.11 Driver Strength Table

ODS2	ODS1	ODS0	Description	Remark
0	0	0	Reserved	
0	0	1	12.50%	
0	1	0	25%	
0	1	1	37.50%	
1	0	0	Reserved	
1	0	1	75%	
1	1	0	100%	
1	1	1	50%	Default

7. PROTECTION MODE

The IS25LP064A supports hardware and software write-protection mechanisms.

7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, SRWD, and QE in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage (V_{WI}) is specified in the section 9.8 POWER-UP AND POWER-DOWN. All write sequence will be ignored when Vcc drops to V_{WI}.

Table 7.1 Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Note: Before the execution of any program, erase or write Status/Function Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

7.2 SOFTWARE WRITE PROTECTION

The IS25LP064A also provides a software write protection feature. The Block Protection (TBS, BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

8. DEVICE OPERATION

The IS25LP064A utilizes an 8-bit instruction register. Refer to Table 8.1. Instruction Set for details on instructions and instruction codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI) or Serial Data IOs (IO0, IO1, IO2, IO3). The input data on SI or IOs is latched on the rising edge of Serial Clock (SCK) for normal mode and both of rising and falling edges for DTR mode after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in to end the operation.

Table 8.1 Instruction Set

Instruction Name	Operation	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
NORD	Normal Read Mode	SPI	03h	A <23:16>	A <15:8>	A <7:0>	Data out		
FRD	Fast Read Mode	SPI QPI	0Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Data out	
FRDIO	Fast Read Dual I/O	SPI	BBh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	AXh(1),(2) Dual	Dual Data out	
FRDO	Fast Read Dual Output	SPI	3Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Dual Data out	
FRQIO	Fast Read Quad I/O	SPI QPI	EBh	A <23:16> Quad	A <15:8> Quad	A <7:0> Quad	AXh(1), (2) Quad	Quad Data out	
FRQO	Fast Read Quad Output	SPI	6Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Quad Data out	
FRDTR	Fast Read DTR Mode	SPI QPI	0Dh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Dual Data out	
FRDDTR	Fast Read Dual I/O DTR	SPI	BDh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	AXh(1), (2) Dual	Dual Data out	
FRQDTR	Fast Read Quad I/O DTR	SPI QPI	EDh	A <23:16>	A <15:8>	A <7:0>	AXh(1), (2) Quad	Quad Data out	
PP	Input Page Program	SPI QPI	02h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
PPQ	Quad Input Page Program	SPI	32h 38h	A <23:16>	A <15:8>	A <7:0>	Quad PD (256byte)		
SER	Sector Erase	SPI QPI	D7h 20h	A <23:16>	A <15:8>	A <7:0>			
BER32 (32Kb)	Block Erase 32K	SPI QPI	52h	A <23:16>	A <15:8>	A <7:0>			
BER64 (64Kb)	Block Erase 64K	SPI QPI	D8h	A <23:16>	A <15:8>	A <7:0>			
CER	Chip Erase	SPI QPI	C7h 60h						
WREN	Write Enable	SPI QPI	06h						
WRDI	Write Disable	SPI QPI	04h						
RDSR	Read Status Register	SPI QPI	05h	SR					
WRSR	Write Status Register	SPI QPI	01h	WSR Data					

Instruction Name	Operation	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
RDFR	Read Function Register	SPI QPI	48h	Data out					
WRFR	Write Function Register	SPI QPI	42h	WFR Data					
QPIEN	Enter QPI mode	SPI	35h						
QPIDI	Exit QPI mode	QPI	F5h						
PERSUS	Suspend during program/erase	SPI QPI	75h B0h						
PERRSM	Resume program/erase	SPI QPI	7Ah 30h						
DP	Deep Power Down	SPI QPI	B9h						
RDID, RDPD	Read ID / Release Power Down	SPI QPI	ABh	XXh(3)	XXh(3)	XXh(3)	ID7-ID0		
SRP	Set Read Parameters	SPI QPI	C0h	Data in					
RDJDID	Read JEDEC ID Command	SPI QPI	9Fh	MF7-MF0	ID15-ID8	ID7-ID0			
RDMDID	Read Manufacturer & Device ID	SPI QPI	90h	XXh(3)	XXh(3)	00h	MF7-MF0	ID7-ID0	
						01h	ID7-ID0	MF7-MF0	
RDJDIDQ	Read JEDEC ID QPI mode	QPI	AFh	MF7-MF0	ID15-ID8	ID7-ID0			
RDUID	Read Unique ID	SPI QPI	4Bh	A(4) <23:16>	A(4) <15:8>	A(4) <7:0>	Dummy Byte	Data out	
RDSFDP	SFDP Read	SPI QPI	5Ah	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Data out	
NOP	No Operation	SPI QPI	00h						
RSTEN	Software Reset Enable	SPI QPI	66h						
RST	Software Reset	SPI QPI	99h						
IRER	Erase Information Row	SPI QPI	64h	A <23:16>	A <15:8>	A <7:0>			
IRP	Program Information Row	SPI QPI	62h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
IRRD	Read Information Row	SPI QPI	68h	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Data out	
SECUN-LOCK	Sector Unlock	SPI QPI	26h	A <23:16>	A <15:8>	A <7:0>			
SECLOCK	Sector Lock	SPI QPI	24h						

Notes:
1. **The number of dummy cycles depends on the value setting in the Table 6.10 Read Dummy Cycles.**
2. **AXh has to be counted as a part of dummy cycles. X means "don't care".**
3. **XX means "don't care".**
4. **A<23:9> are "don't care" and A<8:4> are always "0".**

8.1 NORMAL READ OPERATION (NORD, 03h)

The NORMAL READ (NORD) instruction is used to read memory contents of the IS25LP064A at a maximum frequency of 50MHz.

The NORD instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{MSB} (most significant bit) - A_0 are decoded. The remaining bits (A23 – A_{MSB+1}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

The first byte data (D7 - D0) is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one NORMAL READ instruction. The address is automatically incremented by one after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

If the NORMAL READ instruction is issued while an Erase, Program or Write operation is in process (WIP=1) the instruction is ignored and will not have any effects on the current operation.

Table 8.2 Address Key

Address	IS25LP064A
A_{MSB} – A_0	A23 - A0 (A23=X)

X=Don't Care