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IS25LP128
IS25LP064
IS25LP032

32/64/128M-BIT
3V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

DATA SHEET

32/64/128M-BIT

3V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

FEATURES

- **Industry Standard Serial Interface**
  - IS25LP128: 128M-bit/16M-byte
  - IS25LP064: 64M-bit/8M-byte
  - IS25LP032: 32M-bit/4M-byte
  - 256 bytes per Programmable Page
  - Supports standard SPI, Fast, Dual, Dual I/O, QPI, SPI DTR, Dual SPI DTR I/O, and QPI
  - Double Transfer Rate (DTR) option
  - Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**
  - 50MHz Normal and 133Mhz Fast Read
  - 532 MHz equivalent QPI
  - DTR (Dual Transfer Rate) up to 66MHz
  - Selectable dummy cycles
  - Configurable drive strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles
  - More than 20-year data retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform: Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 bytes per page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous Read 8/16/32/64-Byte burst
  - Selectable burst length
  - QPI for reduced instruction overhead

- **Low Power with Wide Temp. Ranges**
  - Single 2.3V to 3.6V Voltage Supply
  - 10 mA Active Read Current
  - 10 µA Standby Current
  - 5 µA Deep Power Down
  - Temp Grades:
    Extended: -40°C to +105°C
    V Grade: -40°C to +125°C
    Auto Grade: up to +125°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Power Supply lock protect
  - 4x256-Byte dedicated security area with user-lockable bits, (OTP) One Time Programmable Memory
  - 128 bit Unique ID for each device

- **Industry Standard Pin-out & Packages**
  - JM =16-pin SOIC 300mil
  - JB = 8-pin SOIC 208mil
  - JF = 8-pin VSOP 208mil
  - JK = 8-contact WSON 6x5mm
  - JL = 8-contact WSON 8x6mm
  - JG= 24-ball TFBGA 6x8mm
  - KGD (call factory)

GENERAL DESCRIPTION

The IS25LP032/064/128 Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash are for systems that require limited space, a low pin count, and low power consumption. The IS25LP032/064/128 is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) allowing more than 66Mbytes/s of data throughput. The IS25xP series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256-bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4K-byte sectors, 32K-byte blocks, 64K-byte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

GLOSSARY

Standard SPI
In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Instructions are sent via the SI pin to encode instructions, addresses, or input data to the device on the rising edge of SCK. The DO pin is used to read data or to check the status of the device on the falling edge of SCK. This device supports SPI bus operation modes (0,0) and (1,1).

Mutil I/O SPI
Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, and Quad Input and Output capability. Executing these instructions through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

Quad I/O QPI
The IS25LP032/064/128 enables QPI protocol by issuing an "Enter QPI mode (35h)" command. The QPI mode uses four IO pins for input and output to decrease SPI instruction overhead and increase output bandwidth. SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during QPI mode. Issuing an "Exit QPI (F5h) command will cause the device to exit QPI mode. Power Reset or Hardware/Software Reset can also return the device into the standard SPI mode.

DTR
In addition to SPI and QPI features, IS25LP032/064/128 also supports SPI DTR READ. SPI DTR allows high data throughput while running at lower clock frequencies. SPI DTR READ mode uses both rising and falling edges of the clock to drive output, resulting in reducing the dummy cycles by half.

Programmable drive strength and Selectable burst setting.
The IS25LP032/064/128 offers programmable output drive strength and selectable burst (wrap) length features to increase the efficiency and performance of READ operations. The driver strength and burst setting features are controlled by setting the READ registers. A total of six different drive strengths and four different burst sizes (8/16/32/64 Bytes) are available for selection.

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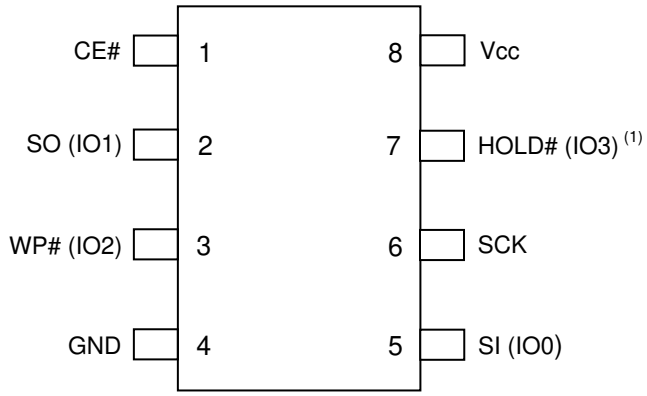
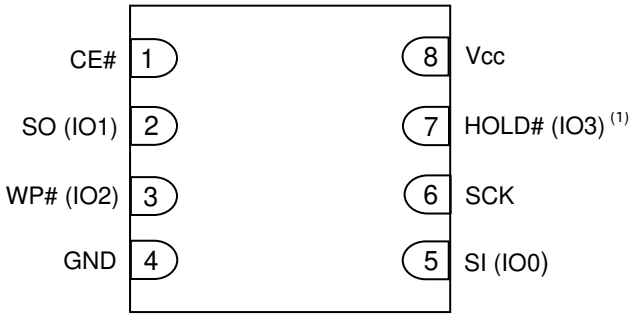
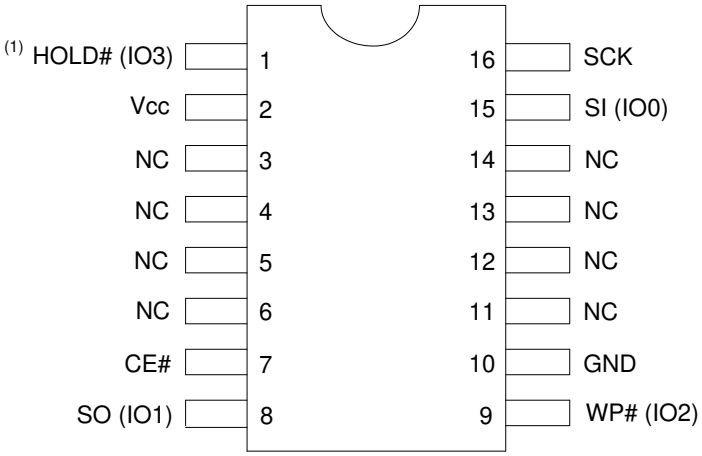
1. PIN CONFIGURATION



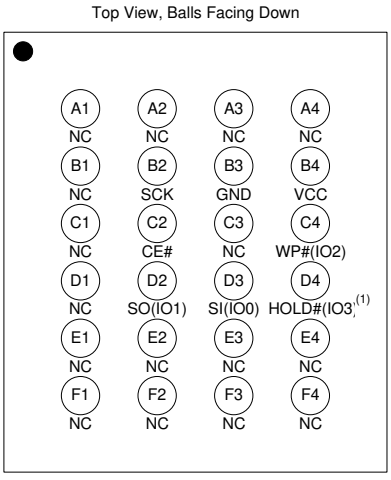
8-pin SOIC 208mil
8-pin VSOP 208mil



8-pin WSON 6x5mm
8-pin WSON 8x6mm



16-pin SOIC 300mil



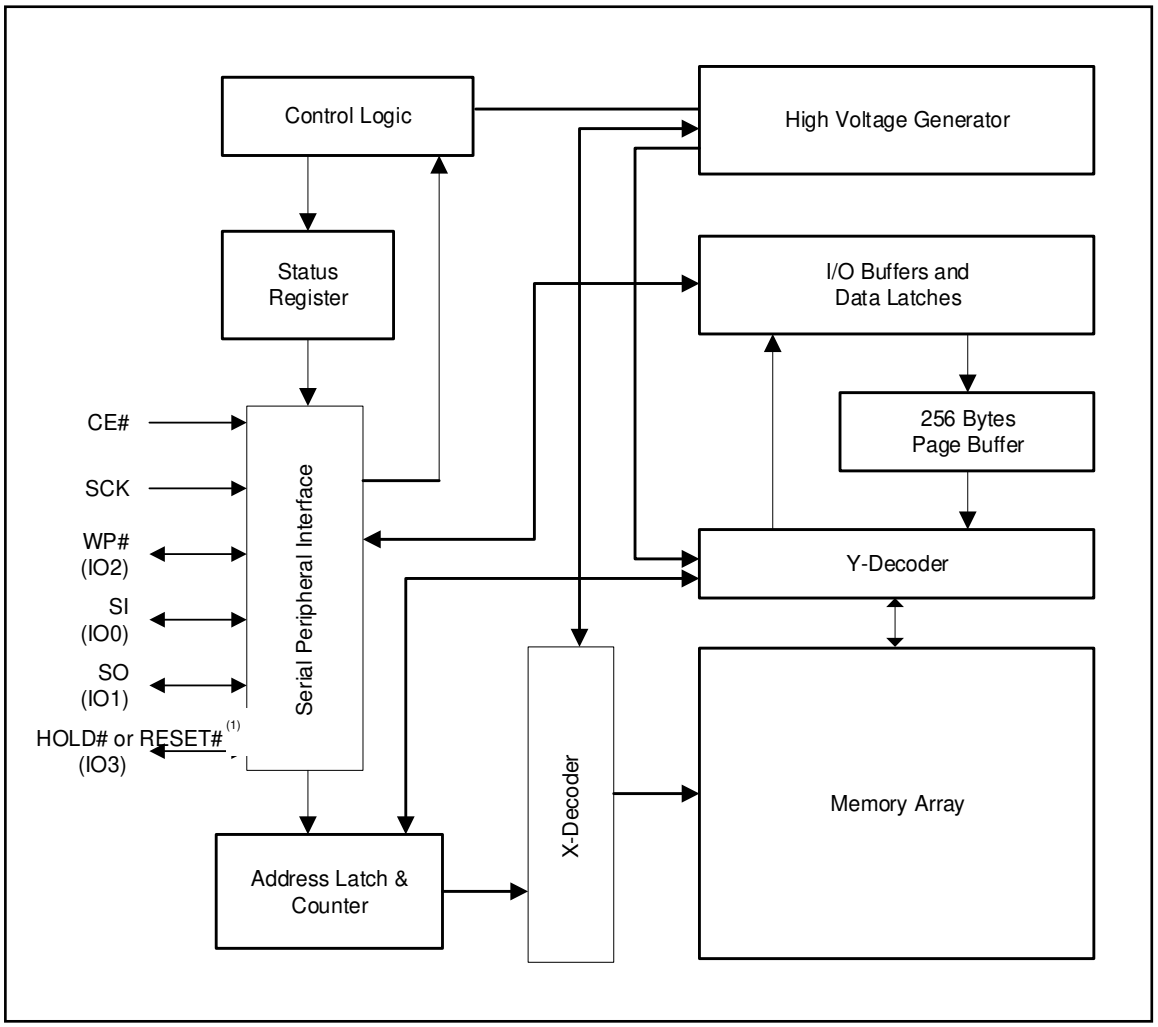
24-ball TFBGA 6x8mm

Note1: For RESET# pin option instead of HOLD# pin, call Factory.

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written. When the WP# is low the status registers are write-protected and vice-versa for high. When the QE bit is set to “1”, the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# or RESET# (IO3)	INPUT/OUTPUT	**HOLD# or RESET#/Serial Data IO (IO3):** When the QE bit of Status Register is set to “1”, HOLD# pin or RESET# is not available since it becomes IO3. When QE=0 the pin acts as HOLD# or RESET#. RESET# pin can be selected with dedicated parts (Call Factory). The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left uncommitted.

3. BLOCK DIAGRAM



Note1: For RESET# pin option instead of HOLD# pin, call Factory.

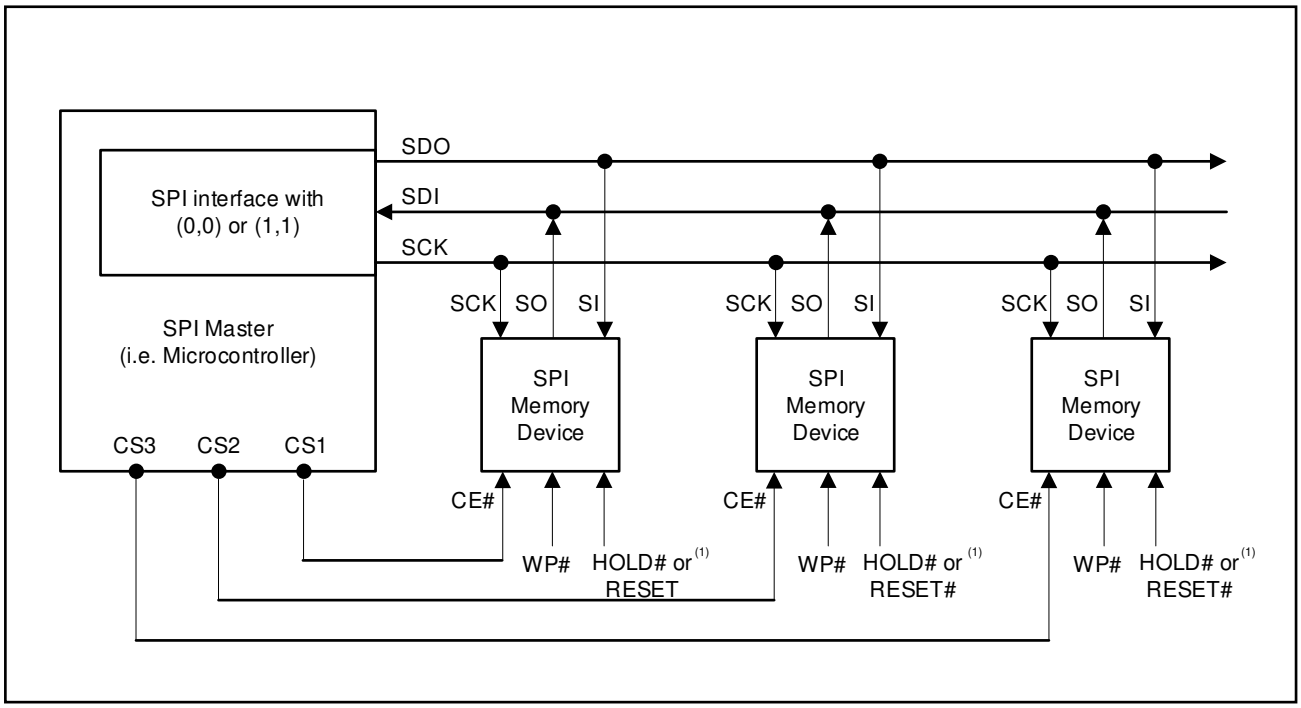
4. SPI MODES DESCRIPTION

Multiple IS25LP032/064/128 devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:

1. For RESET# pin option instead of HOLD# pin, call Factory.
2. SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during QPI mode.

Figure 4.2 SPI Mode Support

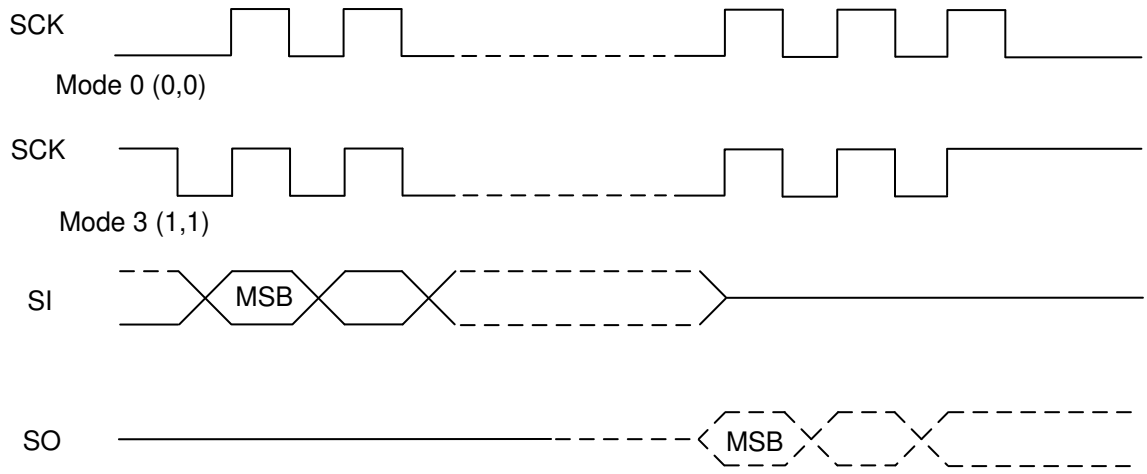
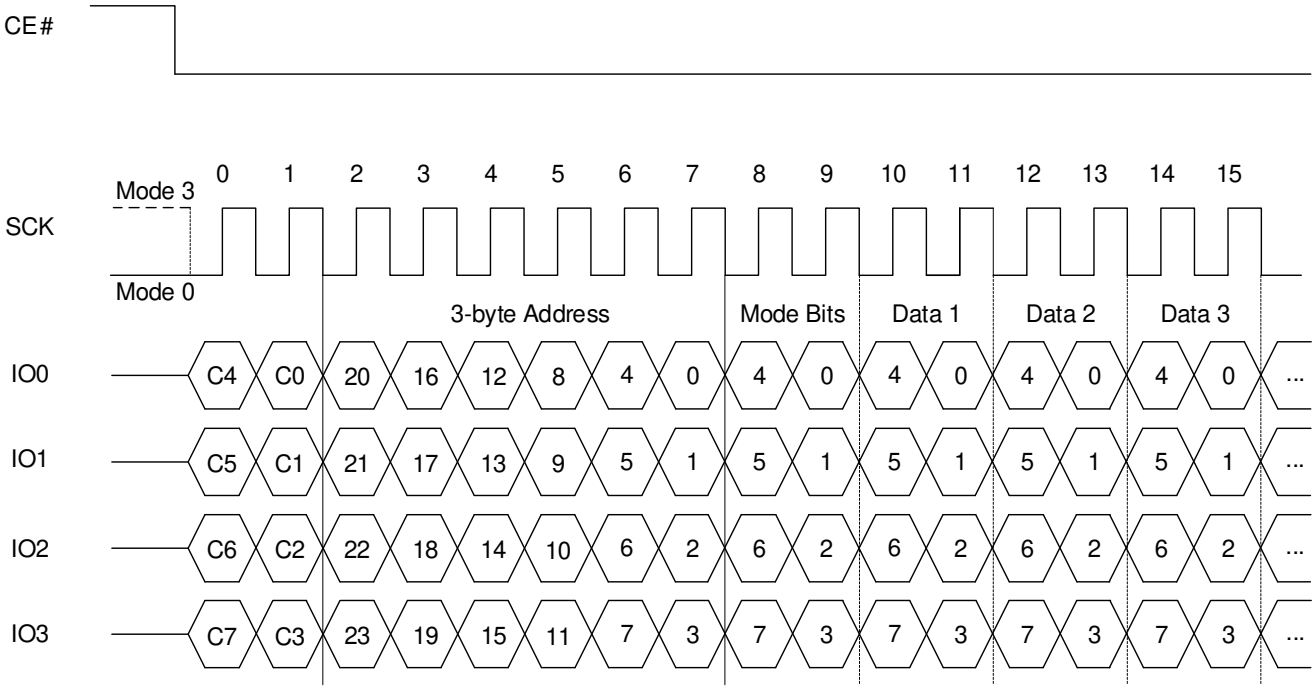


Figure 4.3 QPI Mode Support



5. SYSTEM CONFIGURATION

The memory array of IS25LP032/064/128 is divided into uniform 4 Kbyte sectors or uniform 32K/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is mapped.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses of IS25LP032/064/128

Memory Density			Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (KBytes)	Address Range
32Mb			Block 0	Block 0	Sector 0	4	000000h – 000FFFh
					:	:	:
				Block 1	:	:	:
					Sector 15	4	00F000h - 00FFFFh
			Block 1	Block 2	Sector 16	4	010000h – 010FFFh
					:	:	:
				Block 3	:	:	:
					Sector 31	4	01F000h - 01FFFFh
			Block 2	Block 4	Sector 32	4	020000h - 0200FFh
					:	:	:
				Block 5	:	:	:
	64Mb				Sector 47	4	02F000h – 02FFFFh
			:	:	:	:	:
			Block 63	Block 126	:	:	:
				Block 127	Sector 1023	4	3FF000h – 3FFFFFh
		128Mb	:	:	:	:	:
					:	:	:
				:	:	:	:
					:	:	:
			Block 127	:	:	:	:
					:	:	:
				Block 255	:	:	:
					Sector 2047	4	7FF000h – 7FFFFFh
			:	:	:	:	:
			:	:	:	:	:
			Block 254	Block 508	Sector 4064	4	FE0000h – FE0FFFh
					:	:	:
				Block 509	:	:	:
					Sector 4079	4	FEF000h – FEFFFFh
			Block 255	Block 510	Sector 4080	4	FF0000h – FF0FFFh
					:	:	:
				Block 511	:	:	:
					Sector 4095	4	FFF000h – FFFFFFh

6. REGISTERS

The IS25LP032/064/128 has three sets of Registers: Status, Function and Read.

6.1 STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Tables 6.1 & 6.2.

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default (Flash bit)	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No
Bit 2	BP0	Block Protection Bit: (See Tables 6.3 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Yes
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Yes

The BP0, BP1, BP2, BP3, SRWD, and QE are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP2, BP1, BP0, and SRWD bits were set to “0” at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for write status register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled and all write operations, including write status register, write configuration register, page program, sector erase, block and chip erase operations are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any write operation.

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Tables 6.3 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the status register that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD# pin is tied directly to the power supply or ground.

Table 6.3 Block (64Kbyte) assignment by Block Write Protect (BP) Bits

Status Register Bits				Protected Memory Area (**IS25LP128, 256Blocks**)	
BP3	BP2	BP1	BP0	**TBS(T/B selection) = 0, TOP area**	**TBS(T/B selection) = 1, Bottom area**
0	0	0	0	0(None)	0(None)
0	0	0	1	1(1 block : 255th)	1(1 block : 0th)
0	0	1	0	2(2 blocks : 254th and 255th)	2(2 blocks : 0th and 1st)
0	0	1	1	3(4 blocks : 252nd to 255th)	3(4 blocks : 0th to 3rd)
0	1	0	0	4(8 blocks : 248th to 255th)	4(8 blocks : 0th to 7th)
0	1	0	1	5(16 blocks :240th to 255th)	5(16 blocks : 0th to 15th)
0	1	1	0	6(32 blocks : 224th to 255th)	6(32 blocks : 0th to 31st)
0	1	1	1	7(64 blocks : 192nd to 255th)	7(64 blocks : 0th to 63rd)
1	0	0	0	8(128 blocks : 128th to 255th)	8(128 blocks : 0th to 127th)
1	0	0	1	9(256 blocks : 0th to 255th) All blocks	9(256 blocks : 0th to 255th) All blocks
1	0	1	x	10-11(256 blocks : 0th to 255th) All blocks	10-11(256 blocks : 0th to 255th) All blocks
1	1	x	x	12-15(256 blocks : 0th to 255th) All blocks	12-15(256 blocks : 0th to 255th) All blocks

Status Register Bits				Protected Memory Area(**IS25LP064, 128Blocks**)	
BP3	BP2	BP1	BP0	**TBS(T/B selection) = 0, TOP area**	**TBS(T/B selection) = 1, Bottom area**
0	0	0	0	0(None)	0(None)
0	0	0	1	1(1 block : 127th)	1(1 block : 0th)
0	0	1	0	2(2 blocks : 126th and 127th)	2(2 blocks : 0th and 1st)
0	0	1	1	3(4 blocks : 124th to 127th)	3(4 blocks : 0th to 3rd)
0	1	0	0	4(8 blocks : 120th to 127th)	4(8 blocks : 0th to 7th)
0	1	0	1	5(16 blocks :112nd to 127th)	5(16 blocks : 0th to 15th)
0	1	1	0	6(32 blocks : 96th to 127th)	6(32 blocks : 0th to 31st)
0	1	1	1	7(64 blocks : 64th to 127th)	7(64 blocks : 0th to 63rd)
1	x	x	x	8~15(128 blocks : 0th to 127th) All blocks	8~15(128 blocks : 0th to 127th) All blocks

Status Register Bits				Protected Memory Area(**IS25LP032, 64Blocks**)	
BP3	BP2	BP1	BP0	**TBS(T/B selection) = 0, TOP area**	**TBS(T/B selection) = 1, Bottom area**
0	0	0	0	0(None)	0(None)
0	0	0	1	1(1 block : 63rd)	1(1 block : 0th)
0	0	1	0	2(2 blocks : 62nd and 63rd)	2(2 blocks : 0th and 1st)
0	0	1	1	3(4 blocks : 60th to 63rd)	3(4 blocks : 0th to 3rd)
0	1	0	0	4(8 blocks : 56th to 63rd)	4(8 blocks : 0th to 7th)
0	1	0	1	5(16 blocks :48th to 63rd)	5(16 blocks : 0th to 15th)
0	1	1	0	6(32 blocks : 32nd to 63rd)	6(32 blocks : 0th to 31st)
0	1	1	1	7(64 blocks : 0th to 63rd) All blocks	7(64 blocks : 0th to 63rd) All blocks
1	x	x	x	8~15(64 blocks : 0th to 63rd) All blocks	8~15(64 blocks : 0th to 63rd) All blocks

Note: x is don't care

6.2 FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.4 and 6.5

Table 6.4 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0	ESUS	PSUS	TBS	Reserved
Default	0	0	0	0	0	0	0	0

Table 6.5 Function Register Bit Definition

Bit	Name	Definition	Read-/Write	Non-Volatile bit
Bit 0	Reserved	Reserved	Reserved	Reserved
Bit 1	Top/Bottom Selection	Top/Bottom Selection. (See Tables 6.3 for details) “0” indicates Top area. “1” indicates Bottom area.	R/W	Yes
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	No
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	No
Bit 4	IR Lock 0	Lock the information row 0: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Yes
Bit 5	IR Lock 1	Lock the information row 1: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Yes
Bit 6	IR Lock 2	Lock the information row 2: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Yes
Bit 7	IR Lock 3	Lock the information row 3: “0” indicates the information row can be programmed “1” indicates the information row cannot be programmed	R/W	Yes

Note: Table 6.5 Function Register bits are only one time programmable and cannot be modified

Top/Bottom Selection: BP0~3 area assignment changed from Top or Bottom. See Tables 6.5 for details

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to ‘1’ after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to ‘0.’

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is ‘1’ after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to ‘0.’

IR lock bit 0 ~ 3: The information row lock bits are programmable. If the bit set to “1”, it can’t be programmed.

6.3 READ REGISTERS

Read Register format and Bit definitions pertaining to QPI mode are described below.

READ PARAMETER BITS

Table 6.6 defines all bits that control features in SPI/QPI modes. The ODS2, ODS1, ODS0 (P7, P6, P5) bits provide a method to set and control driver strength. The Dummy Cycle bits (P4, P3) define how many dummy cycles are used during various READ modes. The wrap selection bits (P2, P1, P0) define burst length with wrap around.

The SET READ PARAMETERS Operation (SRP, C0h) is used to set all the Read Register bits, and can thereby define the output driver strength, number of dummy cycles used during READ modes, burst length with wrap around.

Table 6.6 Read Parameter Table

	P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
	ODS2	ODS1	ODS0	Dummy Cycles	Dummy Cycles	Wrap Enable	Burst Length	Burst Length
Default (Flash bit)	1	1	1	0	0	0	0	0

Table 6.7 Burst Length Data

	P1	**P0**
8 bytes	0	0
16 bytes	0	1
32 bytes	1	0
64 bytes	1	1

Table 6.8 Wrap Function

Wrap around boundary	**P2**
Whole cell regardless of P1 and P0 value	0
Burst Length set by P1 and P0	1

Table 6.9 Read Dummy Cycles.

Read Modes	P4,P3 = 00 (Default)	P4,P3 = 01	P4,P3 = 10	P4,P3 = 11	Max Freq	Mode
Normal Read 03h	0	0	0	0	50MHz	SPI
Fast read 0Bh	8	8	8	8	133MHz	SPI
Fast read 0Bh	6	4	8	10	4cc : 84MHz 6cc : 104MHz 8cc/10cc : 133MHz	QPI
Dual IO Read (1) BBh	4	4	8	4	4cc : 104MHz 8cc : 133MHz	SPI
Fast Read Dual Output 3Bh	8	8	8	8	133MHz	SPI
Quad IO Read (2) EBh	6	4	8	10	4cc : 84MHz 6cc : 104MHz 8cc/10cc : 133MHz	SPI , QPI

Notes:

1. **When 4 dummy cycles are used the max clock frequency is 104MHz; when 8 dummy cycles are used the max clock frequency is 133MHz.**
2. **When 4 dummy cycles are used the max clock frequency is 84MHz; when 6 dummy cycles are used the max clock frequency is 104MHz; when 8 or 10 dummy cycles are used the max clock frequency is 133MHz.**
3. **In SPI DTR mode the dummy cycles are reduced by half.**
4. **Dummy cycles in the table are including Mode bit cycles.**

Table 6.10 Driver Strength Table

ODS2	ODS1	ODS0	Description	Remark
0	0	0	Reserved	
0	0	1	12.50%	
0	1	0	25%	
0	1	1	37.50%	
1	0	0	Reserved	
1	0	1	75%	
1	1	0	100%	
1	1	1	50%	Default

7. PROTECTION MODE

The IS25LP032/064/128 supports hardware and software write-protection mechanisms.

7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, SRWD, and QE in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage is 2.1V. All write sequence will be ignored when Vcc drops to 2.1V or lower.

7.2 SOFTWARE WRITE PROTECTION

The IS25LP032/064/128 also provides a software write protection feature. The Block Protection (BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

Table 7.1 Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Note: Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

8. DEVICE OPERATION

The IS25LP032/064/128 utilizes an 8-bit instruction register. Refer to Table 8.1. Instruction Set for details on instructions and instruction codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI) or Serial Data IOs (IO0, IO1, IO2, IO3). The input data on SI or IOs is latched on the rising edge of Serial Clock (SCK) for normal mode and both of rising and falling edges for DTR mode after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in to end the operation.

Table 8.1 Instruction Set

Instruction Name	Operation	Total Bytes	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
NORD	Normal Read Mode	4	SPI	03h	A <23:16>	A <15:8>	A <7:0>	Data out		
FRD	Fast Read Mode	5	SPI QPI	0Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Data out	
FRDIO	Fast Read Dual I/O	3	SPI	BBh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	AXh(1),(2) Dual	Dual Data out	
FRDO	Fast Read Dual Output	5	SPI	3Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Dual Data out	
FRQIO	Fast Read Quad I/O	2	SPI QPI	EBh	A <23:16> Quad	A <15:8> Quad	A <7:0> Quad	AXh(1), (2) Quad	Quad Data out	
FRDTR	Fast Read DTR Mode	5	SPI QPI	0Dh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Dual Data out	
FRDDTR	Fast Read Dual I/O DTR	3	SPI	BDh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	AXh(1), (2) Dual	Dual Data out	
FRQDTR	Fast Read Quad I/O DTR	5	SPI QPI	EDh	A <23:16>	A <15:8>	A <7:0>	AXh(1), (2) Quad	Quad Data out	
PP	Input Page Program	4 + 256	SPI QPI	02h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
PPQ	Quad Input Page Program	4 + 256	SPI	32h 38h	A <23:16>	A <15:8>	A <7:0>	Quad PD (256byte)		
SER	Sector Erase	4	SPI QPI	D7h 20h	A <23:16>	A <15:8>	A <7:0>			
BER32 (32Kb)	Block Erase 32K	4	SPI QPI	52h	A <23:16>	A <15:8>	A <7:0>			
BER64 (64Kb)	Block Erase 64K	4	SPI QPI	D8h	A <23:16>	A <15:8>	A <7:0>			
CER	Chip Erase	1	SPI QPI	C7h 60h						
WREN	Write Enable	1	SPI QPI	06h						
WRDI	Write Disable	1	SPI QPI	04h						
RDSR(5)	Read Status Register	2	SPI QPI	05h	SR					
WRSR	Write Status Register	2	SPI QPI	01h	WSR Data					
RDFR(5)	Read Function Register	2	SPI QPI	48h	Data out					

Instruction Name	Operation	Total Bytes	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
WRFR	Write Function Register	2	SPI QPI	42h	WFR Data					
QIOEN	Enter QPI mode	1	SPI	35h						
QIODI	Exit QPI mode	1	QPI	F5h						
PERSUS	Suspend during program/erase	1	SPI QPI	75h B0h						
PERRSM	Resume program/erase	1	SPI QPI	7Ah 30h						
DP	Deep Power Down	1	SPI QPI	B9h						
RDID(5), RDPD	Read ID / Release Power Down	4	SPI QPI	ABh	XXh(3)	XXh(3)	XXh(3)	ID7-ID0		
SRP	Set Read Parameters	4	SPI QPI	C0h	Data in					
RDJDID(5)	Read JEDEC ID Command	1	SPI	9Fh	MF7-MF0	ID15-ID8	ID7-ID0			
RDMDID(5)	Read Manufacturer & Device ID	4	SPI QPI	90h	XXh(3)	XXh(3)	00h	MF7-MF0	ID7-ID0	
							01h	ID7-ID0	MF7-MF0	
RDJDIDQ(5)	Read JEDEC ID QPI mode	4	QPI	AFh	MF7-MF0	ID15-ID8	ID7-ID0			
RDUID	Read Unique ID	4	SPI QPI	4Bh	A(4) <23:16>	A(4) <15:8>	A(4) <7:0>	Dummy Byte	Data out	
RDSFDP	SFDP Read	5	SPI QPI	5Ah	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Data out	
RSTEN	Software Reset Enable	1	SPI QPI	66h						
RST	Software Reset	1	SPI QPI	99h						
IRER	Erase Information Row	4	SPI QPI	64h	A <23:16>	A <15:8>	A <7:0>			
IRP	Program Information Row	4 + 256	SPI QPI	62h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
IRRD	Read Information Row	4	SPI QPI	68h	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Data out	
SECUN-LOCK	Sector Unlock	4	SPI QPI	26h	A <23:16>	A <15:8>	A <7:0>			
SECLOCK	Sector Lock	1	SPI QPI	24h						

Notes:
1. **The number of dummy cycles depends on the value setting in the Table 6.9 Read Dummy Cycles.**
2. **AXh has to be counted as a part of dummy cycles. X means "don't care".**
3. **XX means "don't care".**
4. **A<23:9> are "don't care" and A<8:4> are always "0".**
5. **The maximum clock frequency is 104MHz for Vcc=2.3V~2.7V and 133MHz for Vcc=2.7V~3.6V.**

8.1 NORMAL READ OPERATION (NORD, 03h)

The NORMAL READ (NORD) instruction is used to read memory contents of the IS25LP032/064/128 at a maximum frequency of 50MHz.

The NORD instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

The first byte data (D7 - D0) is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one NORMAL READ instruction. The address is automatically incremented by one after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

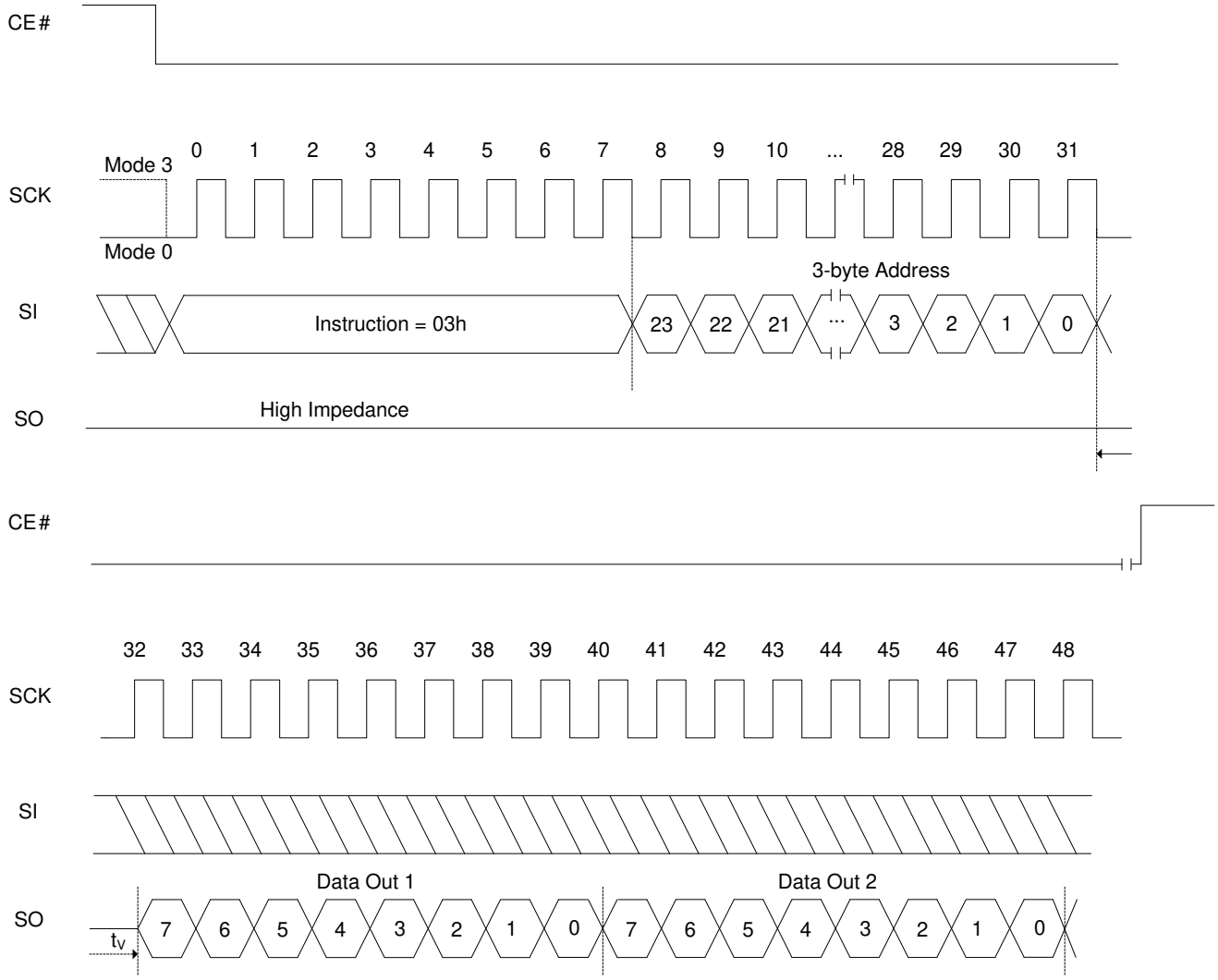
If the NORMAL READ instruction is issued while an Erase, Program or Write operation is in process (WIP=1) the instruction is ignored and will not have any effects on the current operation.

Table 8.2 Address Key

Address	IS25LP032	IS25LP064	IS25LP128
A_N (A_{MSB} – A_0)	A23 - A0 (A23,A22=X)	A23 - A0 (A23=X)	A23 - A0

X=Don't Care

Figure 8.1 Normal Read Sequence



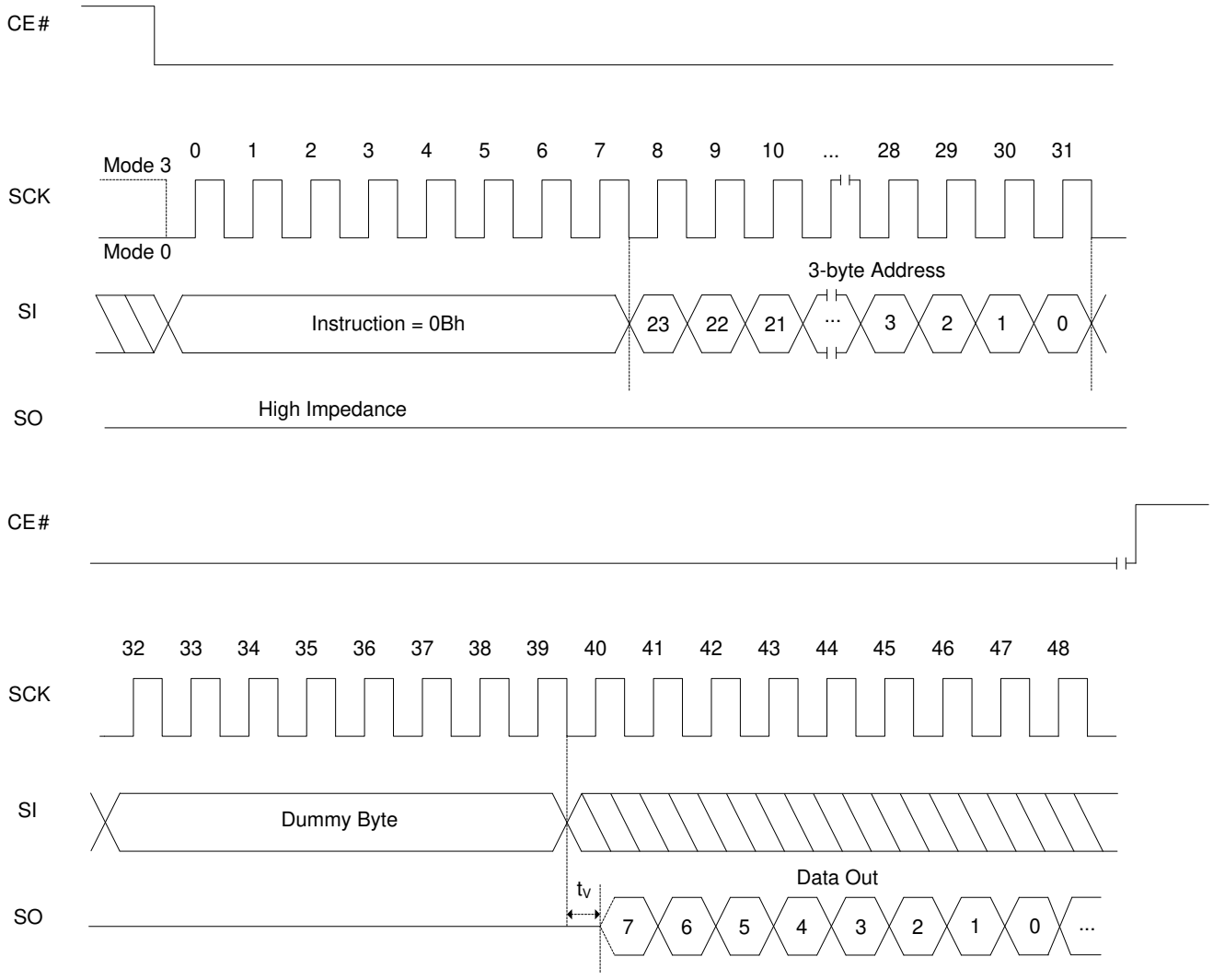
8.2 FAST READ OPERATION (FRD, 0Bh)

The FAST READ (FRD) instruction is used to read memory data at up to a 133MHz clock.

The FAST READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte from the address is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ instruction. The FAST READ instruction is terminated by driving CE# high (VIH). If the FAST READ instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored without affecting the current cycle.

Figure 8.2 Fast Read Sequence



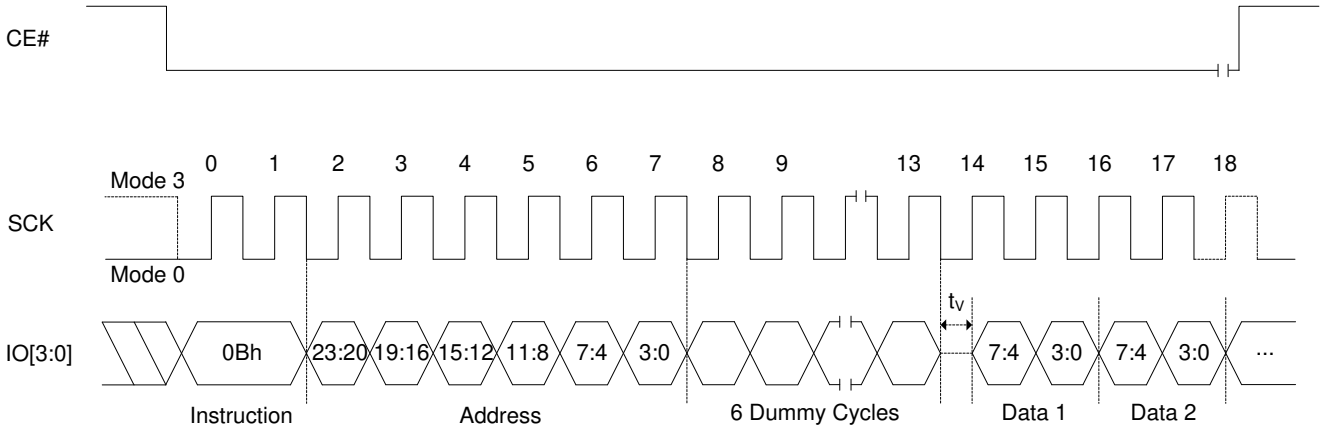
FAST READ QPI OPERATION (FRD QPI, 0Bh)

The FAST READ QPI (FRD QPI) instruction is used to read memory data at up to a 133MHz clock.

The FAST READ QPI instruction code (2 clocks) is followed by three address bytes (A23-A0—6clocks) and dummy cycles, transmitted via the QPI line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ QPI instruction. The FAST READ QPI instruction is terminated by driving CE# high (VIH). If the FAST READ QPI instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored without affecting the current cycle.

Figure 8.3 Fast Read Sequence, QPI Mode



Note: Number of dummy cycles depends on Read Parameter setting. Detailed information in Table 6.9 Read Dummy Cycles.

8.3 HOLD OPERATION

HOLD# is used in conjunction with CE# to select the IS25LP032/064/128. When the device is selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to SIO will be ignored while SO is in the high impedance state.

Note: HOLD is not supported in DTR mode or with QE=1.

Timing graph can be referenced in AC Parameters Figure 9.3

8.4 FAST READ DUAL I/O OPERATION (FRDIO, BBh)

The FRDIO allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRDIO instruction code is followed by three address bytes (A23 – A0) and dummy cycles, transmitted via the IO0 and IO1 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and this shift pattern continues to alternate between the two lines. Depending on the usage of AX read operation mode, a mode byte may be located after address input.

The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The MSB is output on IO1, while simultaneously the second bit is output on IO0. Figure 8.4 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

The device supports the AX read operation by applying mode bits during dummy period. Mode bits consist of 8 bits, such as M7 to M0. Four cycles after address input are reserved for Mode bits in FRDIO execution. M7 to M4 are important for enabling this mode. M3 to M0 become don't care for future use. When M[7:4]=1010(Ah), it enables the AX read operation and subsequent FRDIO execution skips command code. It saves cycles as described in Figure 8.5. When the code is different from AXh (X: don't care), the device exits the AX read operation. After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting. Mode bit must be applied during dummy cycles. Number of dummy cycle in Table 6.9 includes number of mode bit cycles. If dummy cycles is configured as 4 cycles, data output will starts right after mode bit applied.

If the FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not affect the current cycle.