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IS25WP064A
IS25WP032A

64/32Mb
1.8V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

ADVANCED DATA SHEET

64/32Mb

1.8V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

ADVANCED INFORMATION

FEATURES

- **Industry Standard Serial Interface**
  - IS25WP064A: 64Mbit/8Mbyte
  - IS25WP032A: 32Mbit/4Mbyte(Call Factory)
  - 256 bytes per Programmable Page
  - Supports standard SPI, Fast, Dual, Dual I/O, Quad, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
  - Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**
  - 50MHz Normal and 133Mhz Fast Read
  - 532 MHz equivalent QPI
  - DTR (Dual Transfer Rate) up to 66MHz
  - Selectable Dummy Cycles
  - Configurable Drive Strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 Erase/Program Cycles
  - More than 20-year Data Retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform: Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 Bytes per Page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous Read 8/16/32/64-Byte Burst Wrap
  - Selectable Burst Length
  - QPI for Reduced Instruction Overhead
  - AutoBoot Operation

- **Low Power with Wide Temp. Ranges**
  - Single 1.65V to 1.95V Voltage Supply
  - 4 mA Active Read Current (typ.)
  - 5 µA Standby Current (typ.)
  - 1 µA Deep Power Down (typ.)
  - Temp Grades:
    Extended: -40°C to +105°C
    Extended+: -40°C to +125°C (Call Factory)
    Auto Grade: up to +125°C(Call Factory)

    Note: Extended+ should not be used for Automotive.

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Power Supply Lock Protection
  - 4x256-Byte Dedicated Security Area with OTP User-lockable Bits
  - 128 bit Unique ID for Each Device (Call Factory)

- **Industry Standard Pin-out & Packages(1)**
  - M =16-pin SOIC 300mil(2)
  - B = 8-pin SOIC 208mil
  - K = 8-contact WSON 6x5mm
  - L = 8-contact WSON 8x6mm
  - G= 24-ball TFBGA 4x6 ARRAY(2) (Call Factory)
  - H = 24-ball TFBGA 5x5 ARRAY (2)
  - KGD (Call Factory)

Notes:
1. Call Factory for other package options available
2. For the dedicated RESET# option, see the Ordering Information

GENERAL DESCRIPTION

The IS25WP064A/032A Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66Mbytes/s of data throughput. The IS25xP series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256-bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

GLOSSARY

Standard SPI
In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Instructions are sent via the SI pin to encode instructions, addresses, or input data to the device on the rising edge of SCK. The SO pin is used to read data or to check the status of the device. This device supports SPI bus operation modes (0,0) and (1,1).

Mutil I/O SPI
Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, Quad Output, and Quad Input and Output capability. Executing these instructions through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

QPI
The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the enter QPI (35h) instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the instruction code thus requiring only two serial clocks. This can significantly reduce the SPI instruction overhead and improve system performance. Only QPI mode or SPI/Dual/Quad mode can be active at any given time. Enter QPI (35h) and Exit QPI (F5h) instructions are used to switch between these two modes, regardless of the non-volatile Quad Enable (QE) bit status in the Status Register. Power Reset or Hardware/Software Reset will return the device into the standard SPI mode. SI and SO pins become bidirectional I/O0 and I/O1, and WP# and HOLD# pins become I/O2 and I/O3 respectively during QPI mode.

DTR
In addition to SPI and QPI features, the device also supports Fast READ DTR operation. DTR operation allows high data throughput while running at lower clock frequencies. Fast READ DTR operation uses both rising and falling edges of the clock for address inputs, and data outputs, resulting in reducing input and output cycles by half.

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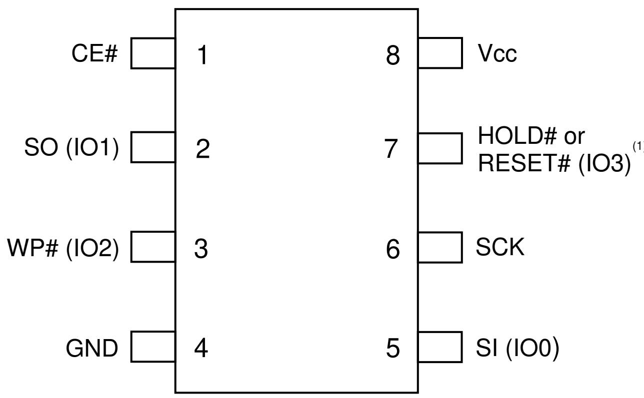
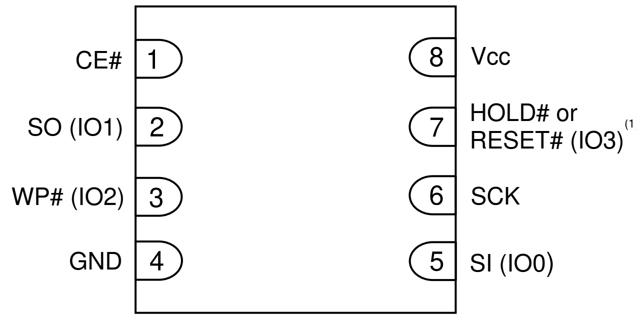
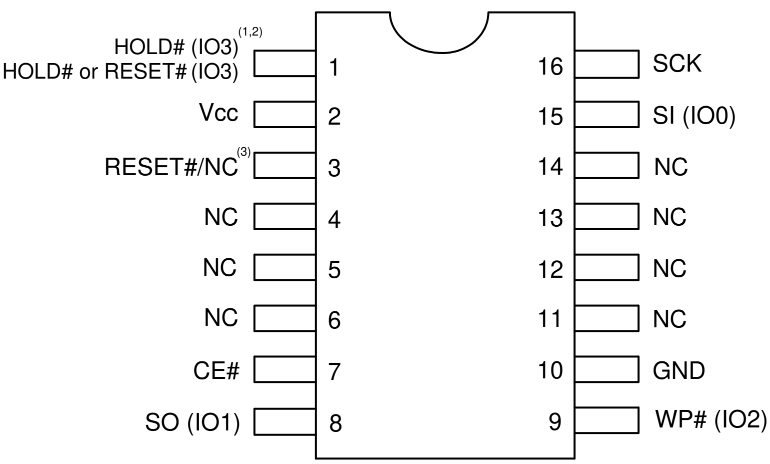
1. PIN CONFIGURATION



8-pin SOIC 208mil

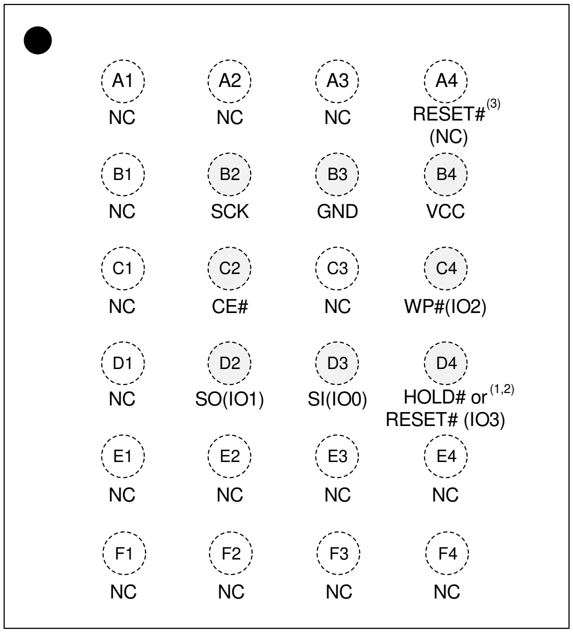


8-contact WSON 6x5mm
8-contact WSON 8x6mm



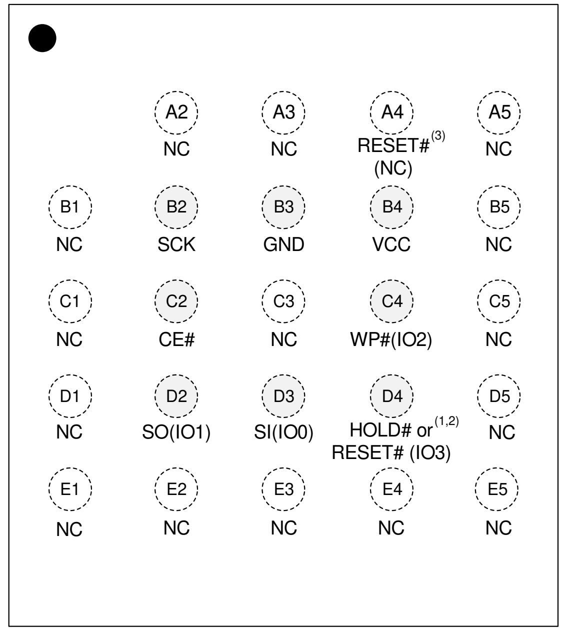
16-pin SOIC 300mil

Top View, Balls Facing Down



24-ball TFBGA 6x8mm (4x6 ball array)

Top View, Balls Facing Down



24-ball TFBGA 6x8mm (5x5 ball array)

Notes:

1. **The pin can be configured as Hold# or Reset# by setting P7 bit of the Read Register. Pin default is Hold#.**
2. **Dedicated RESET# pin is available in devices with a dedicated part number, in these devices Pin 1 (16-pin SOIC) or ball D4 (24-ball TFBGA) are set to Hold# regardless of P7 setting of the Read Register.**
3. **For compatibility, the pin can be disabled on dedicated part numbers by setting Bit0 (RESET# Enable/Disable) of the Function Register to “1” (default is “0” from factory on dedicated part numbers). An internal pull-up resistor exists and the pin may be left floating if not used.**

16-pin SOIC / 24-ball TFBGA	Device with RESET#/HOLD#	Device with dedicated RESET#
Pin1 / Ball D4	Hold#(IO3) or RESET#(IO3) by P7 bit setting	Hold#(IO3) only regardless of P7 bit setting
Pin3 / Ball A4	NC	RESET#
Part Number Option	J	R or P

2. PIN DESCRIPTIONS

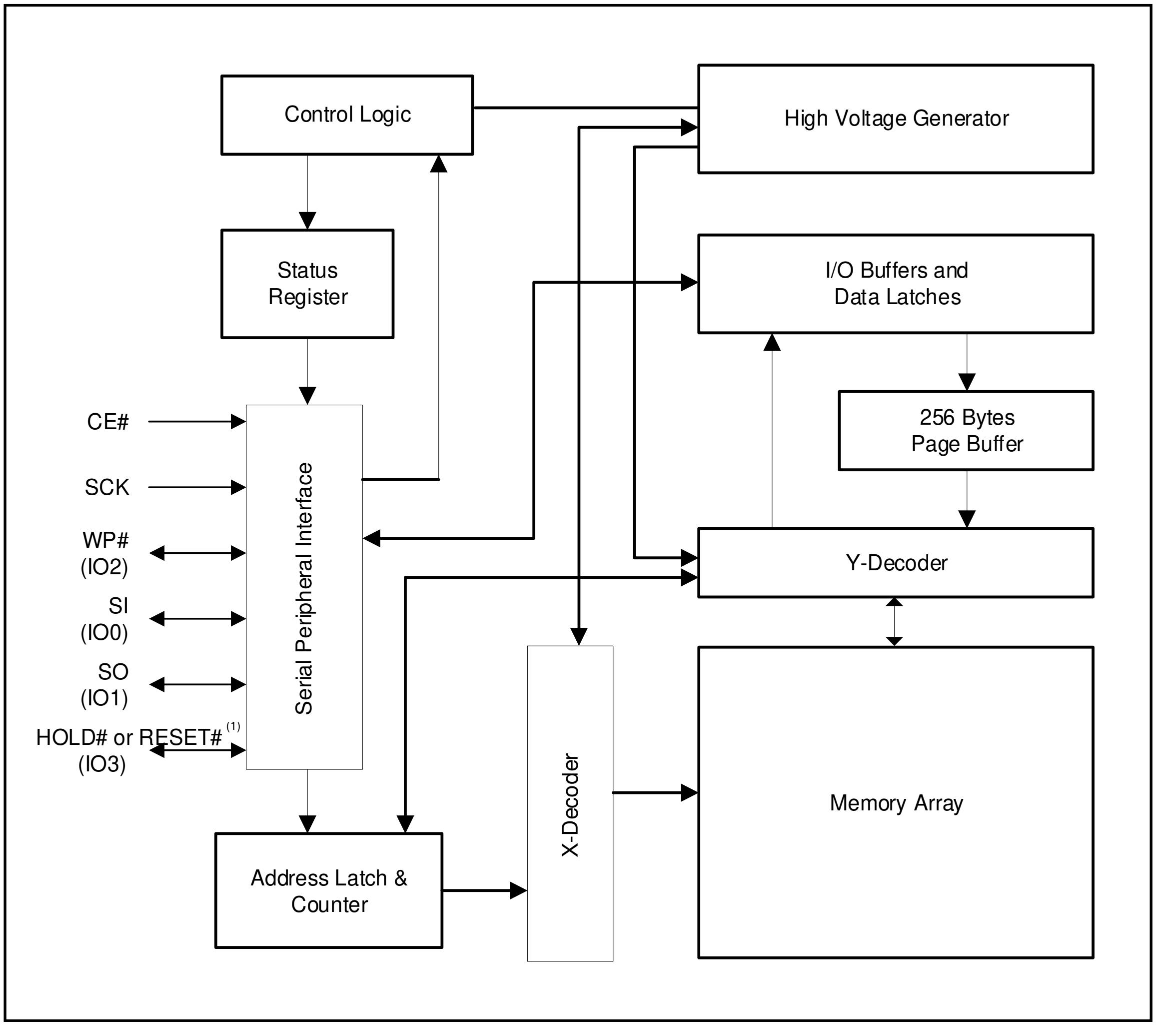
For the device with RESET#/Hold#

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to “1” and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to “0”, the Status Register is not write-protected regardless of WP# state. When the QE bit is set to “1”, the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# or RESET# (IO3)	INPUT/OUTPUT	**HOLD# or RESET#/Serial Data IO (IO3):** When the QE bit of Status Register is set to “1”, HOLD# pin or RESET# is not available since it becomes IO3. When QE=0, the pin acts as HOLD# or RESET# and either one can be selected by the P7 bit setting in Read Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left unconnected.

For the device with dedicated RESET#

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Same as the description in previous page
SI (IO0), SO (IO1)	INPUT/OUTPUT	Same as the description in previous page
WP# (IO2)	INPUT/OUTPUT	Same as the description in previous page
HOLD# (IO3)	INPUT/OUTPUT	**HOLD#/Serial Data IO (IO3):** When the QE bit of Status Register is set to “1”, HOLD# pin is not available since it becomes IO3. When QE=0 the pin acts as HOLD# regardless of the P7 bit of Read Register. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state.
RESET#	INPUT/OUTPUT	**RESET#:** This dedicated RESET# is available only for dedicated parts. The RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	Same as the description in previous page
Vcc	POWER	Same as the description in previous page
GND	GROUND	Same as the description in previous page
NC	Unused	Same as the description in previous page

3. BLOCK DIAGRAM



Note1: In case of 16-pin SOIC or 24-ball TFBFA, dedicated RESET# can be supported without sharing with HOLD# pin for the dedicated parts. See the Ordering Information for the dedicated RESET# option.

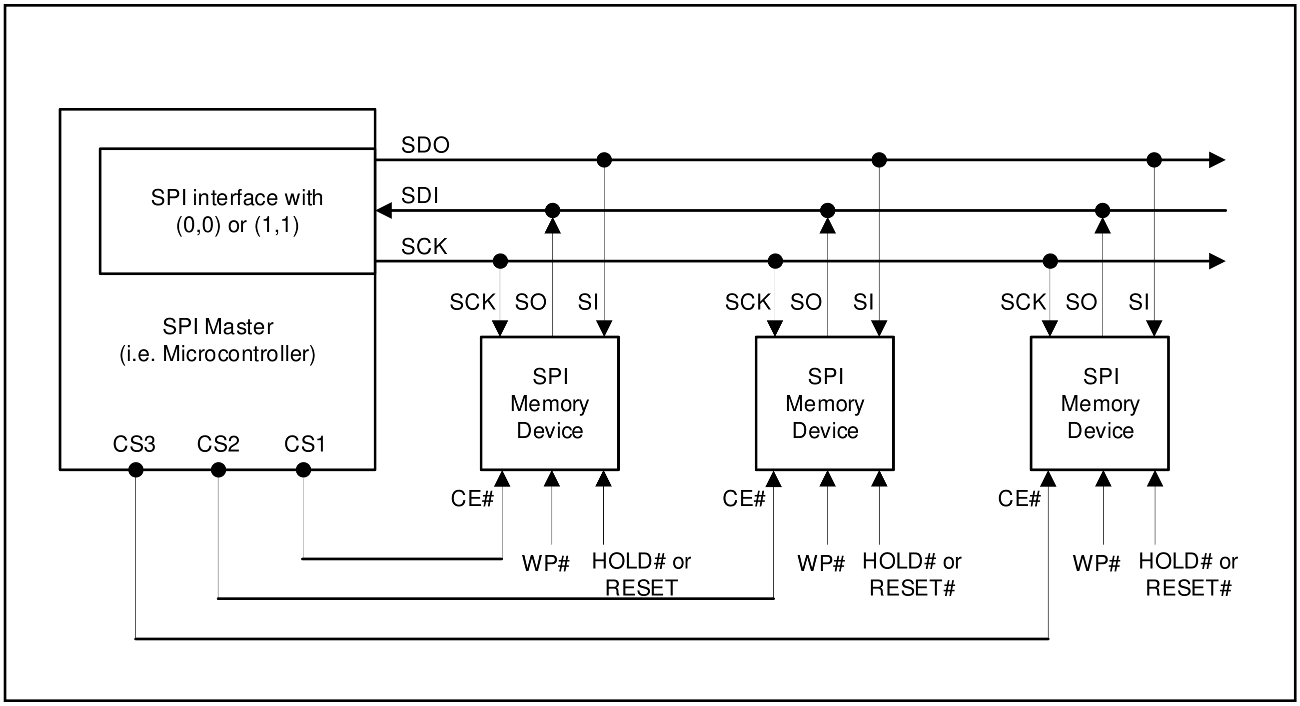
4. SPI MODES DESCRIPTION

Multiple IS25WP064A/032A devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at “0” (SCK = 0) for Mode 0 and the clock remains at “1” (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:

1. **In case of 16-pin SOIC and 24-ball TFBGA, dedicated RESET# can be supported without sharing with HOLD# pin for the dedicated parts. See the Ordering Information for the dedicated RESET# option.**
2. **SI and SO pins become bidirectional IO0 and IO1 respectively during Dual I/O mode and SI, SO, WP#, and HOLD# pins become bidirectional IO0, IO1, IO2, and IO3 respectively during Quad I/O or QPI mode.**

Figure 4.2 SPI Mode Support

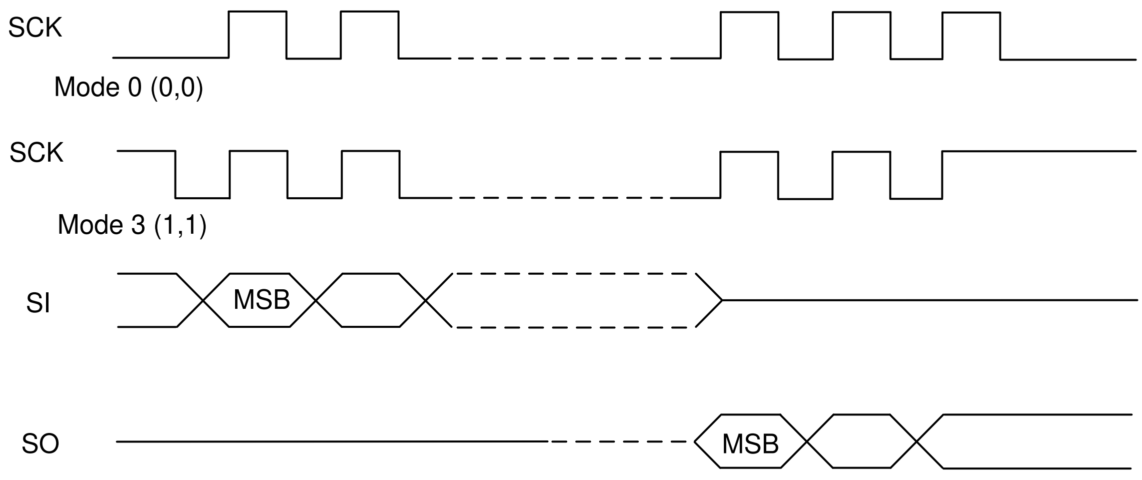
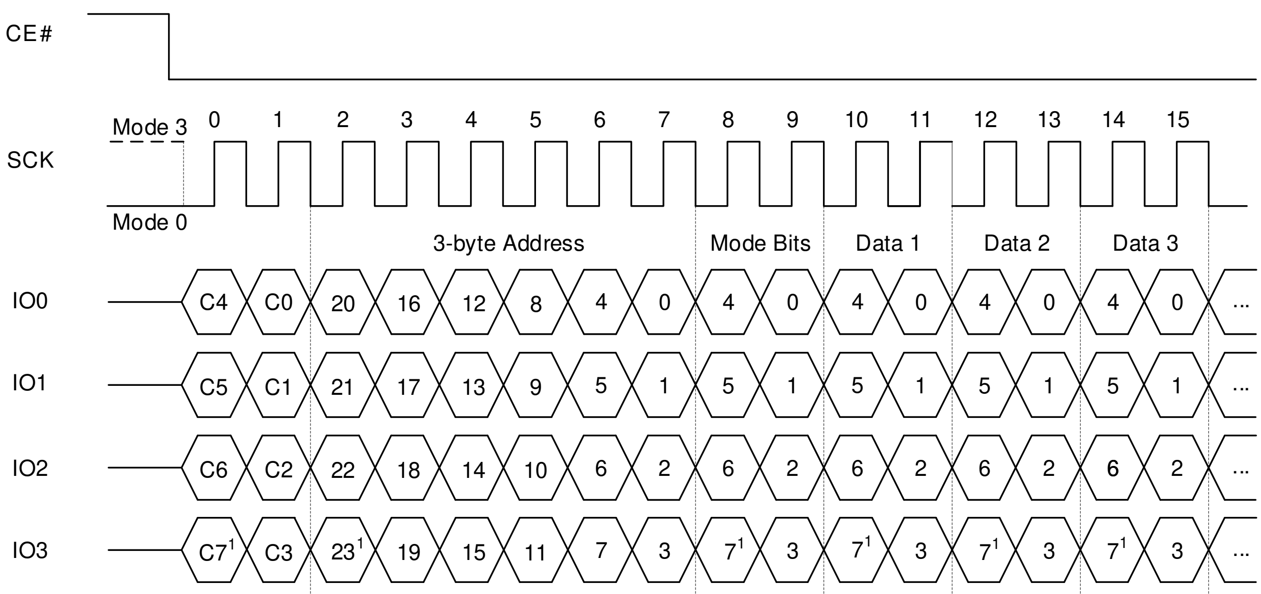


Figure 4.3 QPI Mode Support



Note1: MSB (Most Significant Bit)

5. SYSTEM CONFIGURATION

The memory array is divided into uniform 4 Kbyte sectors or uniform 32/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses of IS25WP064A/032A

Memory Density		Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbytes)	Address Range
32Mb	64Mb	Block 0	Block 0	Sector 0	4	000000h – 000FFFh
				:	:	:
			Block 1	:	:	:
				Sector 15	4	00F000h - 00FFFFh
		Block 1	Block 2	Sector 16	4	010000h – 010FFFh
				:	:	:
			Block 3	:	:	:
				Sector 31	4	01F000h - 01FFFFh
		Block 2	Block 4	Sector 32	4	020000h – 020FFFh
				:	:	:
			Block 5	:	:	:
				Sector 47	4	02F000h – 02FFFFh
		:	:	:	:	:
		Block 63	Block 126	Sector 1008	4	3F0000h – 3F0FFFh
				:	:	:
			Block 127	:	:	:
				Sector 1023	4	3FF000h – 3FFFFFh
		:	:	:	:	:
		Block 127	Block 254	Sector 2032	4	7F0000h – 7F0FFFh
				:	:	:
			Block 255	:	:	:
				Sector 2047	4	7FF000h – 7FFFFFh

6. REGISTERS

The device has four sets of Registers: Status, Function, Read, and Autoboot.

6.1 STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Table 6.1 & Table 6.2.

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read /Write	Type
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W[1]	Volatile
Bit 2	BP0	Block Protection Bit: (See Table 6.4 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Non-Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Non-Volatile
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Non-Volatile

Note1: WEL bit can be written by WREN and WRDI commands, but cannot by WRSR command.

The BP0, BP1, BP2, BP3, QE, and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP0, BP1, BP2, BP3, QE, and SRWD bits were set to “0” at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

WIP bit: Write In Progress (WIP) is read-only, and can be used to detect the progress or completion of a Program, Erase, or Write/Set Non-Volatile/OTP Register operation. WIP is set to “1” (busy state) when the device is executing the operation. During this time the device will ignore further instructions except for Read Status/Function/Extended Read Register and Software/Hardware Reset instructions. In addition to the instructions, an Erase/Program Suspend instruction also can be executed during a Program or an Erase operation. When an operation has completed, WIP is cleared to “0” (ready state) whether the operation is successful or not and the device is ready for further instructions.

WEL bit: Write Enable Latch (WEL) indicates the status of the internal write enable latch. When WEL is “0”, the internal write enable latch is disabled and the write operations described in Table 6.3 are inhibited. When WEL is “1”, the Write operations are allowed. WEL bit is set by a Write Enable (WREN) instruction. Each Write Non-Volatile Register, Program and Erase instruction must be preceded by a WREN instruction. The volatile register related commands such as the Set Volatile Read Register and the Set Volatile Extended Read Register don’t require to set WEL to “1". WEL can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any Write operation.

Table 6.3 Instructions requiring WREN instruction ahead

Instructions must be preceded by the WREN instruction		
Name	**Hex Code**	**Operation**
PP	02h	Serial Input Page Program
PPQ	32h/38h	Quad Input Page Program
SER	D7h/20h	Sector Erase 4KB
BER32 (32KB)	52h	Block Erase 32KB
BER64 (64KB)	D8h	Block Erase 64KB
CER	C7h/60h	Chip Erase
WRSR	01h	Write Status Register
WRFR	42h	Write Function Register
SRPNV	65h	Set Read Parameters (Non-Volatile)
SERPNV	85h	Set Extended Read Parameters (Non-Volatile)
IRER	64h	Erase Information Row
IRP	62h	Program Information Row
WRABR	15h	Write AutoBoot Register

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. BP0~3 area assignment changed from Top or Bottom according to the TBS bit setting in Function Register. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are “0”s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to “0”, the Status Register is not write-protected. When the SRWD is set to “1” and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to “1” and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the Status Register that allows quad operation. When the QE bit is set to “0”, the pin WP# and HOLD#/RESET# are enabled. When the QE bit is set to “1”, the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD#/RESET# pin is tied directly to the power supply.

Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits

Status Register Bits				Protected Memory Area (IS25WP064A, 128Blocks)	
BP3	**BP2**	**BP1**	**BP0**	**TBS(T/B selection) = 0, Top area**	**TBS(T/B selection) = 1, Bottom area**
0	0	0	0	0 (None)	0 (None)
0	0	0	1	1 (1 block : 127th)	1 (1 block : 0th)
0	0	1	0	2 (2 blocks : 126th and 127th)	2 (2 blocks : 0th and 1st)
0	0	1	1	3 (4 blocks : 124th to 127th)	3 (4 blocks : 0th to 3rd)
0	1	0	0	4 (8 blocks : 120th to 127th)	4 (8 blocks : 0th to 7th)
0	1	0	1	5 (16 blocks : 112nd to 127th)	5 (16 blocks : 0th to 15th)
0	1	1	0	6 (32 blocks : 96th to 127th)	6 (32 blocks : 0th to 31st)
0	1	1	1	7 (64 blocks : 64th to 127th)	7 (64 blocks : 0th to 63rd)
1	x	x	x	8~15 (128 blocks : 0th to 127th) All blocks	8~15 (128 blocks : 0th to 127th) All blocks

Status Register Bits				Protected Memory Area (IS25WP032A, 64Blocks)
BP3	**BP2**	**BP1**	**BP0**	
0	0	0	0	0 (None)
0	0	0	1	1 (1 block : 63rd)
0	0	1	0	2 (2 blocks : 62nd and 63rd)
0	0	1	1	3 (4 blocks : 60th to 63rd)
0	1	0	0	4 (8 blocks : 56th to 63rd)
0	1	0	1	5 (16 blocks : 48th to 63rd)
0	1	1	0	6 (32 blocks : 32nd to 63rd)
0	1	1	1	All Blocks
1	0	0	0	
1	0	0	1	9 (32 blocks : 0th to 31st)
1	0	1	0	10 (16 blocks : 0th to 15th)
1	0	1	1	11 (8 blocks : 0th to 7th)
1	1	0	0	12 (4 blocks : 0th to 3rd)
1	1	0	1	13 (2 blocks : 0th and 1st)
1	1	1	0	14 (1 block : 0th)
1	1	1	1	15 (None)

Note: x is don't care

6.2 FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and Table 6.6

Table 6.5 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0	ESUS	PSUS	TBS	Dedicated RESET# Disable
Default	0	0	0	0	0	0	0	0 or 1

Note: TBS bit is Reserved in 32Mb.

Table 6.6 Function Register Bit Definition

Bit	Name	Definition	Read /Write	Type
Bit 0	Dedicated RESET# Disable	Dedicated RESET# Disable “0” indicates Dedicated RESET# was enabled “1” indicates Dedicated RESET# was disabled	R/W for 0 R only for 1	OTP
Bit 1	TBS	Top/Bottom Selection. (See Table 6.4 for details) “0” indicates Top area “1” indicates Bottom area	R/W	OTP
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	Volatile
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
Bit 4	IR Lock 0	Lock the Information Row 0: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 5	IR Lock 1	Lock the Information Row 1: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 6	IR Lock 2	Lock the Information Row 2: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 7	IR Lock 3	Lock the Information Row 3: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP

Note: Once OTP bits of Function Register are written to “1”, it cannot be modified to “0” any more.

Dedicated RESET# Disable bit: The default status of the bit is dependent on part number. The device with dedicated RESET# can be programmed to “1” to disable dedicated RESET# function to move RESET# function to RESET#/Hold# pin (or ball). So the device with dedicated RESET# can be used for dedicated RESET# application and RESET#/HOLD# application.

TBS bit: BP0~3 area assignment can be changed from Top (default) to Bottom by setting TBS bit to “1”. However, once Bottom is selected, it cannot be changed back to Top since TBS bit is OTP. See Table 6.4 for details.

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to “1” after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to “0”.

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is “1” after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to “0”.

IR Lock bit 0 ~ 3: The default is “0” so that the Information Row can be programmed. If the bit set to “1”, the Information Row can’t be programmed. Once it set to “1”, it cannot be changed back to “0” since IR Lock bits are OTP.

6.3 READ REGISTER AND EXTENDED READ REGISTER

Read Register format and Bit definitions are described below. Read Register and Extended Read Register are rewritable non-volatile. It consists of a pair of non-volatile register and volatile register respectively. During power up sequence, volatile register will be loaded with the value of non-volatile value.

6.3.1 READ REGISTER

Table 6.7 and Table 6.8 define all bits that control features in SPI/QPI modes. HOLD#/RESET# pin selection (P7) bit is used to select HOLD# pin or RESET# pin in SPI mode when QE="0" and RESET# Disable bit in Functional Register is "1". For 16-pin SOIC or 24-ball TFBGA with dedicated RESET# device, HOLD# will be selected regardless of P7 bit setting when QE="0" in SPI mode.

The Dummy Cycle bits (P6, P5, P4, P3) define how many dummy cycles are used during various READ modes. The wrap selection bits (P2, P1, P0) define burst length with an enable bit.

The SET READ PARAMETERS Operations (SRPNV: 65h, SRPV: C0h or 63h) are used to set all the Read Register bits, and can thereby define HOLD#/RESET# pin selection, dummy cycles, and burst length with wrap around. SRPNV is used to set the non-volatile register and SRPV is used to set the volatile register.

Table 6.7 Read Register Parameter Bit Table

	P7	P6	P5	P4	P3	P2	P1	P0
	HOLD#/ RESET#	Dummy Cycles	Dummy Cycles	Dummy Cycles	Dummy Cycles	Wrap Enable	Burst Length	Burst Length
Default	0	0	0	0	0	0	0	0

Table 6.8 Read Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
P0	Burst Length	Burst Length	R/W	Non-Volatile and Volatile
P1	Burst Length	Burst Length	R/W	Non-Volatile and Volatile
P2	Burst Length Set Enable	Burst Length Set Enable Bit: "0" indicates disable (default) "1" indicates enable	R/W	Non-Volatile and Volatile
P3	Dummy Cycles	Number of Dummy Cycles: Bits1 to Bit4 can be toggled to select the number of dummy cycles (1 to 15 cycles)	R/W	Non-Volatile and Volatile
P4	Dummy Cycles		R/W	Non-Volatile and Volatile
P5	Dummy Cycles		R/W	Non-Volatile and Volatile
P6	Dummy Cycles		R/W	Non-Volatile and Volatile
P7 [1]	HOLD#/ RESET#	HOLD#/RESET# pin selection bit: when QE bit = "0" in SPI mode "0" indicates the HOLD# pin is selected (default) "1" indicates the RESET# pin is selected	R/W	Non-Volatile and Volatile

Note1: The device with a dedicated RESET# will select HOLD# regardless of P7 bit setting when QE="0" in SPI mode. When QE="1" or in QPI mode, P7 bit setting will be ignored since the pin becomes IO3.

Table 6.9 Burst Length Data

	P1	P0
8 bytes	0	0
16 bytes	0	1
32 bytes	1	0
64 bytes	1	1

Table 6.10 Wrap Function

Wrap around boundary	**P2**
Whole array regardless of P1 and P0 value	0
Burst Length set by P1 and P0	1

Table 6.11 Read Dummy Cycles vs Max Frequency

P[6:3]	Dummy Cycles[2,3]	Fast Read[5] 0Bh	Fast Read[5] 0Bh	Fast Read Dual Output 3Bh	Fast Read Dual IO BBh	Fast Read Quad Output 6Bh	Fast Read Quad IO EBh	FRDTR 0Dh	FRDDTR BDh	FRQDTR EDh
		SPI	QPI	SPI	SPI	SPI	SPI, QPI	SPI/QPI	SPI[4]	SPI, QPI
0	Default[1]	133MHz	104MHz	133MHz	115MHz	133MHz	104MHz	66/66MHz	66MHz	66MHz
1	1	84MHz	33MHz	84MHz	60MHz	66MHz	33MHz	50/20MHz	33MHz	20MHz
2	2	104MHz	50MHz	104MHz	84MHz	80MHz	50MHz	66/33MHz	50MHz	33MHz
3	3	133MHz	60MHz	115MHz	104MHz	90MHz	60MHz	66/46MHz	66MHz	46MHz
4	4	133MHz	70MHz	133MHz	115MHz	104MHz	70MHz	66/60MHz	66MHz	60MHz
5	5	133MHz	84MHz	133MHz	133MHz	115MHz	84MHz	66/66MHz	66MHz	66MHz
6	6	133MHz	104MHz	133MHz	133MHz	133MHz	104MHz	66/66MHz	66MHz	66MHz
7	7	133MHz	115MHz	133MHz	133MHz	133MHz	115MHz	66/66MHz	66MHz	66MHz
8	8	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
9	9	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
10	10	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
11	11	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
12	12	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
13	13	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
14	14	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz
15	15	133MHz	133MHz	133MHz	133MHz	133MHz	133MHz	66/66MHz	66MHz	66MHz

Notes:

1. **Default dummy cycles are as follows.**

Operation	Command		Dummy Cycles		Comment
	Normal mode	DTR mode	Normal mode	DTR mode	
Fast Read SPI	0Bh	0Dh	8	8	RDUID, RDSFDP, IRRD instructions are also applied.
Fast Read QPI	0Bh	0Dh	6	6	
Fast Read Dual Output	3Bh	-	8	-	
Fast Read Dual IO SPI	BBh	BDh	4	4	
Fast Read Quad Output	6Bh	-	8	-	
Fast Read Quad IO SPI, QPI	EBh	EDh	6	6	

2. **Enough number of dummy cycles must be applied to execute properly the AX read operation.**
3. **Must satisfy bus I/O contention. For instance, if the number of dummy cycles and AX bit cycles are same, then X must be Hi-Z.**
4. **QPI is not available for FRDDTR command.**
5. **RDUID, RDSFDP, IRRD instructions are also applied.**

6.3.2 EXTENDED READ REGISTER

Table 6.12 and Table 6.13 define all bits that control features in SPI/QPI modes. The ODS2, ODS1, ODS0 (EB7, EB6, EB5) bits provide a method to set and control driver strength. The four bits (EB3, EB2, EB1, EB0) are read-only bits and may be checked to know what the WIP status is or whether there is an error during an Erase, Program, or Write/Set Register operation. These bits are not affected by SERPNV or SERPV commands. EB4 bit remains reserved for future use.

The SET EXTENDED READ PARAMETERS Operations (SERPNV: 85h, SERPV: 83h) are used to set all the Extended Read Register bits, and can thereby define the output driver strength used during READ modes. SRPNV is used to set the non-volatile register and SRPV is used to set the volatile register.

Table 6.12 Extended Read Register Bit Table

	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
	ODS2	ODS1	ODS0	Reserved	E_ERR	P_ERR	PROT_E	WIP
Default	1	1	1	1	0	0	0	0

Table 6.13 Extended Read Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
EB0	WIP	Write In Progress Bit: Has exactly same function as the bit0 (WIP) of Status Register “0”: Ready, “1”: Busy	R	Volatile
EB1	PROT_E	Protection Error Bit: "0" indicates no error "1" indicates protection error in an Erase or a Program operation	R	Volatile
EB2	P_ERR	Program Error Bit: "0" indicates no error "1" indicates an Erase operation failure or protection error	R	Volatile
EB3	E_ERR	Erase Error Bit: "0" indicates no error "1" indicates a Program operation failure or protection error	R	Volatile
EB4	Reserved	Reserved	R	Reserved
EB5	ODS0	Output Driver Strength: Output Drive Strength can be selected according to Table 6.14	R/W	Non-Volatile and Volatile
EB6	ODS1		R/W	Non-Volatile and Volatile
EB7	ODS2		R/W	Non-Volatile and Volatile

Table 6.14 Driver Strength Table

ODS2	ODS1	ODS0	Description	Remark
0	0	0	Reserved	
0	0	1	12.50%	
0	1	0	25%	
0	1	1	37.50%	
1	0	0	Reserved	
1	0	1	75%	
1	1	0	100%	
1	1	1	50%	Default

WIP bit: The definition of the WIP bit is exactly same as the one of Status Register.

PROT_E bit: The Protection Error bit indicates whether an Erase or Program operation has attempted to modify a protected array sector or block, or to access a locked Information Row region. When the bit is set to “1” it indicates that there was an error or errors in previous Erase or Program operations. See Table 6.15 for details.

P_ERR bit: The Program Error bit indicates whether a Program or Write/Set OTP/Non-Volatile Register operation has succeeded or failed, or whether a Program operation has attempted to program a protected array sector/block or a locked Information Row region. When the bit is set to “1” it indicates that there was an error or errors in previous Program or Write/Set Register operations. See Table 6.15 for details.

E_ERR bit: The Erase Error bit indicates whether an Erase or Write/Set OTP/Non-Volatile Register operation has succeeded or failed, or whether an Erase operation has attempted to erase a protected array sector/block or a locked Information Row region. When the bit is set to “1” it indicates that there was an error or errors in previous Erase or Write/Set Non-Volatile Register operations. See Table 6.15 for details.

Table 6.15 Instructions to set PROT_E, P_ERR, or E_ERR bit

Instructions	Description
PP/PPQ	The commands will set the P_ERR if there is a failure in the operation. Attempting to program within the protected array sector/block or within an erase suspended sector/block will result in a programming error with P_ERR and PROT_E set to “1”.
IRP	The command will set the P_ERR if there is a failure in the operation. In attempting to program within a locked Information Row region, the operation will fail with P_ERR and PROT_E set to 1.
WRSR/WRABR/SRPNV/ SERPNV	The update process for the non-volatile register bits involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails, the related error bit (P_ERR or E_ERR) will be set to “1”. Only for WRSR command, when Status Register is write-protected by SRWD bit and WP# pin, attempting to write the register will set PROT_E and E_ERR to “1”.
WRFR	The commands will set the P_ERR if there is a failure in the operation.
SER/BER32K/BER64K/CER/ IRER	The commands will set the E_ERR if there is a failure in the operation. E_ERR and PROT_E will be set to “1” when the user attempts to erase a protected main memory sector/block or a locked Information Row region. However, the Chip Erase (CER) command will not set E_ERR and PROT_E if a protected sector/block is found during the command execution.

Notes:
1. **OTP bits in the Function Register may only be programmed to “1”. Writing of the bits back to “0” is ignored and no error is set.**
2. **Read only bits in registers are never modified by a command so that the corresponding bits in the Write/Set Register command data byte are ignored without setting any error indication.**
3. **Once the PROT_E, P_ERR, and E_ERR error bits are set to “1”, they remains set to “1” until they are cleared to “0” with a Clear Extended Read Register (CLERP) command. This means that those error bits must be cleared through the CLERP command. Alternatively, Hardware Reset, or Software Reset may be used to clear the bits.**
4. **Any further command will be executed even though the error bits are set to “1”.**

6.4 AUTOBOOT REGISTER

AutoBoot Register Bit (32 bits) Definitions are described in Table 6.15.

Table 6.16 AutoBoot Register Parameter Bit Table

Bits	Symbols	Function	Type	Default Value	Description
AB[31:24]	ABSA	Reserved	Reserved	00h	Reserved for future use
AB[23:5]	ABSA	AutoBoot Start Address	Non-Volatile	00000h	32 byte boundary address for the start of boot code access
AB[4:1]	ABSD	AutoBoot Start Delay	Non-Volatile	0h	Number of initial delay cycles between CE# going low and the first bit of boot code being transferred, and it is the same as dummy cycles of FRD (QE=0) or FRQIO (QE=1). Example: The number of initial delay cycles is 8 (QE=0) or 6 (QE=1) when AB[4:1]=00h (Default setting).
AB0	ABE	AutoBoot Enable	Non-Volatile	0	1 = AutoBoot is enabled 0 = AutoBoot is not enabled

7. PROTECTION MODE

The device supports hardware and software write-protection mechanisms.

7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, SRWD, and QE in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage (V_{WI}) is specified in the section 9.8 POWER-UP AND POWER-DOWN. All write sequence will be ignored when Vcc drops to V_{WI}.

Table 7.1 Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Note: Before the execution of any program, erase or write Status Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

7.2 SOFTWARE WRITE PROTECTION

The device also provides a software write protection feature. The Block Protection (TBS, BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.