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IS25LP128F IS25WP128F

128Mb

SERIAL FLASH MEMORY WITH 166MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

DATA SHEET

128Mb

SERIAL FLASH MEMORY WITH 166MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

FEATURES

- **Industry Standard Serial Interface**
  - IS25LP128F: 128Mbit/16Mbyte
  - IS25WP128F: 128Mbit/16Mbyte
  - 3 or 4 Byte Addressing Mode
  - Supports Standard SPI, Fast, Dual, Dual I/O, Quad, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
  - Software & Hardware Reset
  - Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**
  - 80MHz Normal Read
  - Up to166Mhz Fast Read
  - Up to 80MHz DTR (Dual Transfer Rate)
  - Equivalent Throughput of 664 Mb/s
  - Selectable Dummy Cycles
  - Configurable Drive Strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 Erase/Program Cycles
  - More than 20-year Data Retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 Byte per Page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous Read 8/16/32/64 Byte Burst Wrap
  - Selectable Burst Length
  - QPI for Reduced Instruction Overhead
  - AutoBoot Operation

- **Low Power with Wide Temp. Ranges**
  - Single Voltage Supply
    IS25LP: 2.30V to 3.60V
    IS25WP: 1.65V to 1.95V
  - 10 mA Active Read Current
  - 8 µA Standby Current
  - 1 µA Deep Power Down
  - Temp Grades:
    Extended: -40°C to +105°C
    Auto Grade (A3) : -40°C to +125°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Advanced Sector/Block Protection
  - Top/Bottom Block Protection
  - Power Supply Lock Protection
  - 4x256 Byte Dedicated Security Area with OTP User-lockable Bits
  - 128 bit Unique ID for Each Device (Call Factory)

- **Industry Standard Pin-out & Packages**
  - M =16-pin SOIC 300mil
  - B = 8-pin SOIC 208mil
  - K = 8-contact WSON 6x5mm
  - L = 8-contact WSON 8x6mm
  - G = 24-ball TFBGA (4x6 ball array)
  - H = 24-ball TFBGA (5x5 ball array)
  - KGD (Call Factory)

GENERAL DESCRIPTION

The IS25LP128F and IS25WP128F Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 166MHz allow for equivalent clock rates of up to 664MHz (166MHz x 4) which equates to 83Mbytes/s of data throughput. The IS25xP series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256 bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

Supply Voltage & Temperature Range vs. Maximum Speed

	Voltage & Temp.	Speed
IS25LP (3.0V typ.)	2.30~3.6V, 125°C	133MHz
	2.70~3.6V, 125°C	166MHz
IS25WP (1.8V typ.)	1.65~1.95V, 125°C	133MHz
	1.70~1.95V, 105°C	166MHz(1)

Note:
1. Values are guaranteed by characterization and not 100% tested in production.

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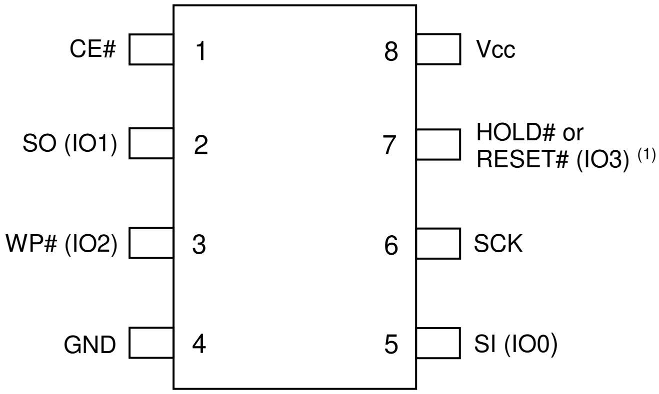
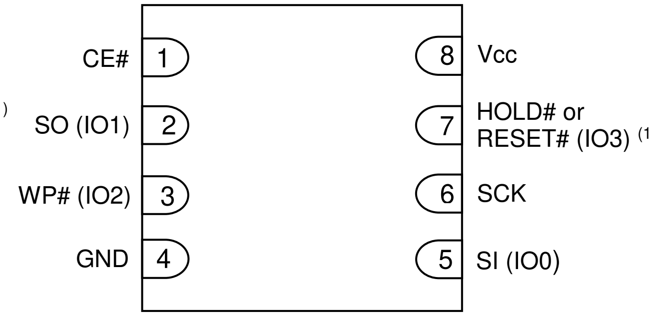
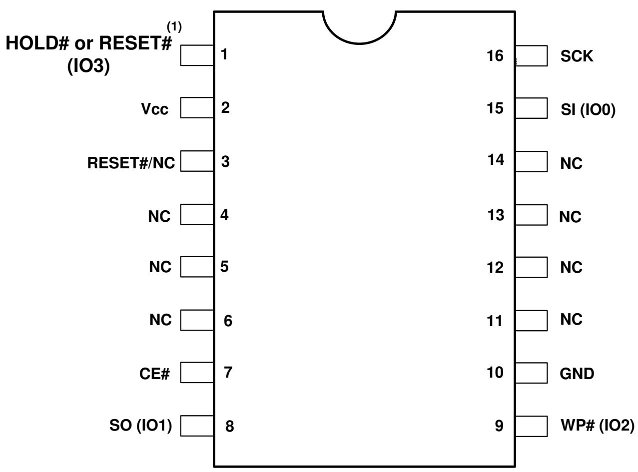
1. PIN CONFIGURATION



8-pin SOIC 208mil

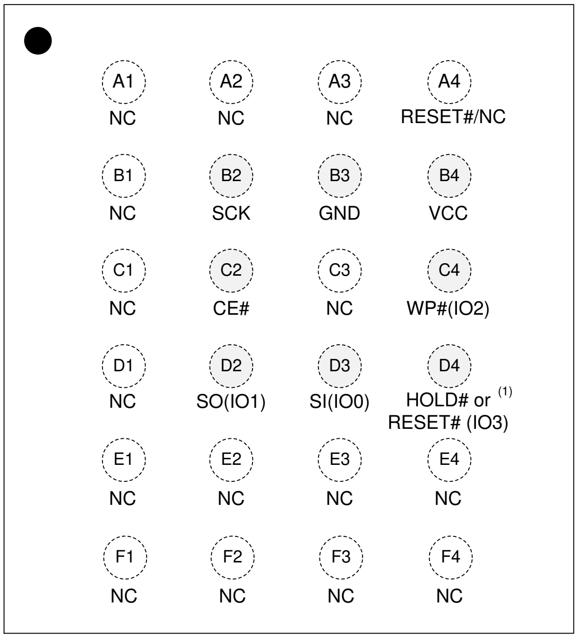


8-contact WSON 6x5mm
8-contact WSON 8x6mm



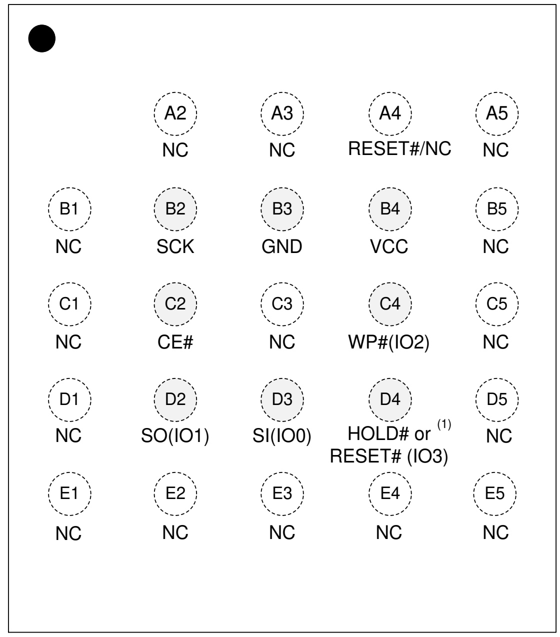
16-pin SOIC 300mil (Package: M)

Top View, Balls Facing Down



24-ball TFBGA 6x8mm (4x6 ball array)
(Package: G)

Top View, Balls Facing Down



24-ball TFBGA 6x8mm (5x5 ball array)
(Package: H)

Note:

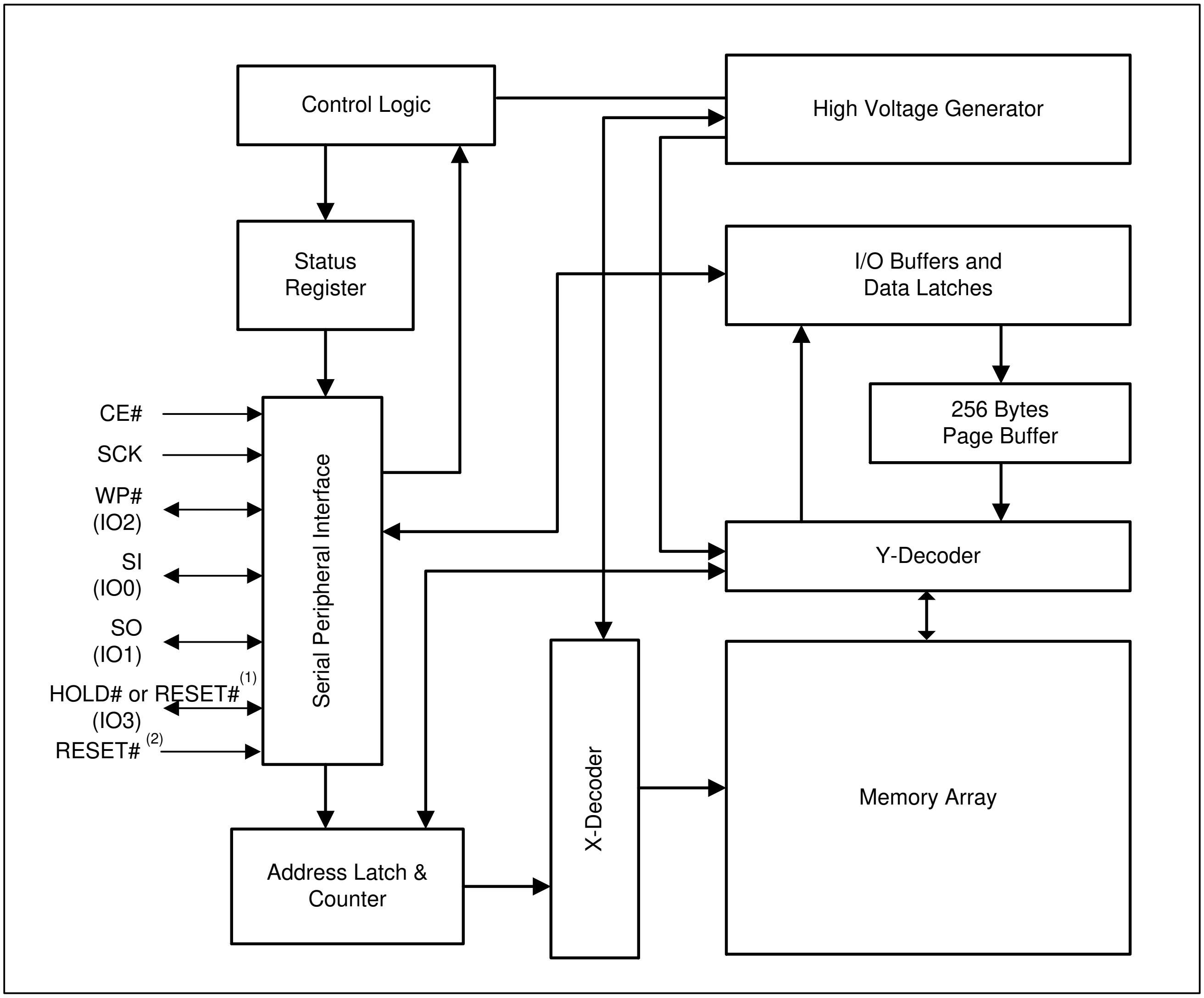
1. **The pin can be configured as Hold# or Reset# by setting P7 bit of the Read Register. Pin default is Hold# (IO3).**

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to “1” and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to “0”, the Status Register is not write-protected regardless of WP# state. When the QE bit is set to “1”, the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3) or RESET# (IO3)	INPUT/OUTPUT	**HOLD# or RESET#/Serial Data IO (IO3):** When the QE bit of Status Register is set to “1”, HOLD# pin or RESET# is not available since it becomes IO3. **Most packages except for 16-pin SOIC and 24-ball BGA:** When QE=0, the pin acts as HOLD# or RESET# and either one can be selected by the P7 bit setting in Read Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1. **16-pin SOIC and 24-ball BGA packages :** - When QE=0 and Dedicated RESET# is Enabled (Default), the pin acts as HOLD# regardless of the P7 bit setting in Read Register. - When QE=0 and Dedicated RESET# is Disabled, the pin acts as HOLD# or RESET# and either one can be selected by the P7 bit setting in Read Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state.

SYMBOL	TYPE	DESCRIPTION
RESET#	INPUT/OUTPUT	**RESET#:** This dedicated RESET# is available in 16-pin SOIC and 24-ball BGA packages. The RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. Dedicated RESET# function can be Disabled when bit 0 of Function Register = 1. It has an internal pull-up resistor and may be left floating if not used.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left uncommitted.

3. BLOCK DIAGRAM



Note:

1: In case of 16-pin SOIC or 24-ball TFBFA, when QE=0 and Dedicated RESET# is Disabled, the pin acts as HOLD# or RESET# and either one can be selected by the P7 bit setting in Read Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1.

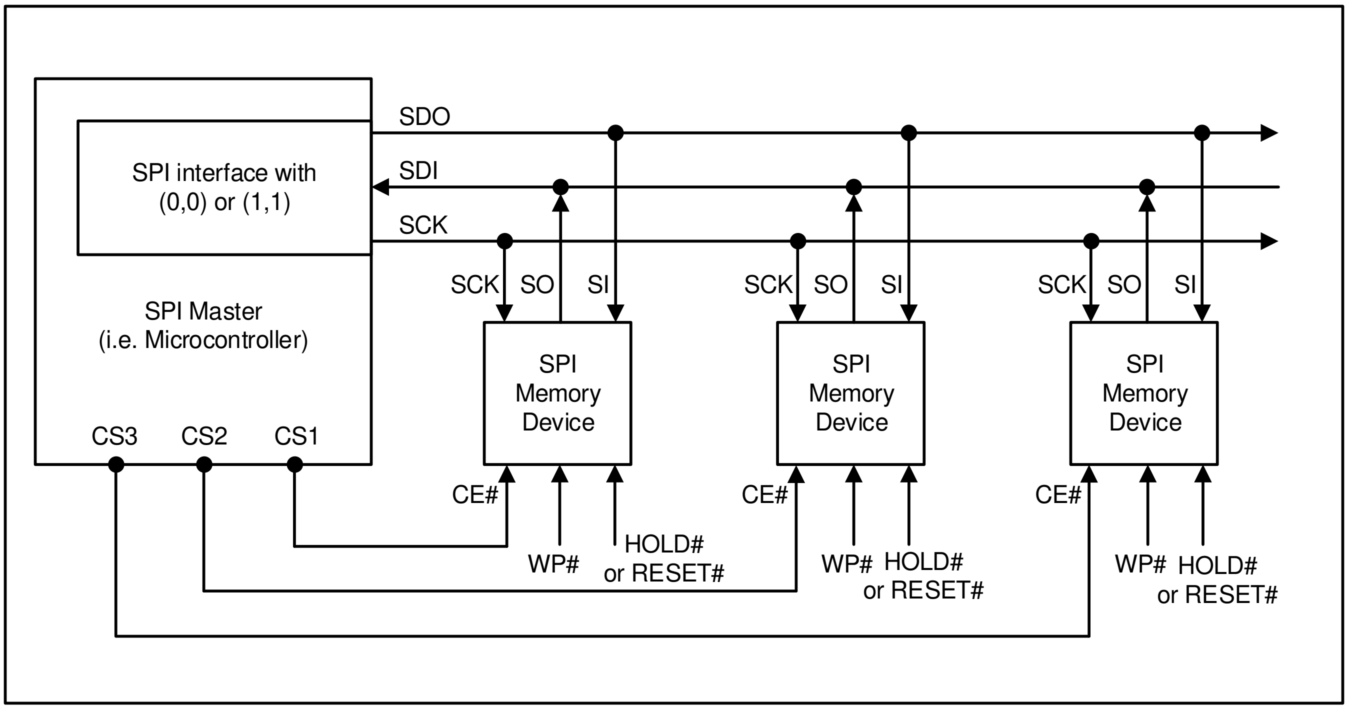
4. SPI MODES DESCRIPTION

Multiple IS25LP128F devices or multiple IS25WP128F devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at “0” (SCK = 0) for Mode 0 and the clock remains at “1” (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:
1. In case of 16-pin SOIC and 24-ball TFBGA, dedicated RESET# is supported.
2. SI and SO pins become bidirectional IO0 and IO1 respectively during Dual I/O mode and SI, SO, WP#, and HOLD# pins become bidirectional IO0, IO1, IO2, and IO3 respectively during Quad I/O or QPI mode.

Figure 4.2 SPI Mode Support

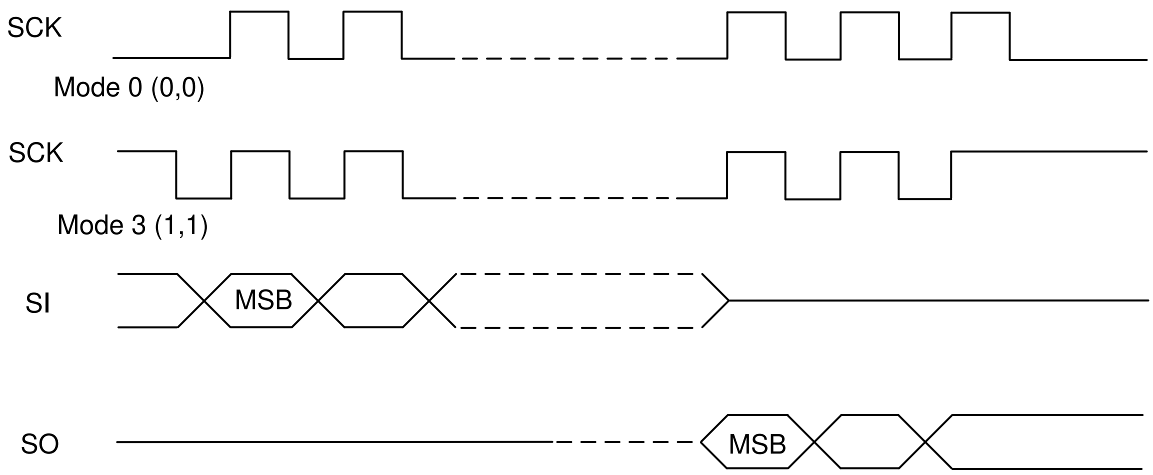
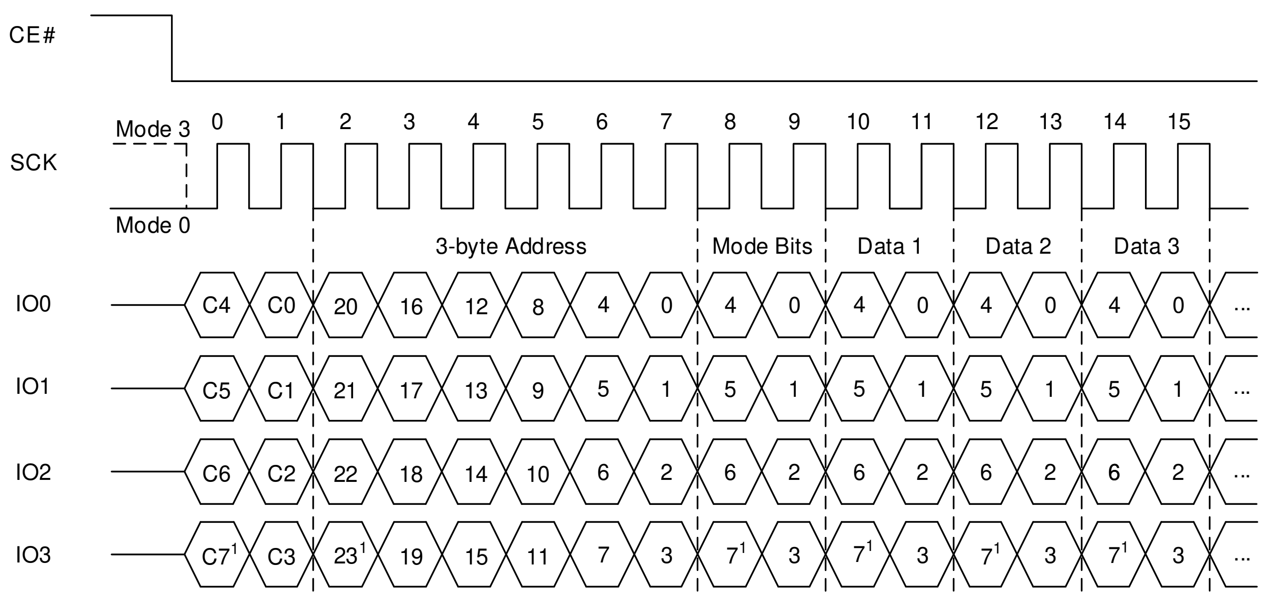


Figure 4.3 QPI Mode Support



Note1: MSB (Most Significant Bit)

5. SYSTEM CONFIGURATION

The memory array is divided into uniform 4 Kbyte sectors or uniform 32/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses

Memory Density	Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
128Mb	Block 0	Block 0	Sector 0	4	000000h – 000FFFh
			:	:	:
		Block 1	:	:	:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Block 2	Sector 16	4	010000h – 010FFFh
			:	:	:
		Block 3	:	:	:
			Sector 31	4	01F000h - 01FFFFh
	Block 2	Block 4	Sector 32	4	020000h – 020FFFh
			:	:	:
		Block 5	:	:	:
			Sector 47	4	02F000h – 02FFFFh
	:	:	:	:	:
	Block 63	Block 126	Sector 1008	4	3F0000h – 3F0FFFh
			:	:	:
		Block 127	:	:	:
			Sector 1023	4	3FF000h – 3FFFFFh
	:	:	:	:	:
	Block 127	Block 254	Sector 2032	4	7F0000h – 7F0FFFh
			:	:	:
		Block 255	:	:	:
			Sector 2047	4	7FF000h – 7FFFFFh
	:	:	:	:	:
	Block 254	Block 508	Sector 4064	4	FE0000h – FE0FFFh
			:	:	:
		Block 509	:	:	:
			Sector 4079	4	FEF000h – FEFFFFh
	Block 255	Block 510	Sector 4080	4	FF0000h – FF0FFFh
			:	:	:
		Block 511	:	:	:
			Sector 4095	4	FFF000h – FFFFFFh

5.2 SERIAL FLASH DISCOVERABLE PARAMETERS

The Serial Flash Discoverable Parameters (SFDP) standard defines the structure of the SFDP database within the memory device. SFDP is the standard of JEDEC JESD216.
The JEDEC-defined header with Parameter ID FF00h and related Basic Parameter Table is mandatory. Additional parameter headers and tables are optional.

Table 5.2 Signature and Parameter Identification Data Values

Description		Address (Byte)	Address (Bit)	Data
SFDP Signature		00h	7:0	53h
		01h	15:8	46h
		02h	23:16	44h
		03h	31:24	50h
SFDP Revision	Minor	04h	7:0	06h
	Major	05h	15:8	01h
Number of Parameter Headers (NPH)		06h	23:16	**00h**
Unused		07h	31:24	FFh
Parameter ID LSB		08h	7:0	00h
Parameter Minor Revision		09h	15:8	06h
Parameter Major Revision		0Ah	23:16	01h
Parameter Table Length (in DWPRDs)		0Bh	31:24	10h
Basic Flash Parameter Table Pointer (PTP)		0Ch	7:0	30h
		0Dh	15:8	00h
		0Eh	23:16	00h
Parameter ID MSB		0Fh	31:24	FFh

Table 5.3 JEDEC Basic Flash Parameter Table

Description	Address (Byte)	Address (Bit)	Data
Minimum Sector Erase Sizes	30h	1:0	01b
Write Granularity		2	1b
Volatile Status Register Block Protect bits		3	0b
Write Enable Instruction Select for writing to Volatile Status Register		4	0b
Unused		7:5	111b
4KB Erase Instruction	31h	15:8	20h
Supports (1-1-2) Fast Read	32h	16	1b
Address Bytes		18:17	01b
Supports Double Transfer Rate (DTR) Clocking		19	1b
Supports (1-2-2) Fast Read		20	1b
Supports (1-4-4) Fast Read		21	1b
Supports (1-1-4) Fast Read		22	1b
Unused		23	1b
Reserved	33h	31:24	FFh
Flash memory Density (bits)	34h	7:0	FFh
	35h	15:8	FFh
	36h	23:16	FFh
	37h	31:24	07h
1-4-4 Fast Read Wait Cycle Count	38h	4:0	00100b
1-4-4 Fast Read Mode bit Cycle Count		7:5	010b
1-4-4 Fast Read Instruction	39h	15:8	EBh
1-1-4 Fast Read Wait Cycle Count	3Ah	20:16	01000b
1-1-4 Fast Read Mode bit Cycle Count		23:21	000b
1-1-4 Fast Read Instruction	3Bh	31:24	6Bh
1-1-2 Fast Read Wait Cycle Count	3Ch	4:0	01000b
1-1-2 Fast Read Mode bit Cycle Count		7:5	000b
1-1-2 Fast Read Instruction	3Dh	15:8	3Bh
1-2-2 Fast Read Wait Cycle Count	3Eh	20:16	00000b
1-2-2 Fast Read Mode bit Cycle Count		23:21	100b
1-2-2 Fast Read Instruction	3Fh	31:24	BBh

Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description	Address (Byte)	Address (Bit)	Data
Supports (2-2-2) Fast Read	40h	0	0
Reserved		3:1	111b
Supports (4-4-4) Fast Read		4	1
Reserved		7:5	111b
Reserved	43:41h	31:8	FFFFFFh
Reserved	45:44h	15:0	FFFFh
2-2-2 Fast Read Wait Cycle Count	46h	20:16	00000b
2-2-2 Fast Read Mode bit Cycle Count		23:21	000b
2-2-2 Fast Read Instruction	47h	31:24	FFh
Reserved	49:48h	15:0	FFFFh
4-4-4 Fast Read Wait Cycle Count	4Ah	20:16	00100b
4-4-4 Fast Read Mode bit Cycle Count		23:21	010b
4-4-4 Fast Read Instruction	4Bh	31:24	EBh
Erase Type 1 Size (4KB)	4Ch	7:0	0Ch
Erase Type 1 Instruction	4Dh	15:8	20h
Erase Type 2 Size (32KB)	4Eh	23:16	0Fh
Erase Type 2 Instruction	4Fh	31:24	52h
Erase Type 3 Size (64KB)	50h	7:0	10h
Erase Type 3 Instruction	51h	15:8	D8h
Erase Type 4 Size (256KB)	52h	23:16	00h
Erase Type 4 Instruction	53h	31:24	FFh
Multiplier from typical erase time to maximum erase time	57:54h	3:0	0010b
Sector Type 1 ERASE time (typ)		8:4	00110b
		10:9	01b
Sector Type 2 ERASE time (typ)		15:11	01000b
		17:16	01b
Sector Type 3 ERASE time (typ)		22:18	01010b
		24:23	01b
Sector Type 4 ERASE time (typ)		29:25	00000b
		31:30	00b

Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description	Address (Byte)	Address (Bit)	Data
Multiplier from typical time to maximum time for page or byte PROGRAM	58h	3:0	0010b
Page size		7:4	1000b
Page Program Typical time	5Ah:59h	12:8	11000b
		13	0b
Byte Program Typical time, first byte		17:14	0111b
		18	0b
Byte Program Typical time, additional byte		22:19	0000b
		23	0b
Chip Erase, Typical time	5Bh	28:24	01000b
Units		30:29	10b
Reserved		31	1b
Prohibited Operations During Program Suspend	5Ch	3:0	1100b
Prohibited Operations During Erase Suspend		7:4	1110b
Reserved	5Eh:5Dh	8	1b
Program Resume to Suspend Interval		12:9	0110b
Suspend in-progress program max latency		17:13	01100b
		19:18	10b
Erase Resume to Suspend Interval		23:20	0110b
Suspend in-progress erase max latency	5Fh	28:24	01100b
		30:29	10b
Suspend /Resume supported		31	0b
Program Resume Instruction	60h	7:0	7Ah
Program Suspend Instruction	61h	15:8	75h
Resume Instruction	62h	23:16	7Ah
Suspend Instruction	63h	31:24	75h
Reserved	64h	1:0	11b
Status Register Polling Device Busy		7:2	111101b

Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description		Address (Byte)	Address (Bit)	Data
Exit Deep Power-down to next operation delay	3V	67h:65h	12:8	00010b
	1.8V			00100b
Exit Deep Power-down to next operation delay Units			14:13	01b
Exit Deep Power-down Instruction			22:15	ABh
Enter Deep Power-down Instruction			30:23	B9h
Deep Power-down Supported			31	0b
4-4-4 mode disable sequences (QPIDI)		69h:68h	3:0	1010b
4-4-4 mode enable sequences (QPIEN)			8:4	00100b
0-4-4 Mode Supported			9	1b
0-4-4 Mode Exit Method			15:10	110000b
0-4-4 Mode Entry Method:		6Ah	19:16	1100b
Quad Enable Requirements (QER)			22:20	010b
Hold or RESET Disable			23	0b
Reserved		6Bh	31:24	FFh
Volatile or Non-Volatile Register and Write Enable (WREN) Instruction for Status Register 1		6Ch	6:0	1101000b
Reserved			7	1b
Soft Reset and Rescue Sequence Support		6Eh:6Dh	13:8	110000b
Exit 4-Byte Addressing			23:14	1111101000b
Enter 4-Byte Addressing		6Fh	31:24	10101001b

6. REGISTERS

The device has various sets of Registers: Status, Function, Read, Extended Read and Autoboot.
When the register is read continuously, the same data is output repeatedly until CE# goes HIGH.

6.1 STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Tables 6.1 & 6.2.
Status Read Register consist of a pair of writable non-volatile register and volatile register, respectively. During power up sequence, volatile register will be loaded with the value of non-volatile value.

But only volatile Status Register is readable with Read Status Register Operation (RDSR, 05h)

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready (default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W[1]	Volatile
Bit 2	BP0	Block Protection Bit: (See Tables 6.4 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Non-Volatile and Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Non-Volatile and Volatile
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Non-Volatile and Volatile

Note: WEL bit can be written by WREN and WRDI commands, but cannot by WRSR and VSRWE command.

The BP0, BP1, BP2, BP3, QE, and SRWD are non-volatile and volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP0, BP1, BP2, BP3, QE, and SRWD bits were set to “0” at factory. Only volatile Status Register is readable with Read Status Register Operation (RDSR, 05h)

The function of Status Register bits are described as follows:

WIP bit: Write In Progress (WIP) is read-only, and can be used to detect the progress or completion of a Program, Erase, Write/Set Non-Volatile/OTP Register, or Gang Sector/Block Lock/Unlock operation. WIP is set to “1” (busy state) when the device is executing the operation. During this time the device will ignore further instructions except for Read Status/Function/Extended Read Register and Software/Hardware Reset instructions. In addition to the instructions, an Erase/Program Suspend instruction also can be executed during a Program or Erase operation. When an operation has completed, WIP is cleared to “0” (ready state) whether the operation is successful or not and the device is ready for further instructions.

WEL bit: Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When WEL bit is “0”, the internal write enable latch is disabled and the Write operations described in Table 6.3 are inhibited. When WEL bit is “1”, the Write operations are allowed. WEL bit is set by a Write Enable (WREN, 06h) instruction. Most of Write Non-Volatile/Volatile Register, Program and Erase instruction must be preceded by a WREN instruction.

But Write Volatile Status Register does not require to set WEL bit to “1” by WREN (06h) instruction. Instead it requires a Volatile Status Register Write Enable (50h) instruction prior to Write Status Register (01h) instruction. Volatile Status Register Write Enable (50h) instruction does not set the Write Enable Latch (WEL) bit to “1”.

WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any Write Non-Volatile Register, Program and Erase operation.

Table 6.3 Instructions requiring WREN instruction ahead

Instructions must be preceded by the WREN instruction		
Name	**Hex Code**	**Operation**
PP	02h	Serial Input Page Program (3-byte or 4-byte Address)
4PP	12h	Serial Input Page Program (4-byte Address)
PPQ	32h/38h	Quad Input Page Program (3-byte or 4-byte Address)
4PPQ	34h/3Eh	Quad Input Page Program (4-byte Address)
SER	D7h/20h	Sector Erase 4KB (3-byte or 4-byte Address)
4SER	21h	Sector Erase 4KB (4-byte Address)
BER32 (32KB)	52h	Block Erase 32KB (3-byte or 4-byte Address)
4BER32 (32KB)	5Ch	Block Erase 32KB (4-byte Address)
BER64 (64KB)	D8h	Block Erase 64KB (3-byte or 4-byte Address)
4BER64 (64KB)	DCh	Block Erase 64KB (4-byte Address)
CER	C7h/60h	Chip Erase
WRSR(1)	01h	Write Non-Volatile Status Register
WRFR	42h	Write Function Register
SRPNV	65h	Set Read Parameters (Non-Volatile)
SRPV(2)	63h	Set Read Parameters (Volatile)
SERPNV	85h	Set Extended Read Parameters (Non-Volatile)
SERPV	83h	Set Extended Read Parameters (Volatile)
IRER	64h	Erase Information Row
IRP	62h	Program Information Row
WRABR	15h	Write AutoBoot Register
WRBRNV	18h	Write Non-Volatile Bank Address Register
WRBRV(2)	C5h	Write Volatile Bank Address Register
WRDYB	FBh	Write DYB Register (4-byte Address)
4WRDYB	E1h	Write DYB Register (3-byte or 4-byte Address)
PGPPB	FDh	Write PPB (3-byte or 4-byte Address)
4PGPPB	E3h	Write PPB (4-byte Address)
ERPPB	E4h	Erase PPB
PGASP	2Fh	Program ASP
WRPLB	A6h	Write PPB Lock Bit
SFRZ	91h	Set FREEZE bit
GBLK	7Eh	GANG Sector/Block Lock
GBUN	98h	GANG Sector/Block Unlock
PGPWD	E8h	Program Password

Notes:
1. **Volatile Status Register Write Enable (50h) command is required for Write Volatile Status Register operation with WRSR(01) command.**
2. **C0h command for SRPV operation and 17h command for WRBRV operation do not require WREN command ahead.**

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD#/RESET# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to "0" if WP# or HOLD#/RESET# pin (or ball) is tied directly to the power supply.

Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits

Status Register Bits				Protected Memory Area (128Mb, 256Blocks)	
BP3	BP2	BP1	BP0	TBS(T/B selection) = 0, Top area	TBS(T/B selection) = 1, Bottom area
0	0	0	0	0 (None)	0 (None)
0	0	0	1	1 (1 block : 255th)	1 (1 block : 0th)
0	0	1	0	2 (2 blocks : 254th and 255th)	2(2 blocks : 0th and 1st)
0	0	1	1	3 (4 blocks : 252nd to 255th)	3 (4 blocks : 0th to 3rd)
0	1	0	0	4 (8 blocks : 248th to 255th)	4 (8 blocks : 0th to 7th)
0	1	0	1	5 (16 blocks : 240th to 255th)	5 (16 blocks : 0th to 15th)
0	1	1	0	6 (32 blocks : 224th to 255th)	6 (32 blocks : 0th to 31st)
0	1	1	1	7 (64 blocks : 192nd to 255th)	7 (64 blocks : 0th to 63rd)
1	0	0	0	8 (128 blocks : 128th to 255th)	8 (128 blocks : 0th to 127th)
1	0	0	1	9 (256 blocks : 0th to 255th) All blocks	9 (256 blocks : 0th to 255th) All blocks
1	0	1	X(1)	10-11 (256 blocks : 0th to 255th) All blocks	10-11 (256 blocks : 0th to 255th) All blocks
1	1	x(1)	x(1)	12-15 (256 blocks : 0th to 255th) All blocks	12-15 (256 blocks : 0th to 255th) All blocks

Status Register Bits				Protected Memory Area (Optional BP Table (2), 128Mb, 256Blocks)	
BP3	BP2	BP1	BP0	TBS = 0, Top area	TBS = 1, Bottom area
0	0	0	0	0 (None)	0 (None)
0	0	0	1	1 (1 block : 255th)	1 (1 block : 0th)
0	0	1	0	2 (2 blocks : 254th and 255th)	2 (2 blocks : 0th and 1st)
0	0	1	1	3 (4 blocks : 252nd to 255th)	3 (4 blocks : 0th to 3rd)
0	1	0	0	4 (8 blocks : 248th to 255th)	4 (8 blocks : 0th to 7th)
0	1	0	1	5 (16 blocks : 240th to 255th)	5 (16 blocks : 0th to 15th)
0	1	1	0	6 (32 blocks : 224th to 255th)	6 (32 blocks : 0th to 31st)
0	1	1	1	7 (64 blocks : 192nd to 255th)	7 (64 blocks : 0th to 63rd)
1	0	0	0	8 (128 blocks : 128th to 255th)	8 (128 blocks : 0th to 127th)
1	0	0	1	9 (192 blocks : 64th to 255th)	9 (192 blocks : 0th to 191st)
1	0	1	0	10 (224 blocks : 32nd to 255th)	10 (224 blocks : 0th to 223rd)
1	0	1	1	11 (240 blocks : 16th to 255th)	11 (240 blocks : 0th to 239th)
1	1	0	0	12 (248 blocks : 8th to 255th)	12 (248 blocks : 0th to 247th)
1	1	0	1	13 (252 blocks : 4th to 255th)	13 (252 blocks : 0th to 251st)
1	1	1	0	14 (254 blocks : 2nd to 255th)	14 (254 blocks : 0th to 253rd)
1	1	1	1	15 (256 blocks : 0th to 255th)	15 (256 blocks : 0th to 255th)

Notes:
1. x is don't care
2. For Optional BP Table, see the Ordering Information (Option "B")

6.2 FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and Table 6.6.

Table 6.5 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IRL3	IRL2	IRL1	IRL0	ESUS	PSUS	TBS	Dedicated RESET# Disable
Default	0	0	0	0	0	0	0	0 or 1

Table 6.6 Function Register Bit Definition

Bit	Name	Definition	Read /Write	Type
Bit 0	Dedicated RESET# Disable	Dedicated RESET# Disable bit “0” indicates Dedicated RESET# was enabled “1” indicates Dedicated RESET# was disabled	R/W for 0 R for 1	OTP
Bit 1	TBS	Top/Bottom Selection. (See Table 6.4 for details) “0” indicates Top area. “1” indicates Bottom area.	R/W	OTP
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	Volatile
Bit 3	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
Bit 4	IR Lock 0	Lock the Information Row 0: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 5	IR Lock 1	Lock the Information Row 1: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 6	IR Lock 2	Lock the Information Row 2: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP
Bit 7	IR Lock 3	Lock the Information Row 3: “0” indicates the Information Row can be programmed “1” indicates the Information Row cannot be programmed	R/W	OTP

Note: Once OTP bits of Function Register are written to “1”, it cannot be modified to “0” any more.

Dedicated RESET# Disable bit: The default status of the bit is dependent on package type. The device with dedicated RESET# (16-pin SOIC and 24-ball BGA) can be programmed to “1” to disable dedicated RESET# function to move RESET# function to Hold#/RESET# pin (or ball). So the device with dedicated RESET# can be used for dedicated RESET# application and HOLD#/RESET# application.

TBS bit: BP0~3 area assignment can be changed from Top (default) to Bottom by setting TBS bit to “1”. However, once Bottom is selected, it cannot be changed back to Top since TBS bit is OTP. See Table 6.4 for details.

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to “1” after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to “0”.

ESUS bit: The Erase Suspend Status bit indicates when an Erase operation has been suspended. The ESUS bit is “1” after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to “0”.

IR Lock bit 0 ~ 3: The default is “0” so that the Information Row can be programmed. If the bit is set to “1”, it cannot be changed back to “0” again since IR Lock bits are OTP.