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IS25WQ040
IS25WQ020

4M/2M-BIT
1.8V QUAD SERIAL FLASH MEMORY WITH 104MHZ MULTI I/O SPI

DATA SHEET

4M/2M-BIT 1.8V QUAD SERIAL FLASH MEMORY WITH MULTI-I/O SPI

FEATURES

- **Industry Standard Serial Interface**
  - IS25WQ040: 4M-bit/ 512K-byte
  - IS25WQ020: 2M-bit/ 256K-byte
  - 256-bytes per Programmable Page Standard
  - Standard SPI/Dual/Quad Multi-I/O SPI

- **High Performance Serial Flash (SPI)**
  - 33MHz SPI Normal Read
  - 104 MHz SPI/Dual/Quad Multi-I/O SPI
  - 416 MHz equivalent Quad SPI
  - 52MB/S Continuous Data Throughput
  - Supports SPI Modes 0 and 3
  - More than 100,000 Erase/Program Cycles(1)
  - More than 20-year Data Retention

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - Continuous data read
  - Allows XIP operations (execute in place)
  - Outperforms X16 Parallel Flash

- **Flexible & Cost Efficient Memory Architecture**
  - Uniform 4 Kbyte Sectors or 32/64 Kbyte Blocks
  - Flexible 4, 32, 64 K-bytes, or Chip Erase
  - Standard Page Program 1 to 256 bytes
  - Program/Erase Suspend and Resume

- **Low Power with Wide Temp. Ranges**
  - Single 1.65V to 1.95V Voltage Supply
  - 8 mA Active Read Current (typ)
  - 15 µA Standby Current (typ.)
  - 2 µA Deep Power Down (typ.)
  - Temp Grades:
    Extended: -40°C to +105°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - 256-Byte dedicated security area, One Time Programmable (OTP) Memory
  - 128 bit Unique ID for each device (Call Factory)

- **Industry Standard Pin-out & Pb-Free Packages[2]**
  - JN = 8-pin SOIC 150mil
  - JB = 8-pin SOIC 208mil
  - JV = 8-pin VVSOP 150mil
  - JK = 8-contact WSON 6x5mm
  - JU = 8-contact USON 2x3mm
  - KGD (Call Factory)

Note2: Call Factory for other package options available

GENERAL DESCRIPTION

The IS25WQ040/020 (4M/2Mbit) Serial Flash memory offers a storage solution with flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" is for systems that have limited space, pins, and power. The IS25WQ040/020 is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which also serve as multi-function I/O pins in Dual and Quad modes (see pin descriptions). The IS25xQ series of Flash is ideal for code shadowing to RAM, execute in place (XIP) operations, and storing non-volatile data.

The memory array is organized into programmable pages of 256-bytes each. The IS25WQ040/020 supports page program mode where 1 to 256 bytes of data can be programmed into the memory with one command. Pages can be erased in groups of 4K-byte sectors, 32K-byte blocks, 64K-byte blocks, and/or the entire chip. The uniform sectors and blocks allow greater flexibility for a variety of applications requiring solid data retention.

The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad output (SPI), and Dual/Quad I/O (SPI). Clock frequencies of up to 104MHz for all read modes allow for equivalent clock rates of up to 416MHz (104MHz x 4) allowing up to 52MBytes/S of throughput. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access for a XIP (execute in place) operation. The IS25WQ040/020 is manufactured using industry leading non-volatile memory technology and offered in industry standard lead-free packages. See Ordering Information for the density and package combinations available.

Note1: 100,000 Continuous Chip and Block cycling, 100,000 Continuous Sector cycling.

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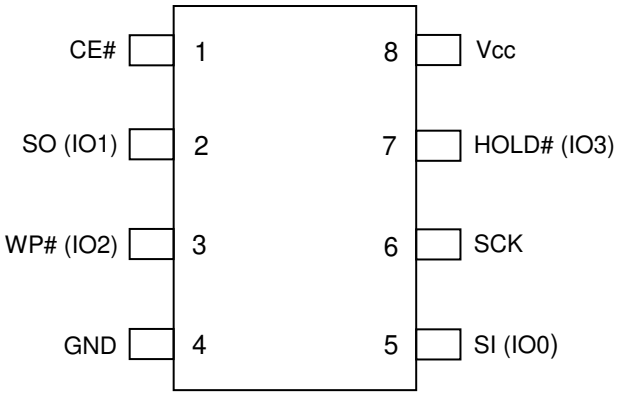
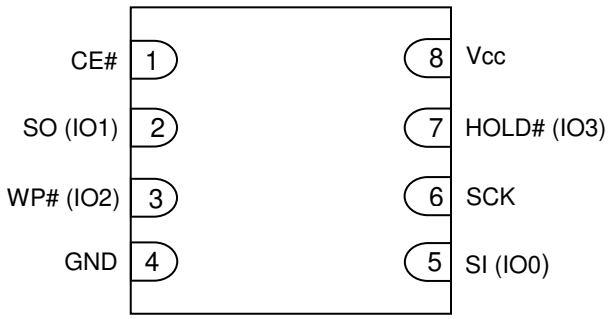
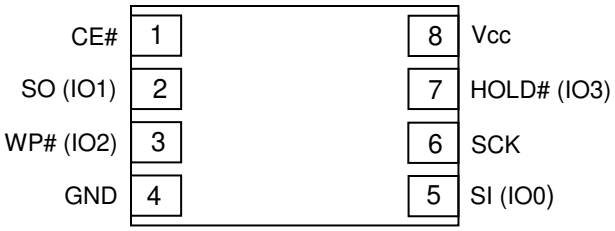
1. PIN CONFIGURATION



8-pin SOIC 150mil (Package: JN)
8-pin SOIC 208mil (Package: JB)
8-pin VVSOP 150mil (Package: JV)



8-contact WSON 6x5mm (Package: JK)

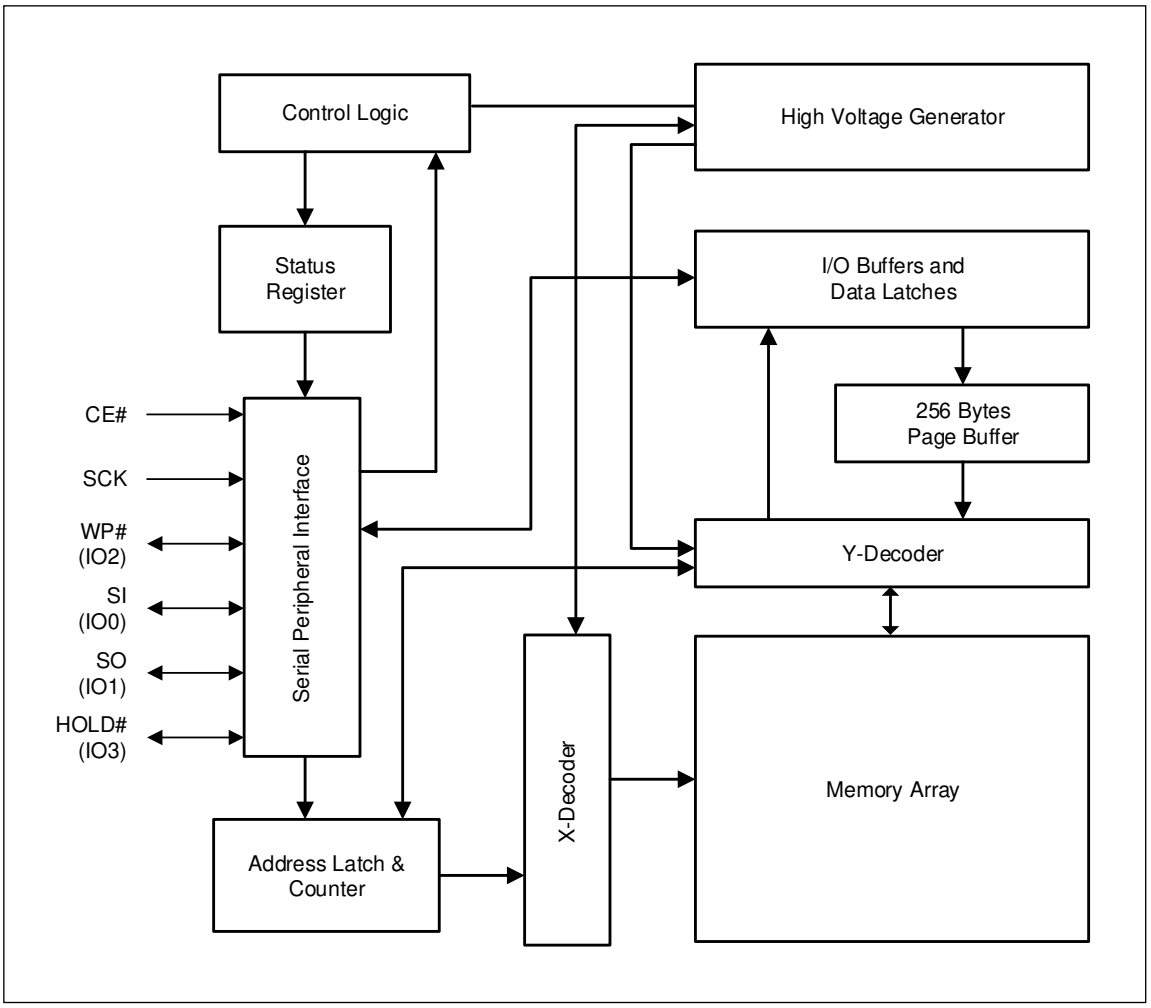


8-contact USON 2x3mm (Package: JU)

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Enable:** The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
SI (IO0), SO (IO1)	INPUT/OUTPUT	**Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):** This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK). In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.
WP# (IO2)	INPUT/OUTPUT	**Write Protect/Serial Data IO (IO2):** The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to “1” and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to “0”, the Status Register is not write-protected regardless of WP# state. When the QE bit is set to “1”, the WP# pin (Write Protect) function is not available since this pin is used for IO2.
HOLD# (IO3)	INPUT/OUTPUT	**Hold/Serial Data IO (IO3):** Pauses serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set to “1”, HOLD# pin is not available since it becomes IO3. The HOLD# pin allows the device to be paused while it is selected. The HOLD# pin is active low. When HOLD# is in a low state, and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state. When the QE bit of Status Register is set for Quad I/O, the HOLD# pin function is not available and becomes IO3 for Multi-I/O SPI mode.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left uncommitted.

3. BLOCK DIAGRAM



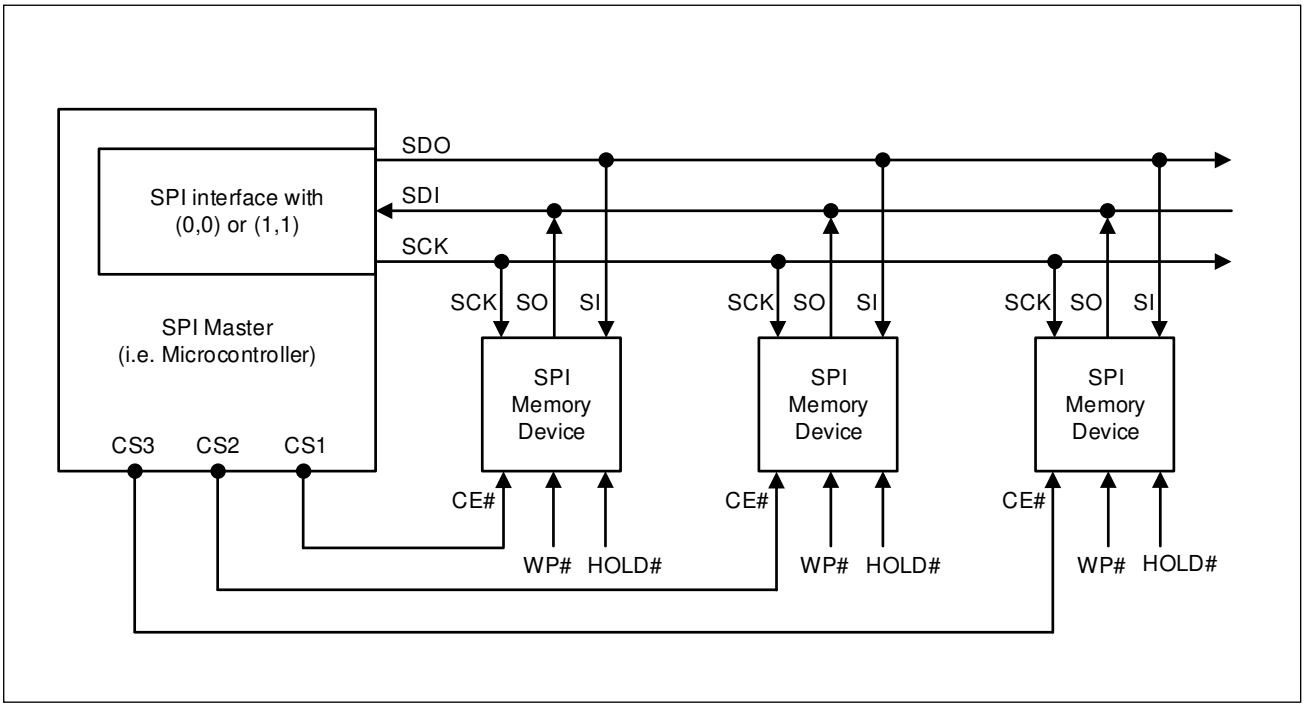
4. SPI MODES DESCRIPTION

Multiple IS25WQ040/020 devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1 the devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

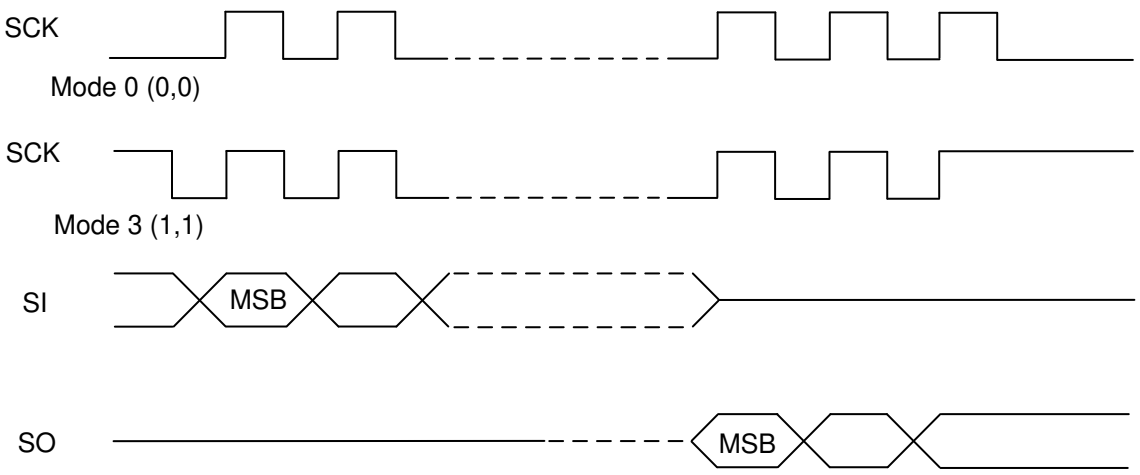
The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 for SPI mode. In SPI mode, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:
1. **The Write Protect (WP#) and Hold (HOLD#) signals should be driven high or low as necessary.**
2. **SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during Multi-IO mode.**

Figure 4.2 SPI Mode Support



5. SYSTEM CONFIGURATION

The IS25WQ040/020 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) microcontrollers or any SPI interface-equipped system controllers.

The memory array of IS25WQ040/020 is divided into uniform 4 Kbyte sectors or uniform 32/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses of IS25WQ040/020

Memory Density		Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
2 Mbit	4 Mbit	Block 0	Block 0	Sector 0	4	000000h - 000FFFh
				:	:	:
			Block 1	:	:	:
				Sector 15	4	00F000h - 00FFFFh
		Block 1	Block 2	Sector 16	4	010000h - 010FFFh
				:	:	:
			Block 3	:	:	:
				Sector 31	4	01F000h - 01FFFFh
		Block 2	Block 4	Sector 32	4	020000h - 020FFFh
				:	:	:
			Block 5	:	:	:
				Sector 47	4	02F000h - 02FFFFh
		Block 3	Block 6	Sector 48	4	030000h - 030FFFh
				:	:	:
			Block 7	:	:	:
				Sector 63	4	03F000h - 03FFFFh
		Block 4	Block 8	Sector 64	4	040000h - 040FFFh
				:	:	:
			Block 9	:	:	:
				Sector 79	4	04F000h - 04FFFFh
		Block 5	Block 10	Sector 80	4	050000h - 050FFFh
				:	:	:
			Block 11	:	:	:
				Sector 95	4	05F000h - 05FFFFh
		Block 6	Block 12	Sector 96	4	060000h - 060FFFh
				:	:	:
			Block 13	:	:	:
				Sector 111	4	06F000h - 06FFFFh
		Block 7	Block 14	Sector 112	4	070000h - 070FFFh
				:	:	:
			Block 15	:	:	:
				Sector 127	4	07F000h - 07FFFFh

6. REGISTERS

The IS25WQ040/020 has two sets of Registers: Status, Function.

6.1. STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Tables 6.1 & 6.2.

Table 6.1 Status Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SRWD	QE	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	Volatile
Bit 2	BP0	Block Protection Bit: (See Table 6.4 for details) "0" indicates the specific blocks are not write-protected (default) "1" indicates the specific blocks are write-protected	R/W	Non-Volatile
Bit 3	BP1			
Bit 4	BP2			
Bit 5	BP3			
Bit 6	QE	Quad Enable bit: “0” indicates the Quad output function disable (default) “1” indicates the Quad output function enable	R/W	Non-Volatile
Bit 7	SRWD	Status Register Write Disable: (See Table 7.1 for details) "0" indicates the Status Register is not write-protected (default) "1" indicates the Status Register is write-protected	R/W	Non-Volatile

The BP0, BP1, BP2, BP3 and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP3, BP2, BP1, BP0, and SRWD bits were set to “0” at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

WIP bit: The Write In Progress (WIP) bit is read-only, and can be used to detect the progress or completion of a program or erase operation. When the WIP bit is “0”, the device is ready for Write Status Register, program or erase operation. When the WIP bit is “1”, the device is busy.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When the WEL is “0”, the write enable latch is disabled and all write operations described in Table 6.3 are inhibited. When the WEL bit is “1”, write operations are allowed. The WEL bit is set by a Write Enable (WREN) instruction. Each write register, program and erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by a Write Disable (WRDI) instruction. It will automatically be reset after the completion of any write operation.

Table 6.3 Instructions requiring WREN instruction ahead

Instructions must be preceded by the WREN instruction		
Name	**Hex Code**	**Operation**
PP	02h	Input Page Program
PPQ	32h	Quad Input Page Program
SER	D7h/20h	Sector Erase
BER32 (32Kb)	52h	Block Erase 32K
BER64 (64Kb)	D8h	Block Erase 64K
CER	C7h/60h	Chip Erase
WRSR	01h	Write Status Register
IRP	62h	Program Information Row

BP3, BP2, BP1, BP0 bits: The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) instruction will be ignored unless all the Block Protection Bits are "0"s.

SRWD bit: The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write-protected. When the SRWD is set to "1" and the WP# is pulled low (V_{IL}), the bits of Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to "1" and WP# is pulled high (V_{IH}), the Status Register can be changed by a WRSR instruction.

QE bit: The Quad Enable (QE) is a non-volatile bit in the Status Register that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD# pin is tied directly to the power supply.

Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits.

Status Register Bits				Protected Memory Area	
BP3	**BP2**	**BP1**	**BP0**	**4 Mbit**	**2 Mbit**
0	0	0	0	None	None
0	0	0	1	1 block : 7	1 block : 3
0	0	1	0	2 blocks : 6 - 7	2 blocks : 2 - 3
0	0	1	1	4 blocks : 4 - 7	All Blocks
0	1	0	0	All Blocks	
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0	4 blocks 0 - 3	
1	1	0	1	2 blocks : 0 - 1	2 blocks : 0 - 1
1	1	1	0	1 block : 0	1 block : 0
1	1	1	1	None	None

6.2. FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and Table 6.6

Table 6.5 Function Register Format

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved	Reserved	Reserved	Reserved	Reserved	PSUS	ESUS	Reserved
Default	0	0	0	0	0	0	0	0

Table 6.6 Function Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
Bit 0	Reserved	Reserved	R	Reserved
Bit 1	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
Bit 2	PSUS	Program suspend bit: “0” indicates program is not suspend “1” indicates program is suspend	R	Volatile
Bit 3	Reserved	Reserved	R	Reserved
Bit 4	Reserved	Reserved	R	Reserved
Bit 5	Reserved	Reserved	R	Reserved
Bit 6	Reserved	Reserved	R	Reserved
Bit 7	Reserved	Reserved	R	Reserved

ESUS bit: The Erase Suspend Status indicates when an Erase operation has been suspended. The ESUS bit is ‘1’ after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to ‘0’.

PSUS bit: The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to ‘1’ after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to ‘0’.

7. PROTECTION MODE

The IS25WQ040/020 supports hardware and software write-protection mechanisms.

7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, SRWD, and QE in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage (V_{WI}) is specified in the section 9.8 POWER-UP AND POWER-DOWN. All write sequence will be ignored when Vcc drops to V_{WI}.

Table 7.1 Hardware Write Protection on Status Register

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

Note: Before the execution of any program, erase or Write Status Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

7.2 SOFTWARE WRITE PROTECTION

The device also provides a software write protection feature. The Block Protection (BP3, BP2, BP1, and BP0) bits allow part or the whole memory area to be write-protected.

8. DEVICE OPERATION

The device utilizes an 8-bit instruction register. Refer to Table 8.1. Instruction Set for details on Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first_on Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CE#) is driven low (V_{IL}). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high (V_{IH}) after the last bit of the instruction sequence has been shifted in to end the operation.

Table 8.1 Instruction Set

Instruction Name	Hex Code	Operation	Mode	Maximum Frequency
RD	03h	Read Data Bytes from Memory at Normal Read Mode	SPI	33MHz
FR	0Bh	Read Data Bytes from Memory at Fast Read Mode	SPI	104MHz
FRDIO	BBh	Fast Read Dual I/O	SPI	104MHz
FRDO	3Bh	Fast Read Dual Output	SPI	104MHz
FRQIO	EBh	Fast Read Quad I/O	SPI	104MHz
FRQO	6Bh	Fast Read Quad Output	SPI	104MHz
PP	02h	Page Program Data Bytes Into Memory	SPI	104MHz
PPQ	32h	Page Program Data Bytes Into Memory with Quad interface	SPI	104MHz
SER	D7h/20h	Sector Erase 4K	SPI	104MHz
BER32 (32Kbyte)	52h	Block Erase 32K	SPI	104MHz
BER64 (64Kbyte)	D8h	Block Erase 64K	SPI	104MHz
CER	C7h/60h	Chip Erase	SPI	104MHz
WREN	06h	Write Enable	SPI	104MHz
WRDI	04h	Write Disable	SPI	104MHz
RDSR	05h	Read Status Register	SPI	104MHz
WRSR	01h	Write Status Register	SPI	104MHz
RDFR	07h	Read Function Register	SPI	104MHz
PERSUS	75h/B0h	Suspend during the program/erase	SPI	104MHz
PERRSM	7Ah/30h	Resume program/erase	SPI	104MHz
DP	B9h	Deep power down mode	SPI	104MHz
RDID, RDPD	ABh	Read Manufacturer and Product ID/release Deep power down	SPI	104MHz
RDUID	A1h	Read Unique ID Number	SPI	104MHz
RDJDID	9Fh	Read Manufacturer and Product ID by JEDEC ID Command	SPI	104MHz
RDMDID	90h	Read Manufacturer and Device ID	SPI	80MHz
IRP	B1h	Program Information Row	SPI	104MHz
IRRD	4Bh	Read Information Row	SPI	33MHz
SECUNLOCK	26h	Sector Unlock	SPI	104MHz
SECLOCK	24h	Sector Lock	SPI	104MHz

8.1 READ DATA OPERATION (RD, 03h)

The Read Data (RD) instruction is used to read memory contents of the device at a maximum frequency of 33MHz.

The RD instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{VMSB} (Valid Most Significant Bit) - A_0 are decoded. The remaining bits (A23 – A_{MSB}) are ignored. The first byte address can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

The first byte data (D7 - D0) address is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one READ instruction. The address is automatically incremented after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

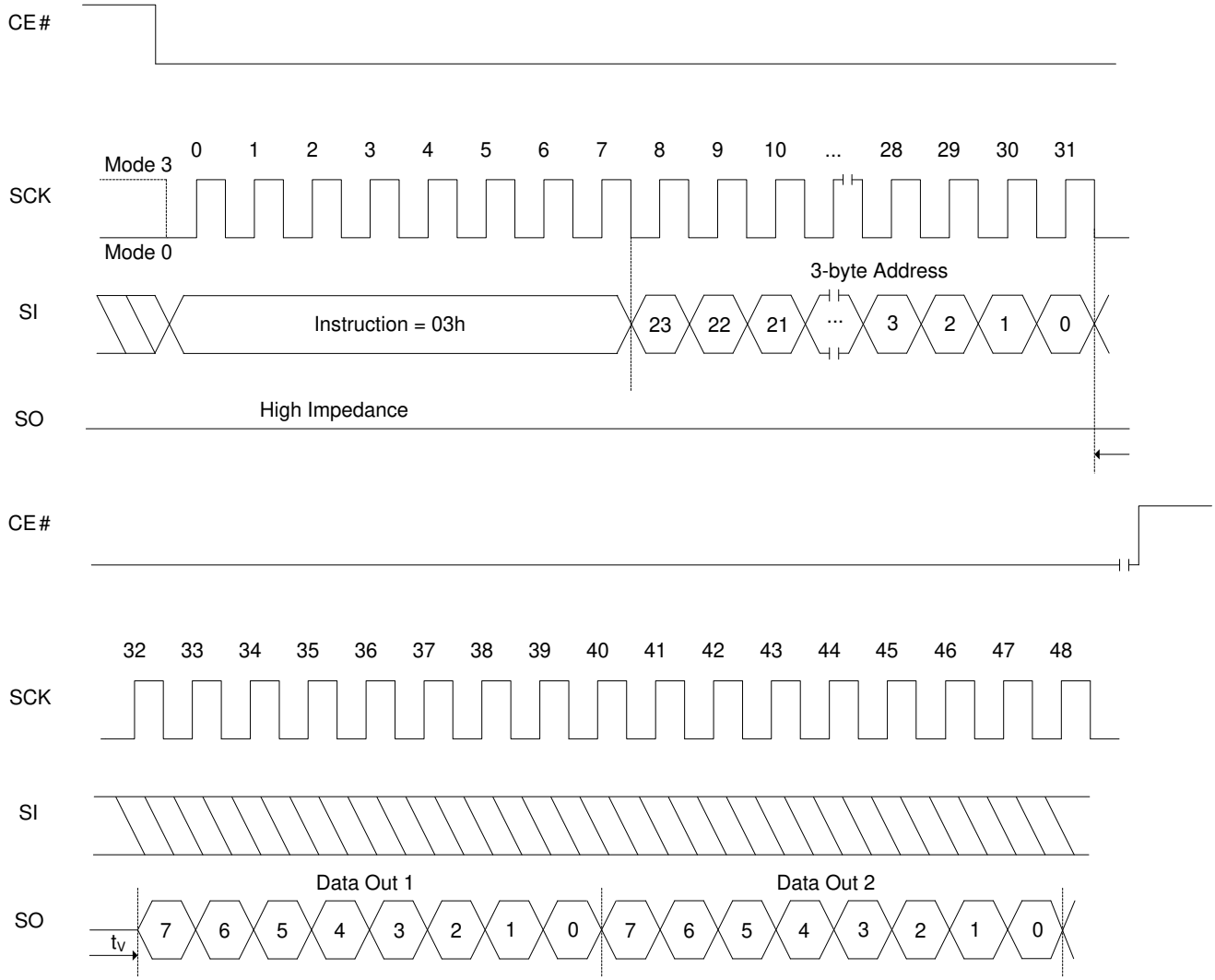
If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Table 8.2 Address Key

Valid Address	IS25WQ040	IS25WQ020
A_{VMSB}–A_0	A23-A0 (A23-A19=X)	A23-A0 (A23-A18=X)

Note: X=Don't Care

Figure 8.1 Read Data Sequence



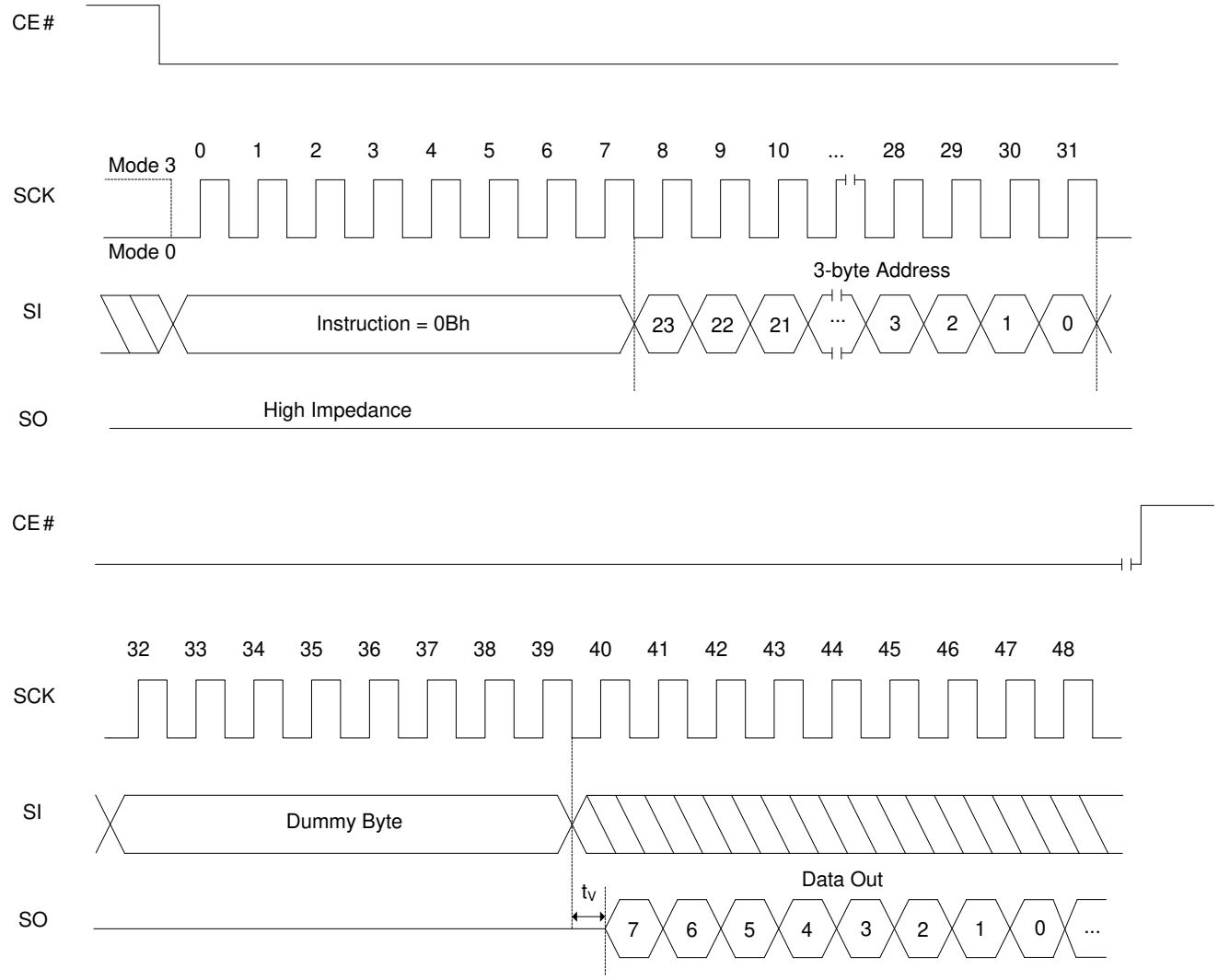
8.2 FAST READ DATA OPERATION (FR, 0Bh)

The FAST_READ instruction is used to read memory data at up to a 104MHZ clock.

The FAST_READ instruction code is followed by three address bytes (A23 - A0) and a dummy byte (8 clocks), transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte from the address is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.
The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST_READ instruction. The FAST_READ instruction is terminated by driving CE# high (VIH).

If a Fast Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.2 Fast Read Data Sequence



8.3 HOLD OPERATION

HOLD# is used in conjunction with CE# to select the device. When the device is selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to SI will be ignored while SO is in the high impedance state.

Timing graph can be referenced in AC Parameters Figure 9.3

8.4 FAST READ DUAL I/O OPERATION (FRDIO, BBh)

The FRDIO instruction allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

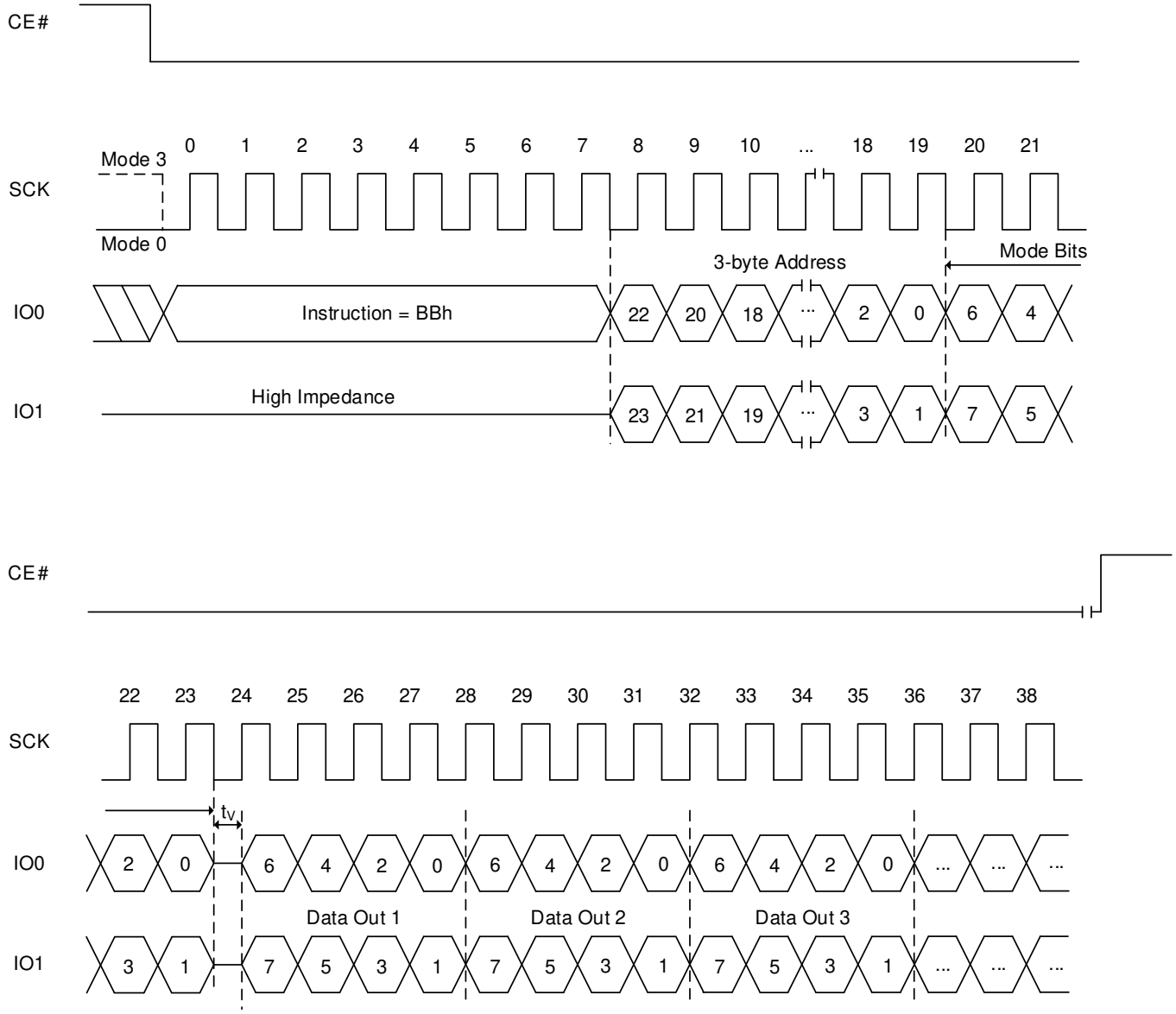
The FRDIO instruction code is followed by three address bytes (A23 – A0) and a mode byte, transmitted via the IO1 and IO0 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and continue to shift in alternating on the two lines. If AXh (X: don't care) is input for the mode byte, the device will enter AX read mode. In the AX read mode, the next instruction expected from the device will be another FRDIO instruction and will not need the BBh instruction code so that it saves cycles as described in Figure 8.4. If the following mode byte is not set to AXh, the device will exit AX read mode. To avoid any I/O contention problem, X should be Hi-Z.

Once address and mode byte are input the device will read out data at the specified address. The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO1, while simultaneously the second bit is output on IO0. Figure 8.3 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high (V_{IH}).

If the FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not affect the current cycle.

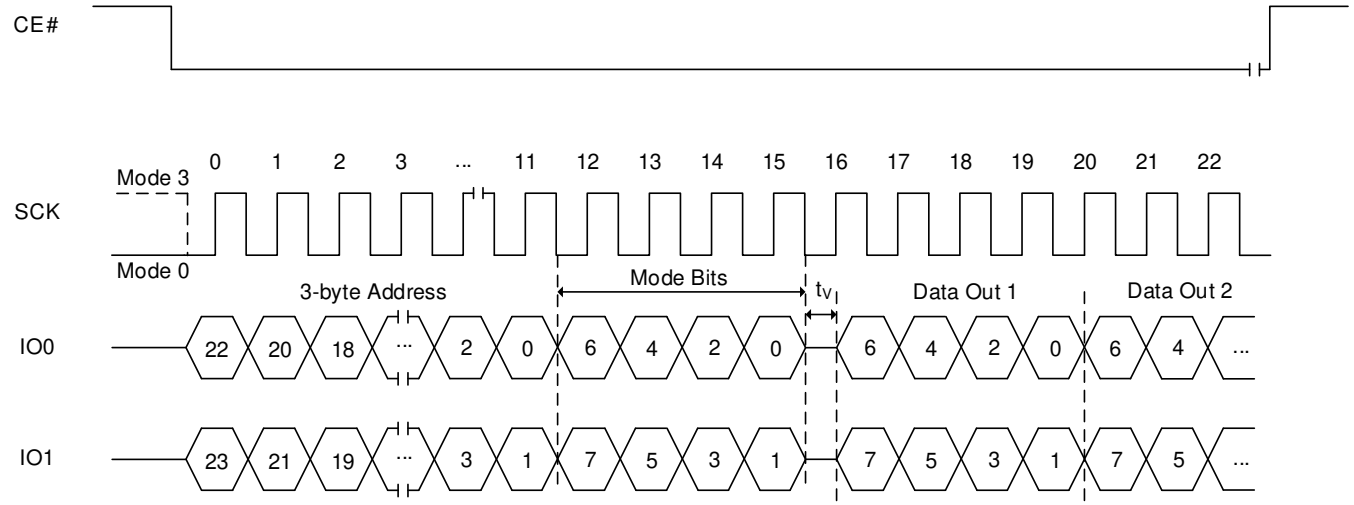
Figure 8.3 Fast Read Dual I/O Sequence (with command decode cycles)



Notes:

1. **If the mode bits=AXh (X: don't care), it can execute the AX read mode (without command). When the mode bits are different from AXh (X: don't care), the device exits the AX read operation.**
2. **To avoid I/O contention, X should be Hi-Z.**

Figure 8.4 Fast Read Dual I/O Sequence (without command decode cycles)



Notes:

1. **If the mode bits=AXh (X: don't care), it can execute the AX read mode (without command). When the mode bits are different from AXh (X: don't care), the device exits the AX read operation.**
2. **To avoid I/O contention, X should be Hi-Z.**

8.5 FAST READ DUAL OUTPUT OPERATION (FRDO, 3Bh)

The FRDO instruction is used to read memory data on two output pins each at up to a 104MHZ clock.

The FRDO instruction code is followed by three address bytes (A23 – A0) and a dummy byte (8 clocks), transmitted via the IO0 line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The first bit (MSB) is output on IO1. Simultaneously the second bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. FRDO instruction is terminated by driving CE# high (VIH).

If a FRDO instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle.

Figure 8.5 Fast Read Dual-Output Sequence