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IS31AP2121

2×25W STEREO / 1× 50W MONO DIGITAL AUDIO AMPLIFIER WITH 20 BANDS EQ FUNCTIONS, DRC AND 2.1CH MODE

October 2015

GENERAL DESCRIPTION

The IS31AP2121 is a digital audio amplifier capable of driving 25W (BTL) each to a pair of 8Ω speakers and 50W (PBTL) to a 4Ω speaker operating at 24V supply without external heat-sink or fan. The IS31AP2121 is also capable of driving 4Ω, 12W (SE)×2 + 8Ω, 25W (BTL)×1 at 24V supply for 2.1CH application.

The IS31AP2121 can provide advanced audio processing functions, such as volume control, 20 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I2C control interface. Robust protection circuits are provided to protect the IS31AP2121 from damage due to accidental erroneous operating condition. The full digital circuit design of IS31AP2121 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. IS31AP2121 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

APPLICATIONS

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

FEATURES

- 16/18/20/24-bits input with I2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  Loudspeaker: 104dB (PSNR), 110dB (DR) @24V
- Multiple sampling frequencies (F_S)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  - 64x~1024x F_S for 32kHz / 44.1kHz / 48kHz
  - 64x~512x F_S for 64kHz / 88.2kHz / 96kHz
  - 64x~256x F_S for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for speaker driver
- Supports 2.0CH/2.1CH/Mono configuration
- Loudspeaker output power for at 24V
  - 10W × 2CH into 8Ω @0.16% THD+N for stereo
  - 15W × 2CH into 8Ω @0.19% THD+N for stereo
  - 25W × 2CH into 8Ω @0.3% THD+N for stereo
- Sound processing including:
  - 20 bands parametric speaker EQ
  - Volume control (+24dB ~ -103dB, 0.125dB/step),
  - Dynamic range control (DRC)
  - Dual band dynamic range control
  - Power clipping
  - 3D surround sound
  - Channel mixing
  - Noise gate with hysteresis window
  - Bass/Treble tone control
  - Bass management crossover filter
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- Supports I2C control without MCLK
- I2C control interface with selectable device address
- Support BCLK system
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode

TYPICAL APPLICATION CIRCUIT

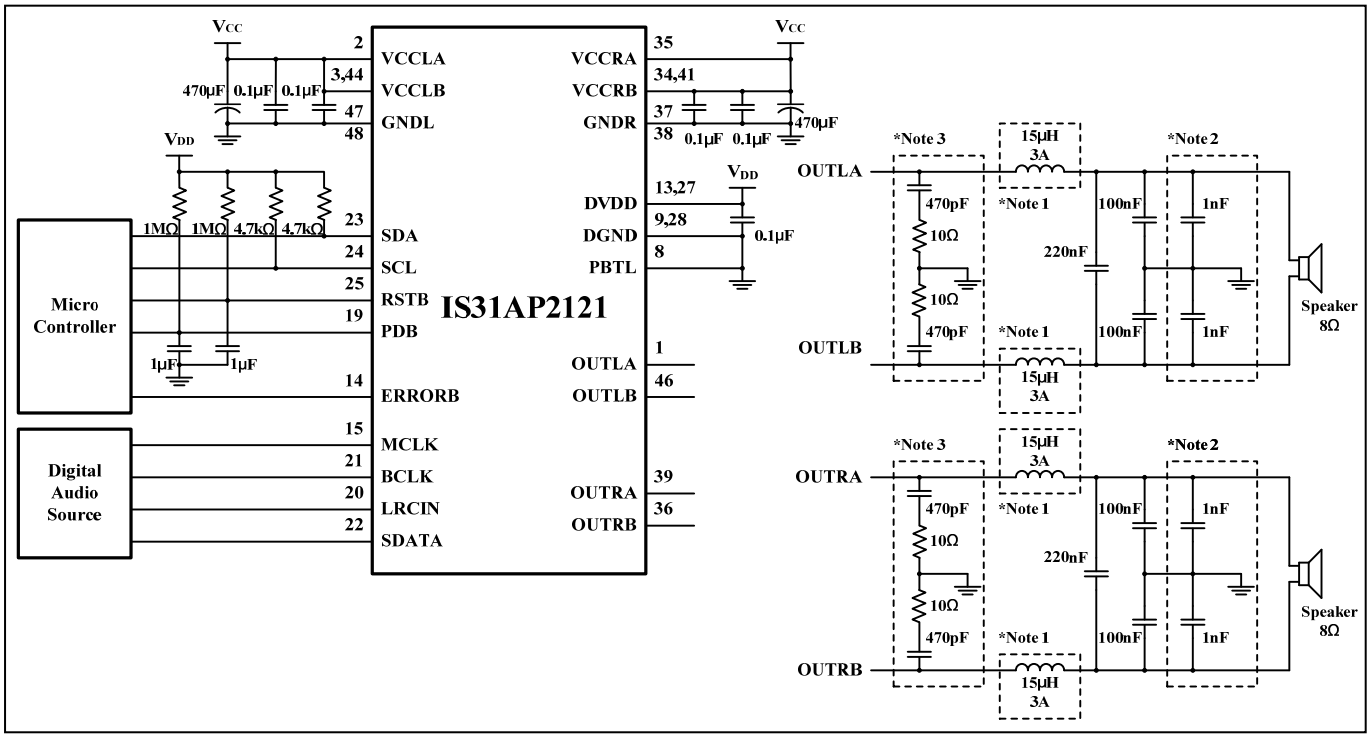


Figure 1 Typical Application Circuit (For Stereo)

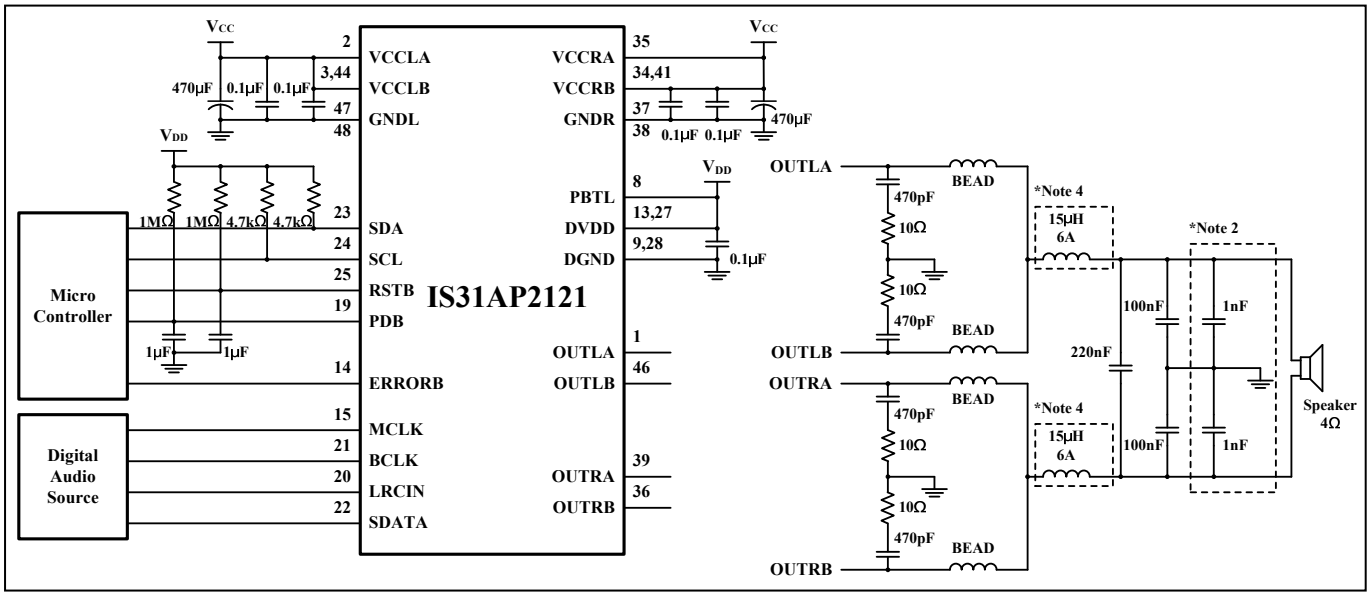


Figure 2 Typical Application Circuit (For Mono)

Pin / Logic	0	1
PDB	Power Down	Normal
RSTB	Reset	Normal
PBTL	Stereo	Mono

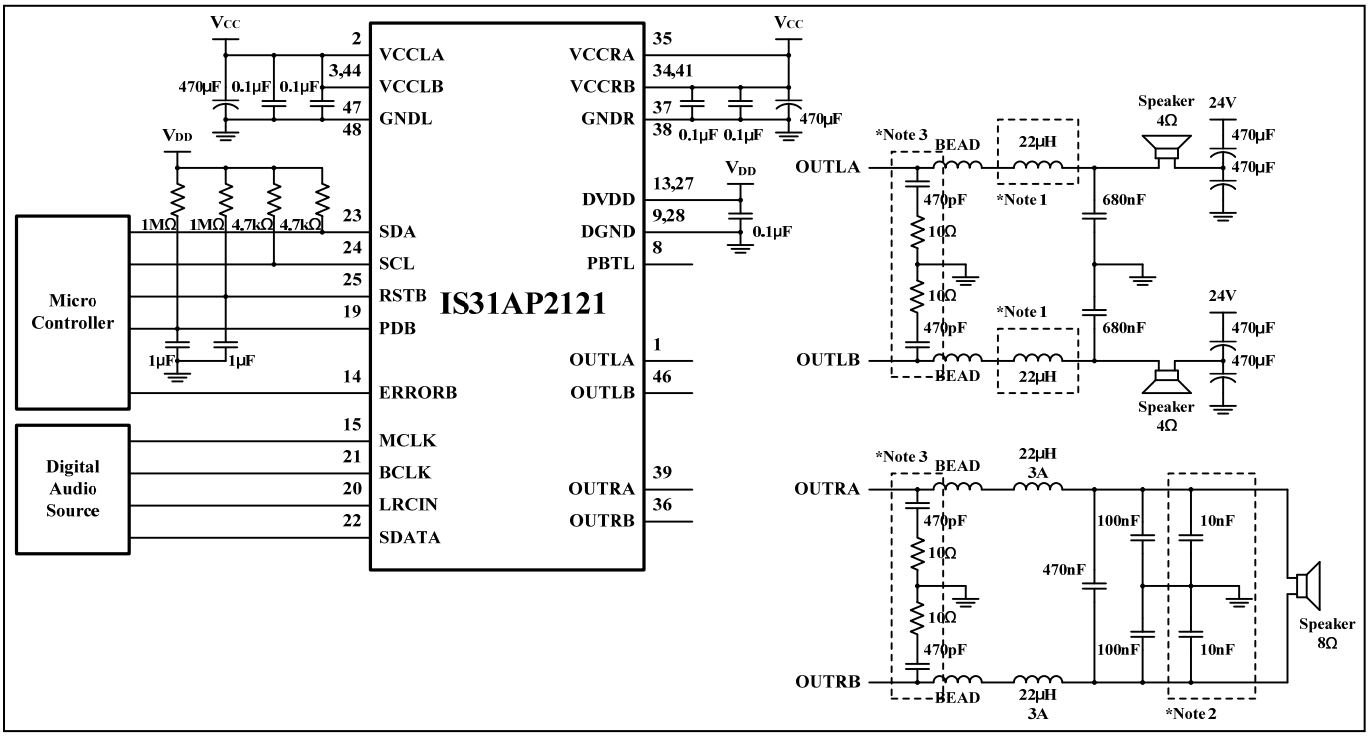


Figure 3 Typical Application Circuit (For 2.1CH) (Note 5)

Pin / Logic	0	1
PDB	Power Down	Normal
RSTB	Reset	Normal
PBTL	X	X

Note 1: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 7A.

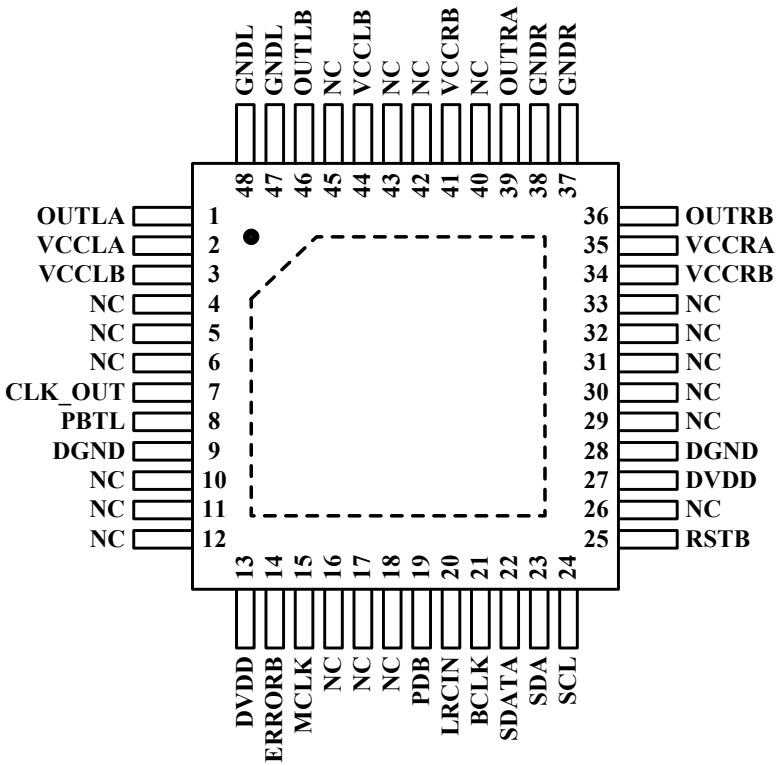
Note 2: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 3: The snubber circuit can be removed while the V_{CC} ≤20V.

Note 4: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 14A.

Note 5: 2.1CH configuration, it programs by I2C via register address 0x11, D4 bit SEM.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eLQFP-48	

PIN DESCRIPTION

No.	Pin	Description	Characteristics
1	OUTLA	Left channel output A.	
2	VCCLA	Left channel supply A.	
3,44	VCCLB	Left channel supply B.	
4~6,10~12	NC	Not connected.	
7	CLK_OUT	PLL ratio setting pin during power up, this pin is monitored on the rising edge of reset. PMF register will be default set at 1 or 4 times PLL ratio. Low: PMF [3:0]=[0000], 1 time of PLL ratio to avoid system MCLK over flow. High: PMF [3:0]=[0100], 4 times of PLL ratio. This pin could be clock output pin also during normal operating if EN_CLK_OUT register bit is enabled.	TTL output buffer, internal pull low with an 80kΩ resistor.
8	PBTL	Stereo/mono configuration pin (Low: Stereo; High: Mono).	
9,28	DGND	Digital ground.	
13,27	DVDD	Digital power.	
14	ERRORB	ERRORB pin is a dual function pin. One is I2C address setting during power up. The other one is error status report (low active). It sets by register of A_SEL_FAULT at address 0x13 D6 to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15kΩ pull down) sets the I2C device address to 0x30 and a value of High (15kΩ pull up) sets it to 0x31.
15	MCLK	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with an 80kΩ resistor.
16~18,26	NC	Not connected.	
19	PDB	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330kΩ resistor.
20	LRCIN	Left/Right clock input (F_S).	Schmitt trigger TTL input buffer, internal pull Low with an 80kΩ resistor.
21	BCLK	Bit clock input ($64F_S$).	Schmitt trigger TTL input buffer, internal pull Low with an 80kΩ resistor.
22	SDATA	I2S serial audio data input.	Schmitt trigger TTL input buffer
23	SDA	I2C serial data.	Schmitt trigger TTL input buffer
24	SCL	I2C serial clock input.	Schmitt trigger TTL input buffer
25	RSTB	Reset, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330kΩ resistor.
29~33,40	NC	Not connected.	

PIN DESCRIPTION (CONTINUE)

No.	Pin	Description	Characteristics
34,41	VCCRB	Right channel supply B.	
35	VCCRA	Right channel supply A.	
36	OUTRB	Right channel output B.	
37,38	GNDR	Right channel ground.	
39	OUTRA	Right channel output A.	
42,43,45	NC	Not connected.	
46	OUTLB	Left channel output B.	
47,48	GNDL	Left channel ground.	
	Thermal Pad	Connect to DGND.	

ORDERING INFORMATION

Industrial Range: 0°C to +70°C

Order Part No.	Package	QTY
IS31AP2121-LQLS1	e-LQFP-48, Lead-free	250/Tray

ABSOLUTE MAXIMUM RATINGS

Supply for driver stage (VCCR, VCCL), V_{CC}	−0.3V ~ +30V
Supply for digital circuit (DVDD), V_{DD}	−0.3V ~ +3.6V
Input voltage (SDA,SCL,RSTB,PDB,ERRORB,MCLK, BCLK,LRCIN,SDATA,PBTL), V_{IN}	−0.3V ~ +3.6V
Thermal resistance, θ_{JA}	27.4°C/W
Junction temperature range, T_J	0°C ~ 150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
ESD (HBM) ESD (CDM)	±2kV ±500V

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply for driver stage to VCCR/L		10		26	V
V_{DD}	Supply for digital circuit		3.15		3.45	V
T_J	Junction operating temperature		0		125	°C
T_A	Ambient operating temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{PDH}	VCC supply current during power down	V_{CC} = 24V		10	200	μA
I_{PDL}	DVDD supply current during power down	V_{DD} = 3.3V, PBTL=Low		13	20	μA
I_{CCH}	Quiescent current for VCC (50%/50% PWM duty)	V_{CC} = 24V		37		mA
I_{CCL}	Quiescent current for DVDD (Un-mute)	V_{DD} = 3.3V, PBTL=Low		70		mA
V_{UVH}	Under-voltage disabled (For DVDD)			2.8		V
V_{UVL}	Under-voltage enabled (For DVDD)			2.7		V
$R_{DS(ON)}$	Static drain-to-source on-state resistor, PMOS	V_{CC} =24V, I_D = 500mA		260		mΩ
	Static drain-to-source on-state resistor, NMOS			230		
I_{SC}	L/R channel over-current protection	V_{CC} =24V, I_D =500mA (Note 1)		7		A
	Mono channel over-current protection			14		
T_S	Junction temperature for driver shutdown			158		°C
	Temperature hysteresis for recovery from shutdown			33		°C

DC ELECTRICAL CHARACTERISTICS (CONTINUE)

T_A=25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics						
V_{IH}	High level input voltage	V_{DD} =3.3V	2.0			V
V_{IL}	Low level input voltage	V_{DD} =3.3V			0.8	V
V_{OH}	High level output voltage	V_{DD} =3.3V	2.4			V
V_{OL}	Low level output voltage	V_{DD} =3.3V			0.4	V
C_{IN}	Input capacitance			6.4		pF

Note 1: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=24V, V_{DD} = 3.3V, f_S = 48kHz, R_L=8Ω with passive LC lowpass filter (L= 15μH, R_{DC}= 63mΩ, C=220nF), input is 1kHz sinewave, volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_O	RMS output power (Note 2)	THD+N=0.16%, V_{CC}=24V, +8dB volume		10		W
		THD+N=0.25%, V_{CC}=24V, +8dB volume		20		
		THD+N=1%, V_{CC}=12V, +8dB volume		7.5		
		THD+N=10%, V_{CC}=12V, +8dB volume		9		
		PBTL Mode, V_{CC}=24V, R_L=4Ω, THD+N=0.16%, +8dB volume		40		
		PBTL Mode, V_{CC}=12V, R_L=4Ω, THD+N=1%, +8dB volume		15		
		PBTL Mode, V_{CC}=12V, R_L=4Ω, THD+N=10%, +8dB volume		18		
		2.1CH Mode, V_{CC}=24V, R_L=4Ω, THD+N=0.14%, +8dB volume		5		
		2.1CH Mode, V_{CC}=24V, R_L=4Ω, THD+N=0.16%, +8dB volume		10		
		2.1CH Mode, V_{CC}=12V, R_L=4Ω, THD+N=1%, +8dB volume		3.7		
		2.1CH Mode, V_{CC}=12V, R_L=4Ω, THD+N=10%, +8dB volume		4.5		
THD+N	Total harmonic distortion + noise	V_{CC}=24V, P_O = 7.5W		0.15		%
		V_{CC}=12V, Po = 2.5W		0.16		
V_{NO}	Output noise	20Hz ~ 20kHz (Note 3)		120		μV
SNR	Signal-to-noise ratio	+8dB volume, input level is -9dB (Note 3)		104		dB
DR	Dynamic range	+8dB volume, input level is -68dB (Note 3)		110		dB
PSRR	Power supply ripple rejection	V_{RIPPLE} = 1V_{RMS} at 1kHz		-71		dB
	Channel separation	1W @1kHz		-81		dB

I2C DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Serial-Clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	4.7		1.3		µs
$t_{HD, STA}$	Hold time (repeated) START condition	4.0		0.6		µs
$t_{SU, STA}$	Repeated START condition setup time	4.7		0.6		µs
$t_{SU, STO}$	STOP condition setup time	4.0		0.6		µs
$t_{HD, DAT}$	Data hold time	0	3.45	0	0.9	µs
$t_{SU, DAT}$	Data setup time	250		100		ns
t_{LOW}	SCL clock low period	4.7		1.3		µs
t_{HIGH}	SCL clock high period	4.0		0.6		µs
t_R	Rise time of both SDA and SCL signals, receiving		1000	$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving		300	$20+0.1C_b$	300	ns
C_b	Capacitive load for each bus line		400		400	pF
V_{NL}	Noise margin at the low level for each connected device (including hysteresis)	$0.1V_{DD}$		$0.1V_{DD}$		V
V_{NH}	Noise margin at the high level for each connected device (including hysteresis)	$0.2V_{DD}$		$0.2V_{DD}$		V

I2S DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{LR}	LRCIN period ($1/F_S$)		10.41		31.25	µs
t_{BL}	BCLK rising edge to LRCIN edge		50			ns
t_{LB}	LRCIN edge to BCLK rising edge		50			ns
t_{BCC}	BCLK period ($1/64F_S$)		162.76		488.3	ns
t_{BCH}	BCLK pulse width high		81.38		244	ns
t_{BCL}	CBLK pulse width low		81.38		244	ns
t_{DS}	SDATA set up time		50			ns
t_{DH}	SDATA hold time		50			ns

Note 2: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

Note 3: Measured with A-weighting filter.

Note 4: Guaranteed by design.

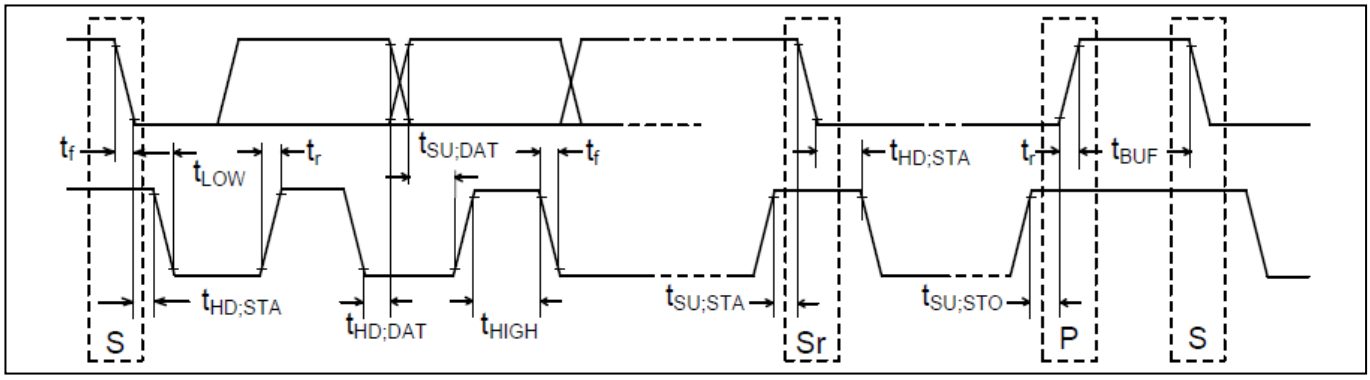


Figure 4 I2C Timing

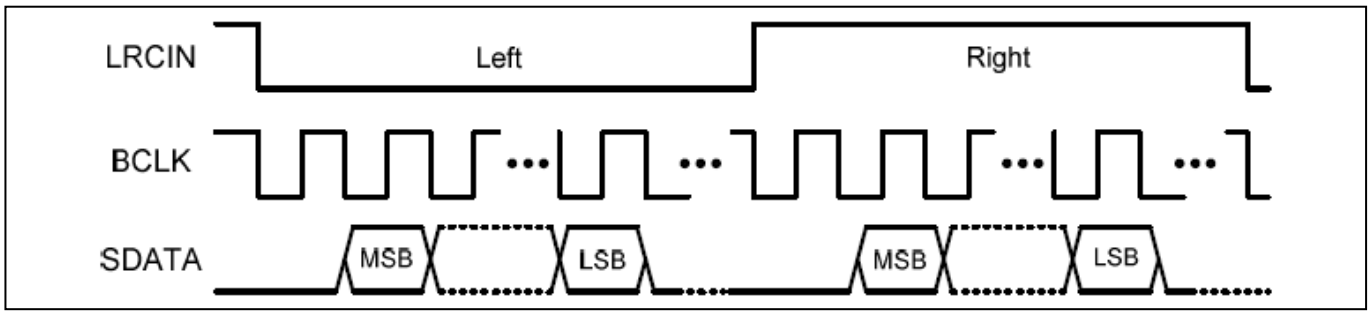


Figure 5 I2S

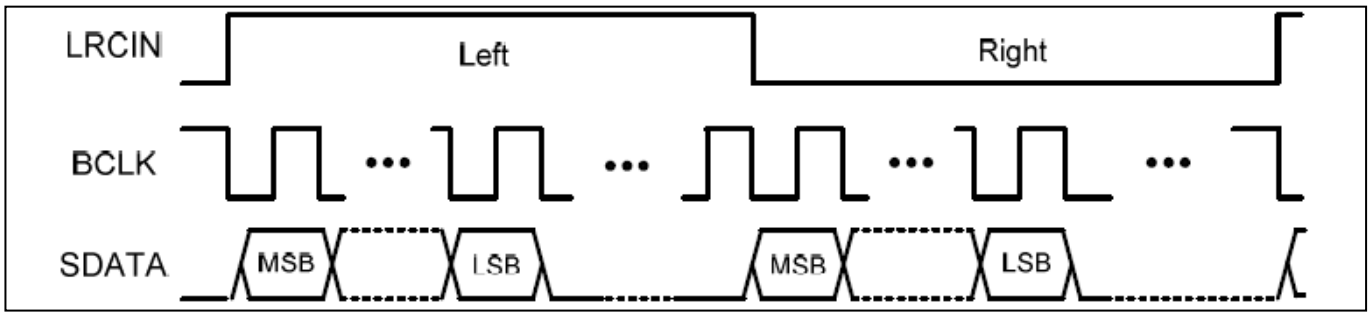


Figure 6 Left-Alignment

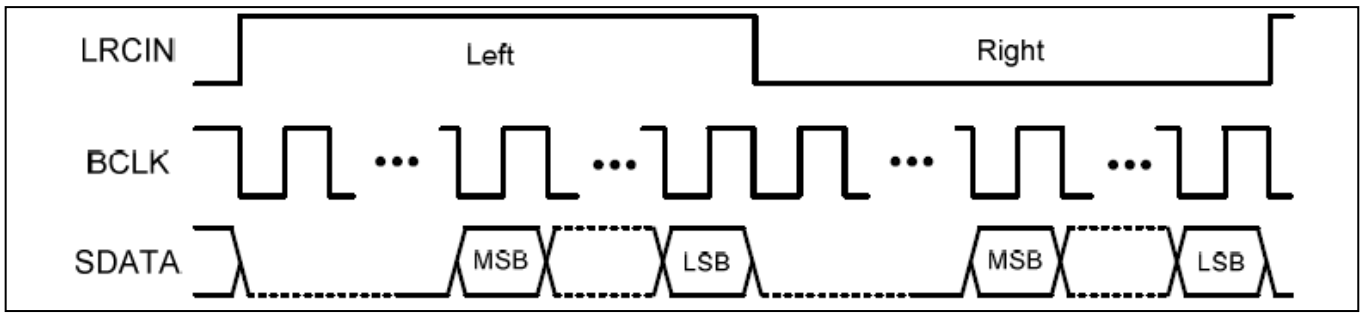


Figure 7 Right-Alignment

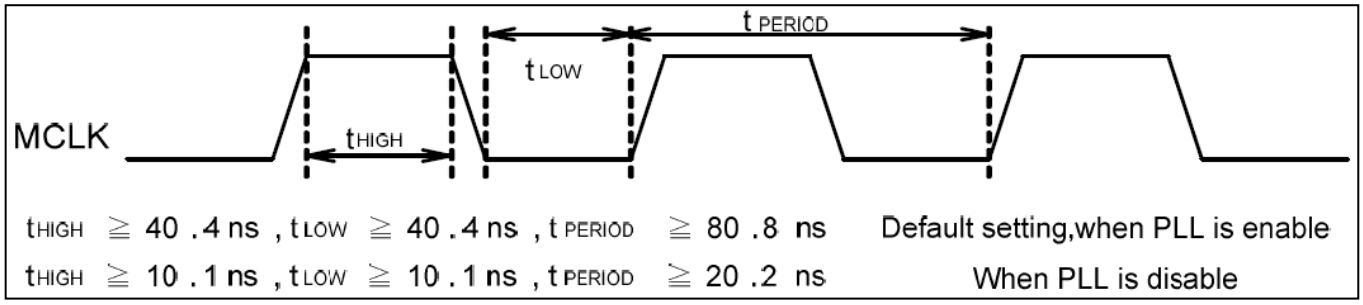


Figure 8 System Clock Timing

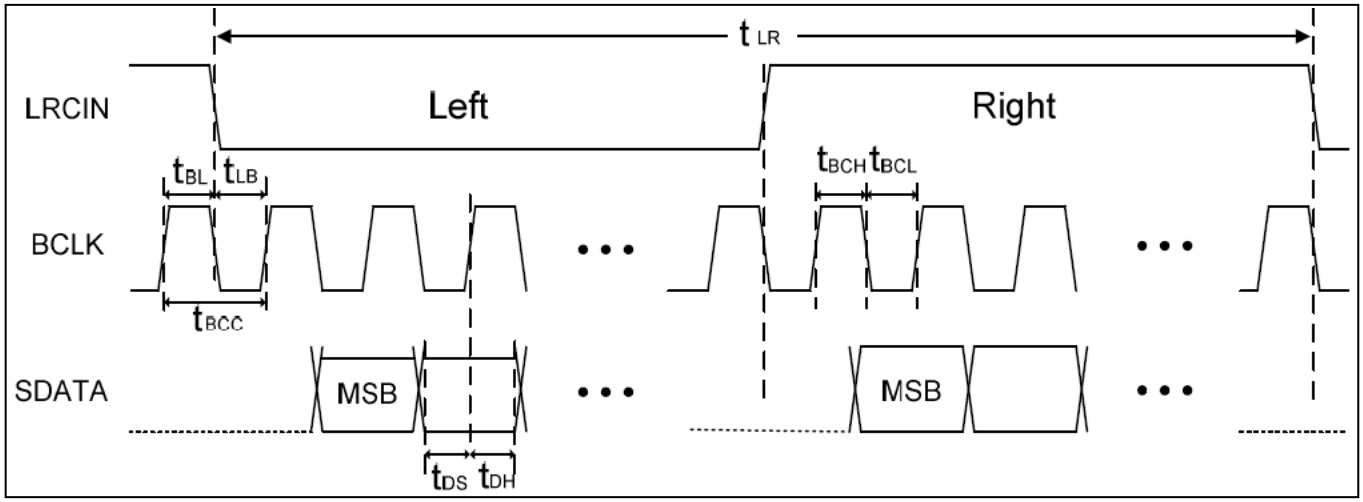


Figure 9 Timing Relationship (Using I2S format as an example)

TYPICAL PERFORMANCE CHARACTERISTICS

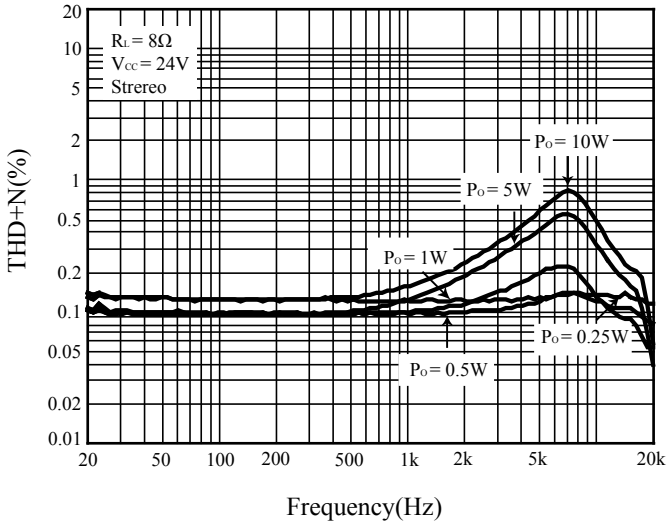


Figure 10 THD+N vs. Frequency

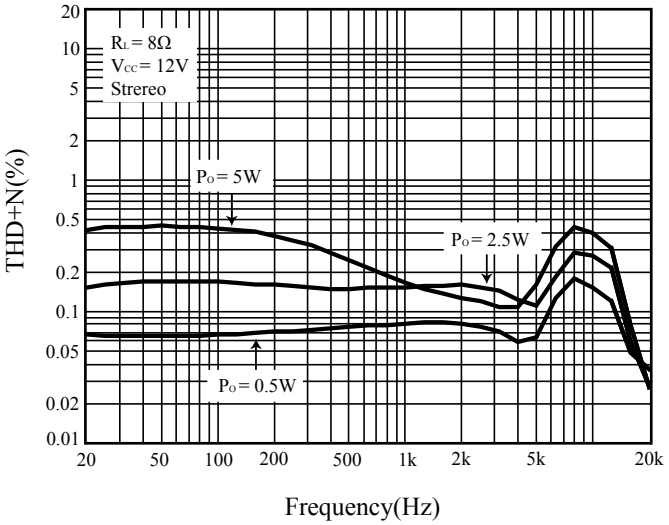


Figure 11 THD+N vs. Frequency

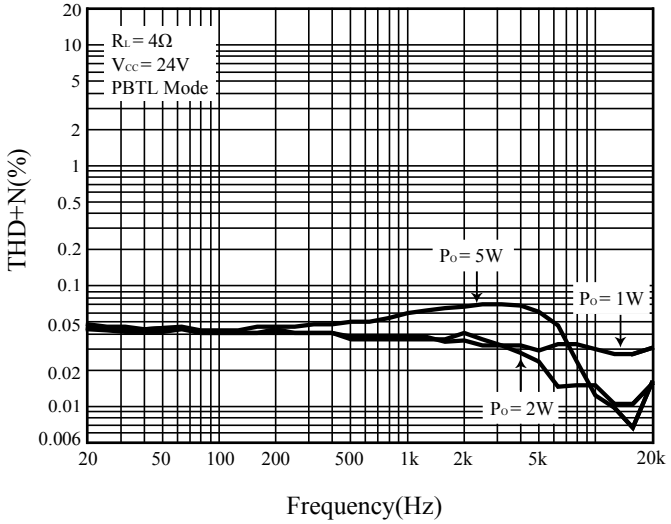


Figure 12 THD+N vs. Frequency

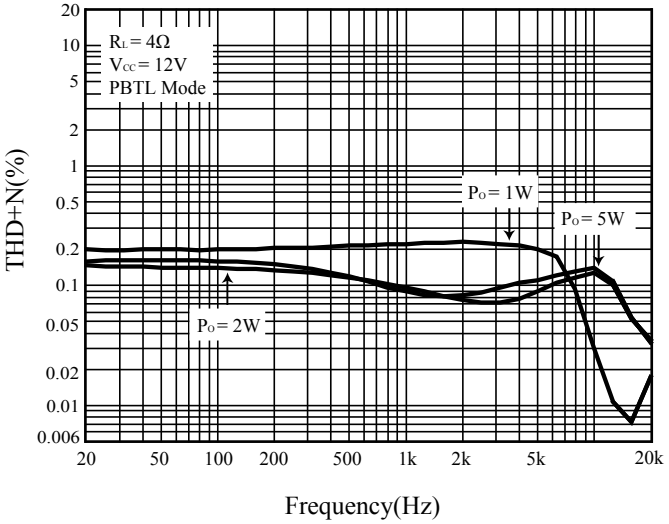


Figure 13 THD+N vs. Frequency

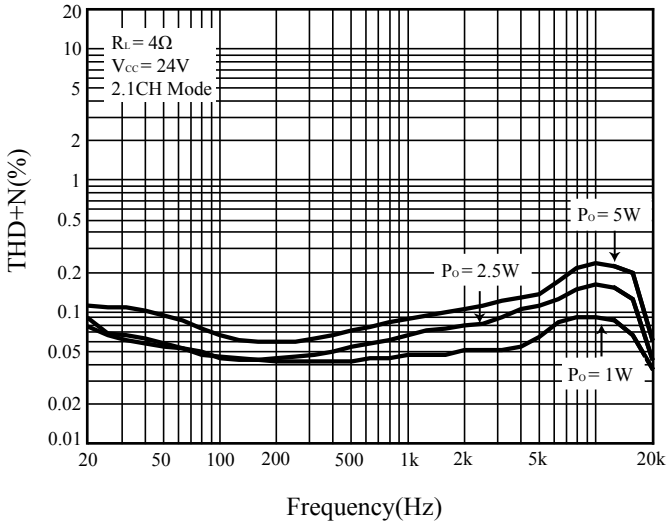


Figure 14 THD+N vs. Frequency

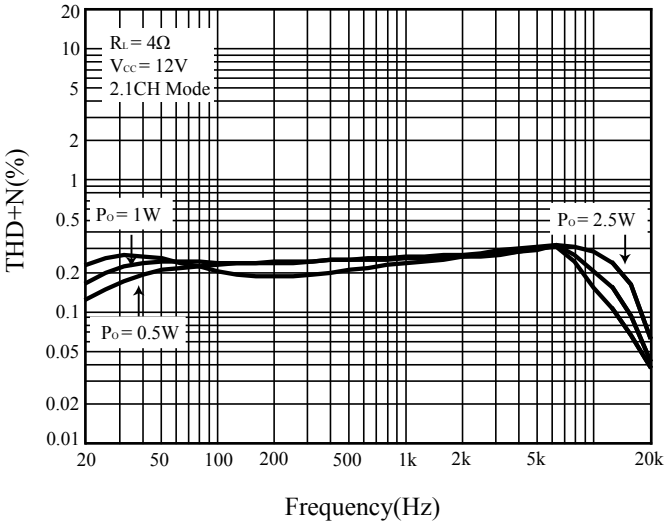


Figure 15 THD+N vs. Frequency

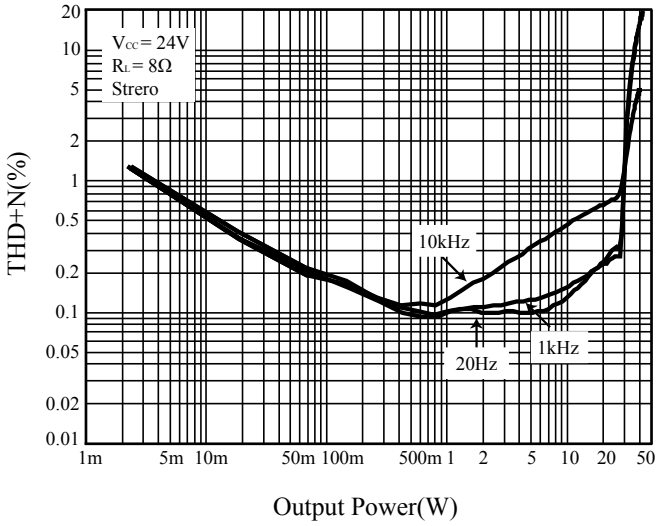


Figure 16 THD+N vs. Output Power

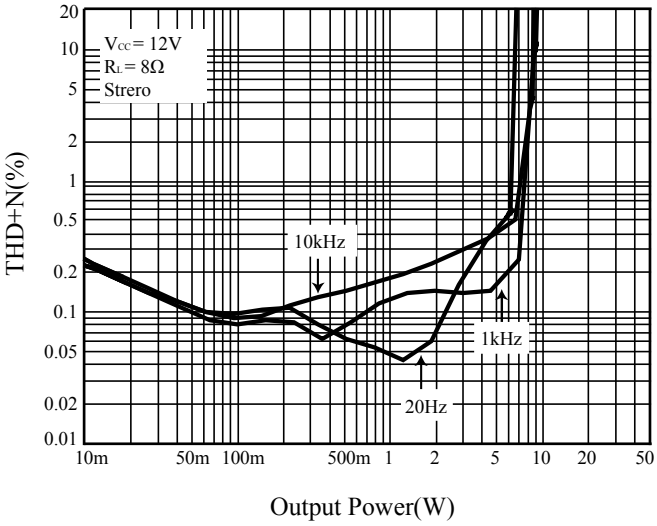


Figure 17 THD+N vs. Output Power

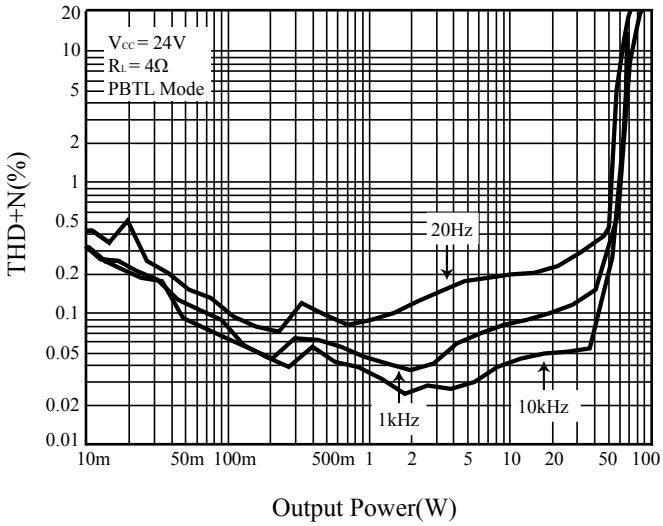


Figure 18 THD+N vs. Output Power

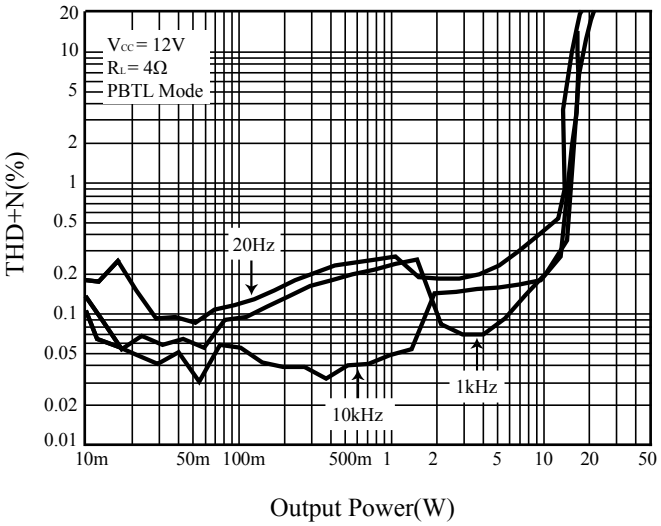


Figure 19 THD+N vs. Output Power

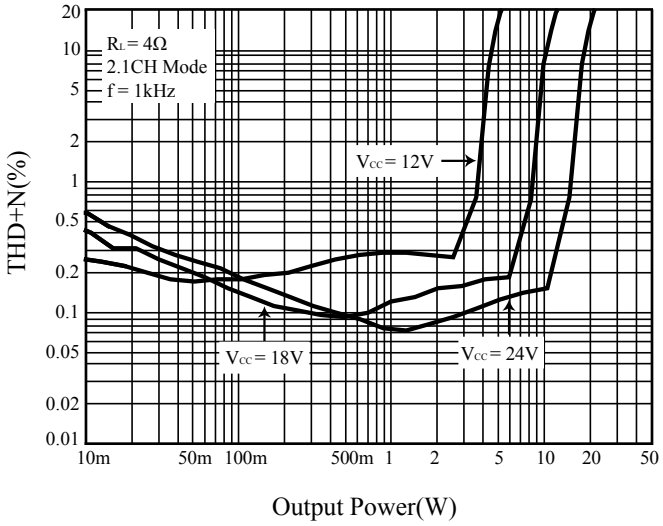


Figure 20 THD+N vs. Output Power

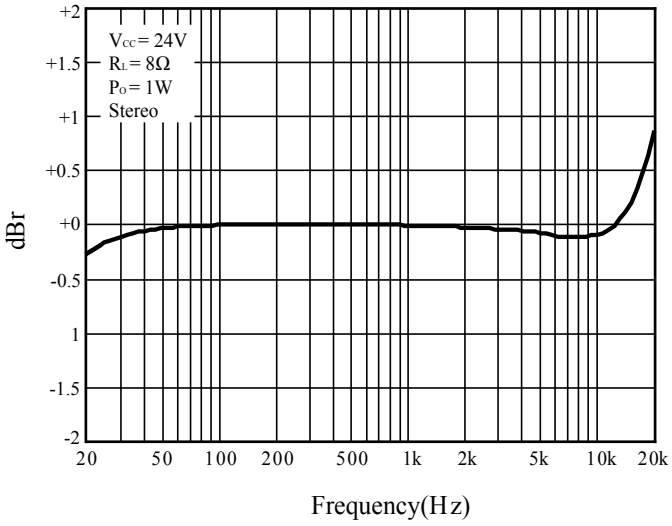


Figure 21 Frequency Response

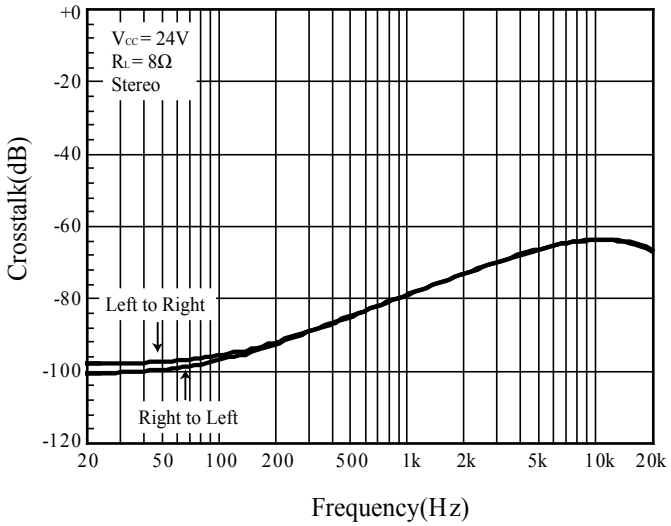


Figure 22 Cross-Talk

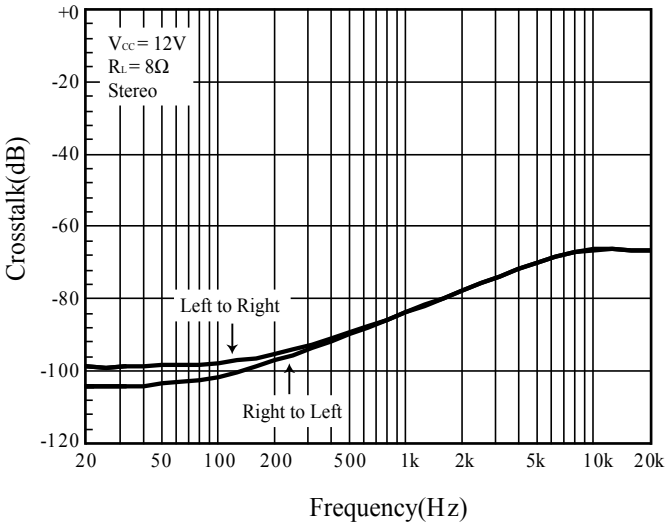


Figure 23 Cross-Talk

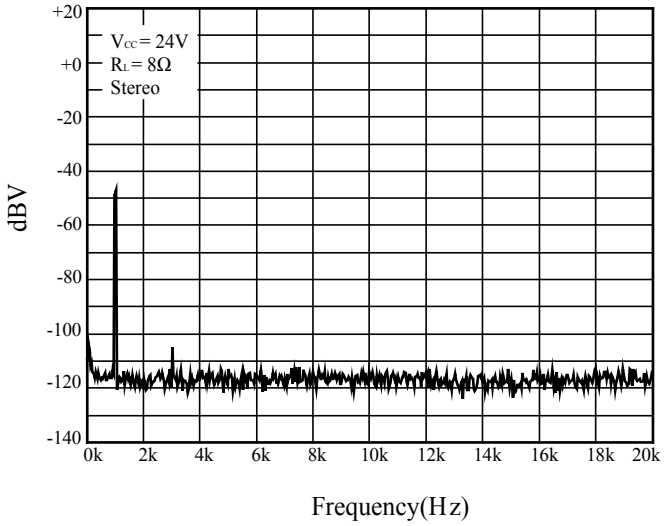


Figure 24 Spectrum at -60dB Signal Input Level

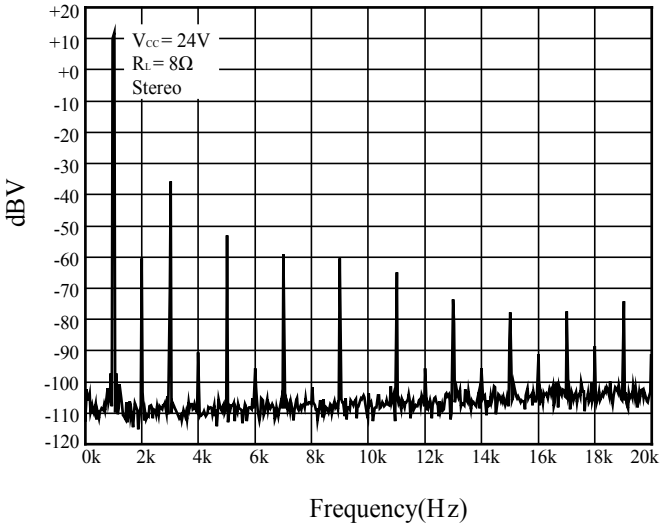


Figure 25 Spectrum at Peak SNR at -1dB Signal Input

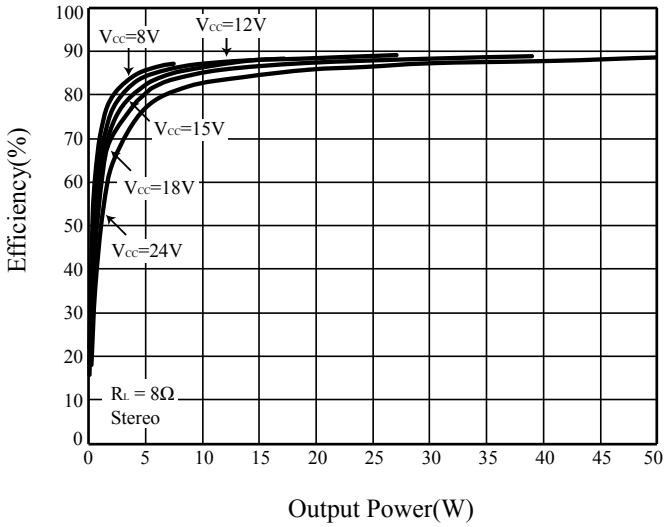


Figure 26 Efficiency vs. Output Power (Power Saving Mode)

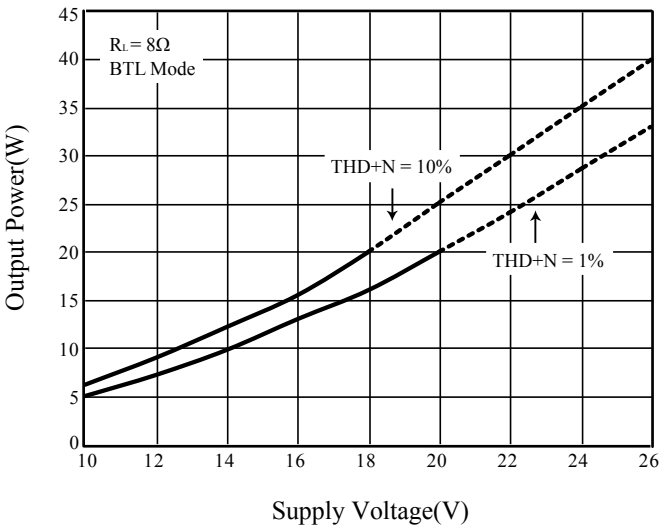


Figure 27 Output Power vs. Supply Voltage

Note: Dashed lines represent thermally limited region.

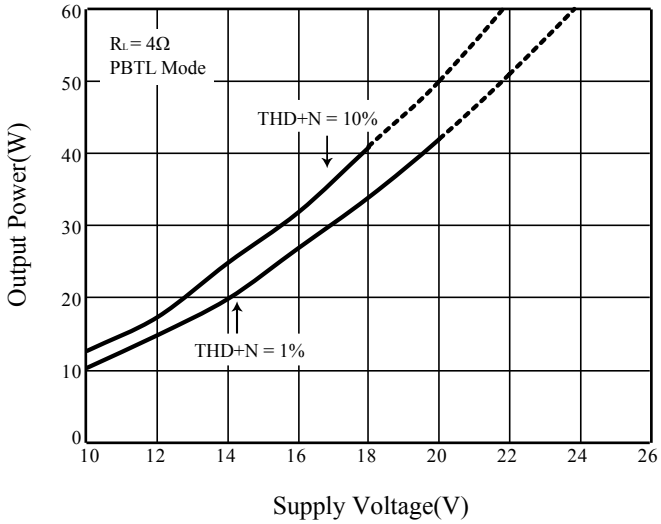


Figure 28 Output Power vs. Supply Voltage

Note: Dashed lines represent thermally limited region.

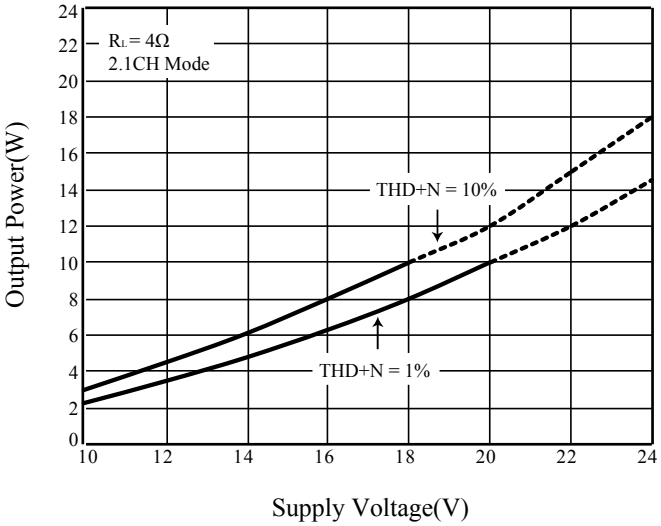
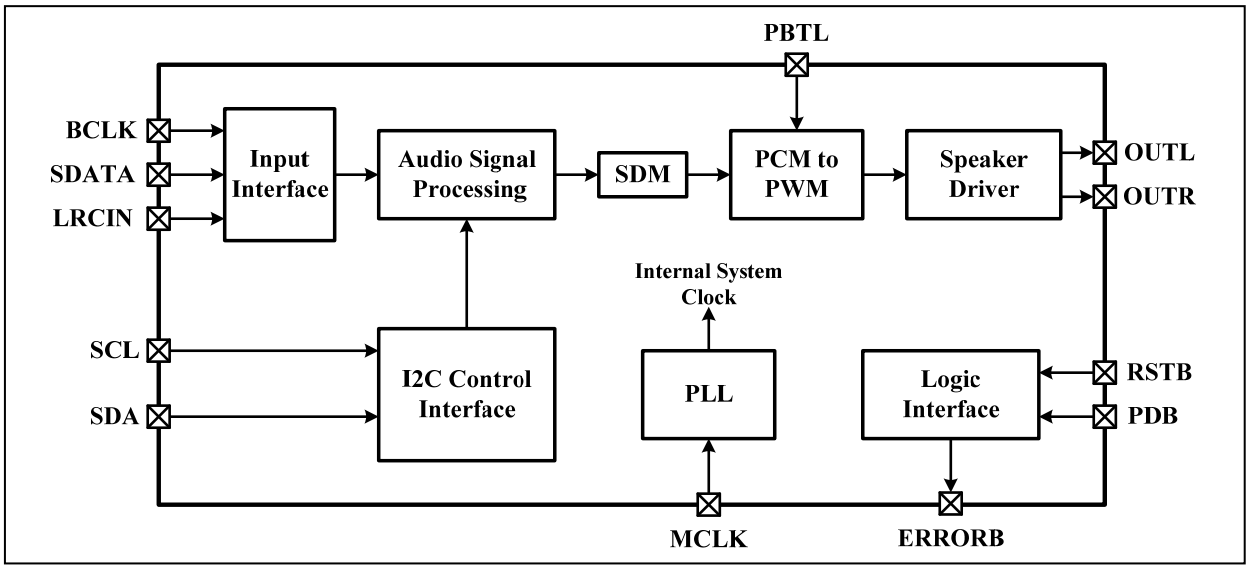


Figure 29 Output Power vs. Supply Voltage

Note: Dashed lines represent thermally limited region.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

IS31AP2121 has a built-in PLL internally, the default volume is muted. IS31AP2121 will activate while the de-mute command via I2C is programmed.

OPERATION MODES

Without I2C Control

The default settings, Bass, Treble, EQ, Volume, DRC, PLL, Subwoofer Bandwidth, …, and Sub-woofer gain are applied to register table content when using IS31AP2121 without I2C control. The more information about default settings, please refer to the highlighted column of register table section.

With I2C Control

When using I2C control, user can program suitable parameters into IS31AP2121 for their specific applications. Please refer to the register table section to get the more detail.

INTERNAL PLL

IS31AP2121 has a built-in PLL internally. The MCLK/F_S ratio will be fixed at 1024x, 512x, or 256x with a sample frequency of 48kHz, 96kHz, or 192kHz respectively. A carrier clock frequency is the frequency divided by 128 of master clock.

Table 1 MCLK/F_S Ratio

F_S	MCLK Frequency
48kHz	49.152MHz
44.1kHz	45.158MHz
32kHz	32.768MHz

RESET

When the RSTB pin is lowered, IS31AP2121 will clear the stored data and reset the register table to default values. IS31AP2121 will exit reset state at the 256th MCLK cycle after the RSTB pin is raised to high.

POWER DOWN CONTROL

IS31AP2121 has a built-in volume fade-in/fade-out design for power down and mute function. The relative power down timing diagrams for loudspeakers are shown below.

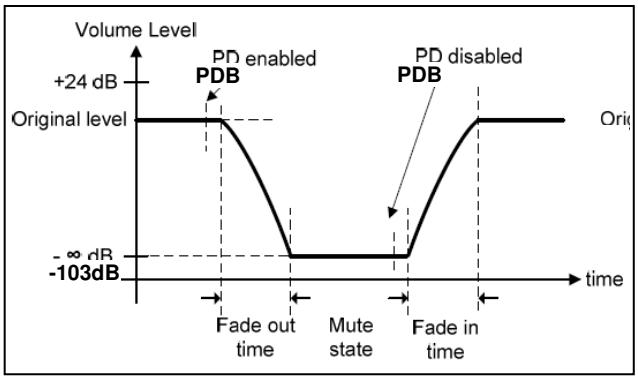


Figure 30 Power Down Timing Diagrams With Mute

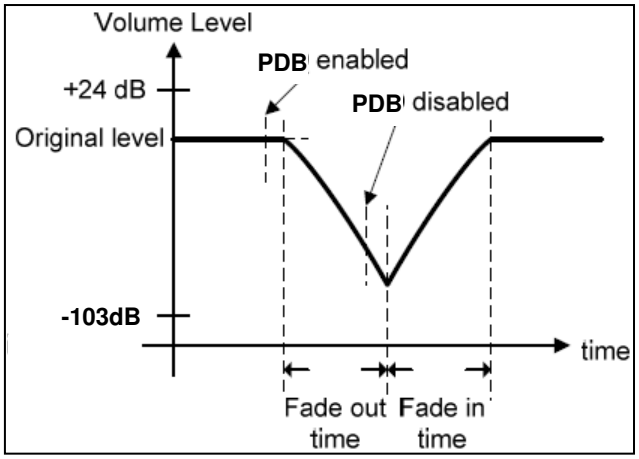


Figure 31 Power Down Timing Diagrams

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, IS31AP2121 will turn off the power stages, stop clock signals (MCLK, BCLK) from feeding into digital circuit and turn off the current of the internal analog circuits. After PDB pin is pulled low, IS31AP2121 needs up to 256 LRCIN clocks to finish the above works before entering power down state. Users can't program IS31AP2121 during power down state, but all the settings of register table will still be kept except that DVDD is removed.

If the PD function is disabled in the midway of the fade-out procedure, IS31AP2121 will also execute the fade-in procedure. In addition, IS31AP2121 will establish the analog circuits' bias current and feed the clock signals (MCLK, BCLK) into digital circuits. Then, IS31AP2121 will return to its normal operation without power down.

SELF-PROTECTION CIRCUITS

IS31AP2121 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

Thermal Protection

When the internal junction temperature is higher than 158°C, power stages will be turned off and IS31AP2121 will return to normal operation once the

temperature drops to 125°C. The temperature values may vary around 10%.

Short-Circuit Protection

The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 7A for stereo configuration or less than 14A for mono configuration. Otherwise, the short-circuit detectors may pull the ERRORB pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain ERRORB pin will be pulled low and latched into ERROR state.

Once the over-temperature or short-circuit condition is removed, IS31AP2121 will exit ERROR state when one of the following conditions is met: (1) RSTB pin is pulled low. (2) PDB pin is pulled low. (3) Master mute is enabled through the I2C interface.

Under-voltage Protection

Once the V_{DD} voltage is lower than 2.7V, IS31AP2121 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When V_{DD} becomes larger than 2.8V, IS31AP2121 will return to normal operation.

ANTI-POP DESIGN

IS31AP2121 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

3D SURROUND SOUND

IS31AP2121 provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

I2C CHIP SELECT

ERRORB is an input pin during power. It can be pulled High (15kΩ pull up) or Low (15kΩ pull down). Low indicates an I2C address of 0x30, and high an address of 0x31.

OUTPUT CONFIGURATION

The bit 4 [SEM] of address 0X11 and PBTL pin defines the configuration mode. IS31AP2121 can be configured to stereo, mono via PBTL pin (the bit 4 [SEM] of address 0X11 default is low). 2.1CH output mode configuration, user can via I2C to program it from the bit 4 [SEM] of address 0X11. Table 2 provides a reference of available configuration.

Table 2 Output Configurations

[SEM]	PBTL	Configuration Mode
0	0	Stereo
0	1	Mono
1	x	2.1CH

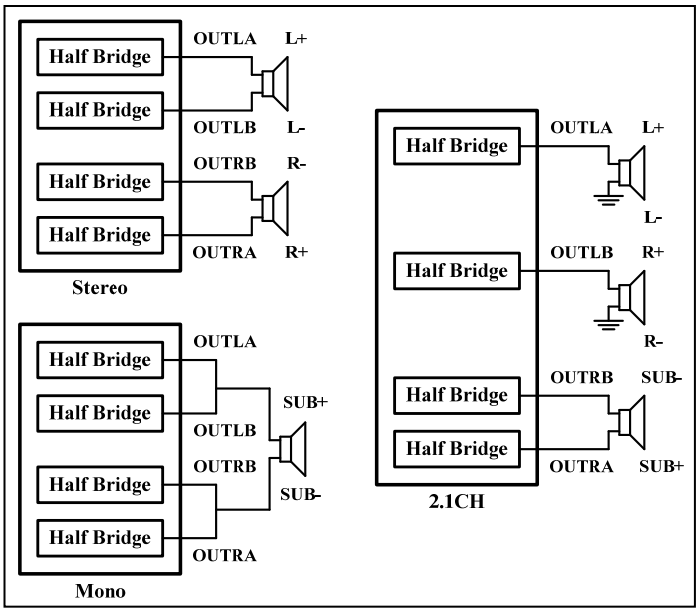


Figure 32 Output Configurations

POWER ON SEQUENCE

Hereunder is IS31AP2121's power on sequence. Give a de-mute command via I2C when the whole system is stable.

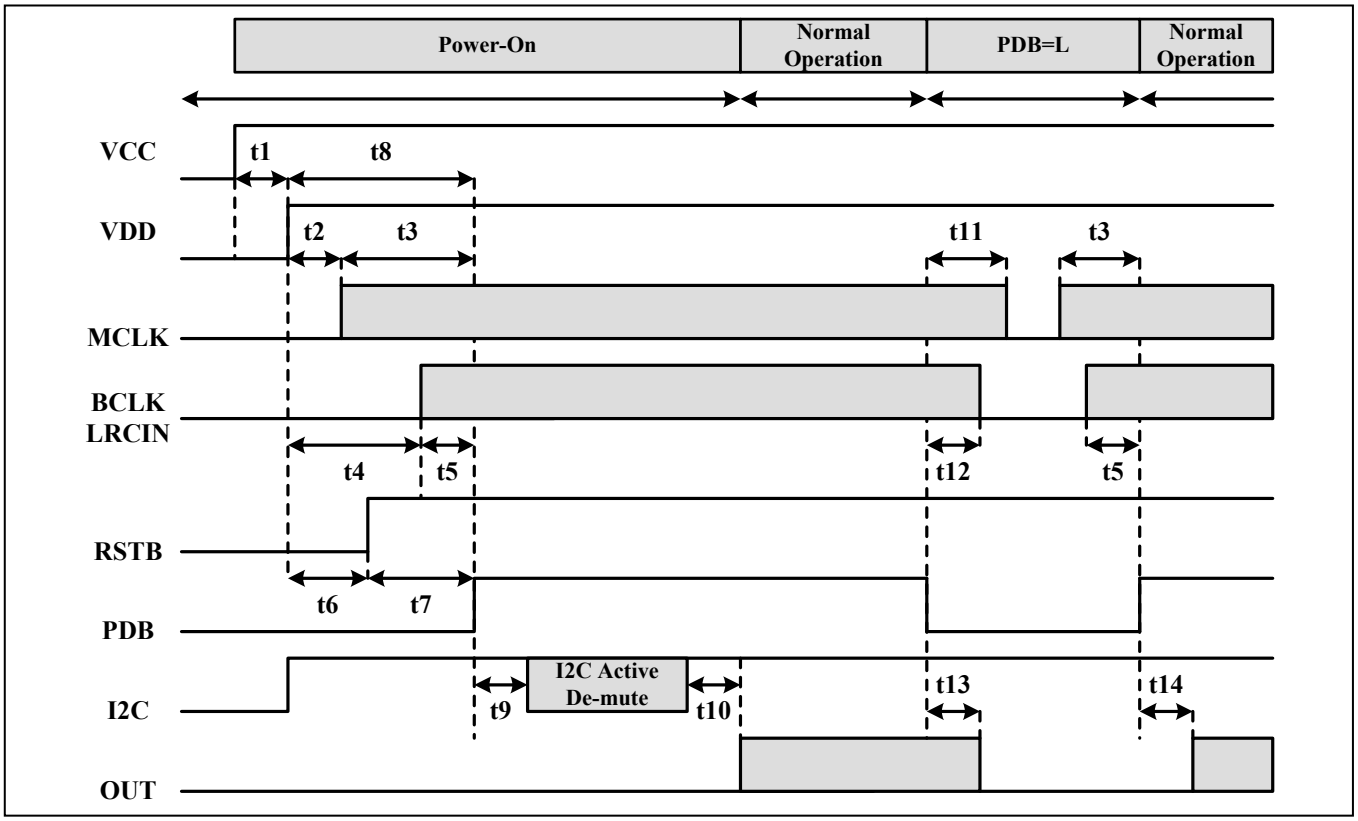


Figure 33 Power On Sequence

Table 2 Power On Sequence

Symbol	Condition	Min.	Max.	Unit
t1		0	-	ms
t2		0	-	ms
t3		10	-	ms
t4		0	-	ms
t5		10	-	ms
t6		10	-	ms
t7		0	-	ms
t8		200	-	ms
t9		20	-	ms
t10		-	0.1	ms
t11		25	-	ms
t12		25	-	ms
t13		-	22	ms
t14		-	0.1	ms

POWER OFF SEQUENCE

Hereunder is IS31AP2121's power off sequence.

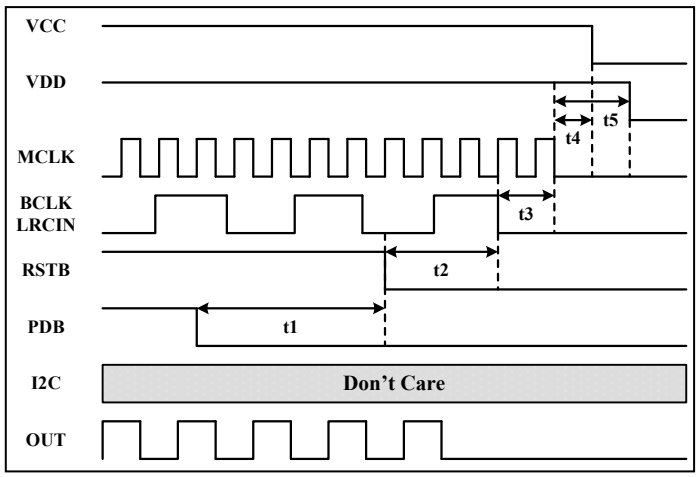


Figure 34 Power Off Sequence

Table 3 Power Off Sequence

Symbol	Min.
t1 (With I2C Control)	35ms
t1 (Without I2C Control)	5ms
t2	0ms (Note)
t3	0ms
t4	1ms
t5	1ms

Note: When t2 is less than 0.1ms, pop noise may occur.

I2C-BUS TRANSFER PROTOCOL

INTRODUCTION

IS31AP2121 employs I2C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. IS31AP2121 is always an I2C slave device.

PROTOCOL

START and STOP Condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between IS31AP2121 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

Data Validity

The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. IS31AP2121 samples the SDA signal at the rising edge of SCL signal.

Device Addressing

The master generates 7-bit address to recognize slave devices. When IS31AP2121 receives 7-bit address matched with 0110000 or 0110001 (ERRORB pin state during power up), IS31AP2121 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for IS31AP2121 internal sub-addresses.

Data Transferring

Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, IS31AP2121 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.

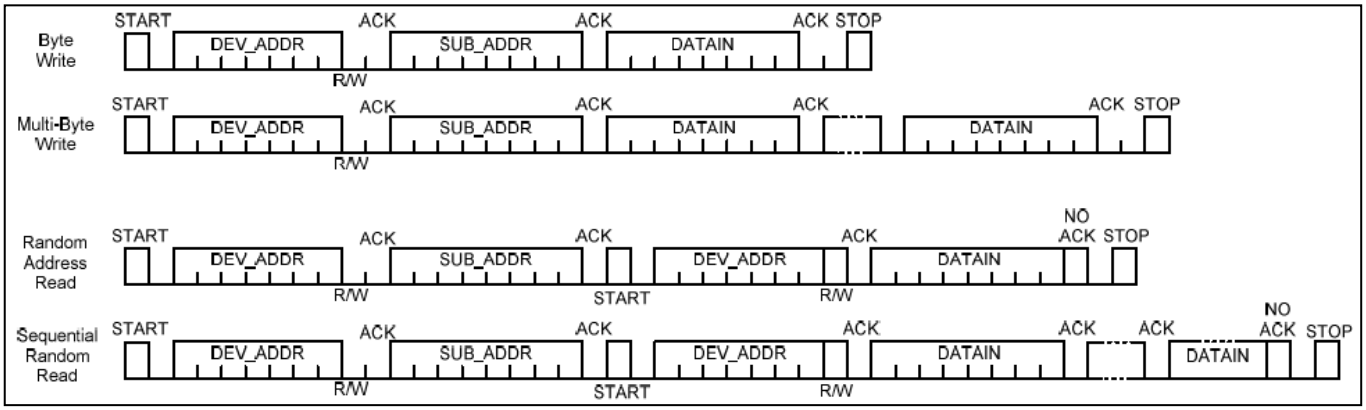
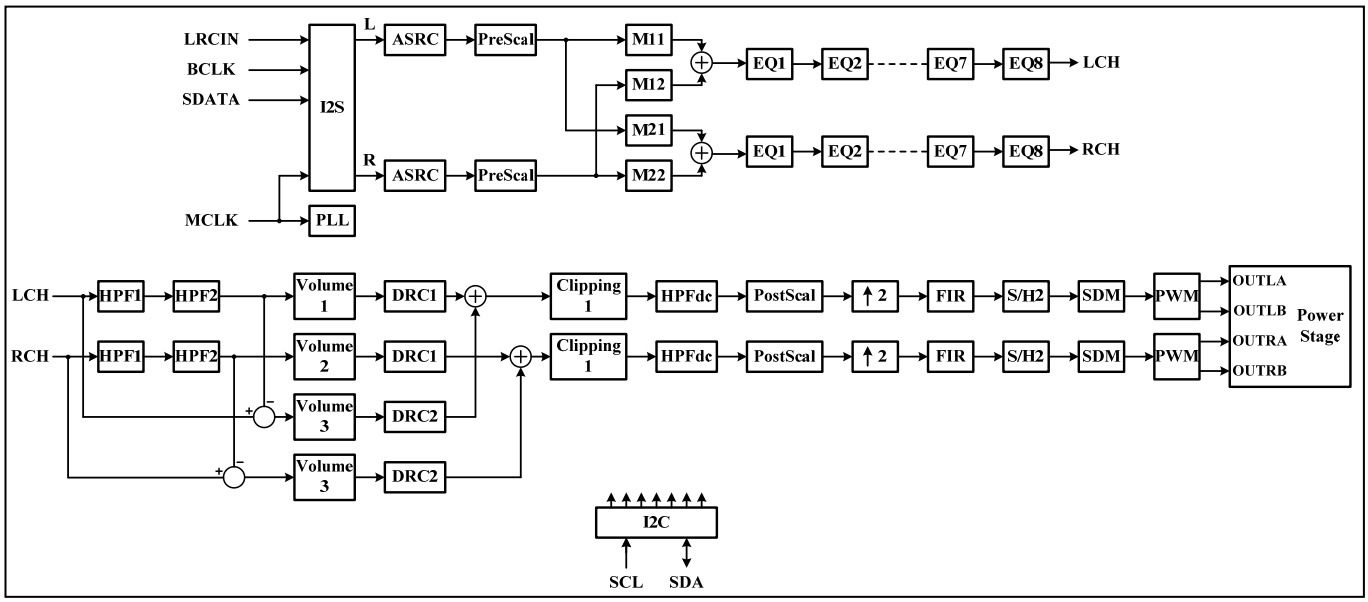


Figure 35 Data Transferring

REGISTER DEFINITIONS

The IS31AP2121's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

Dual Band DRC Enable (Only for stereo mode, PBTL=Low)



Dual Band DRC Disable

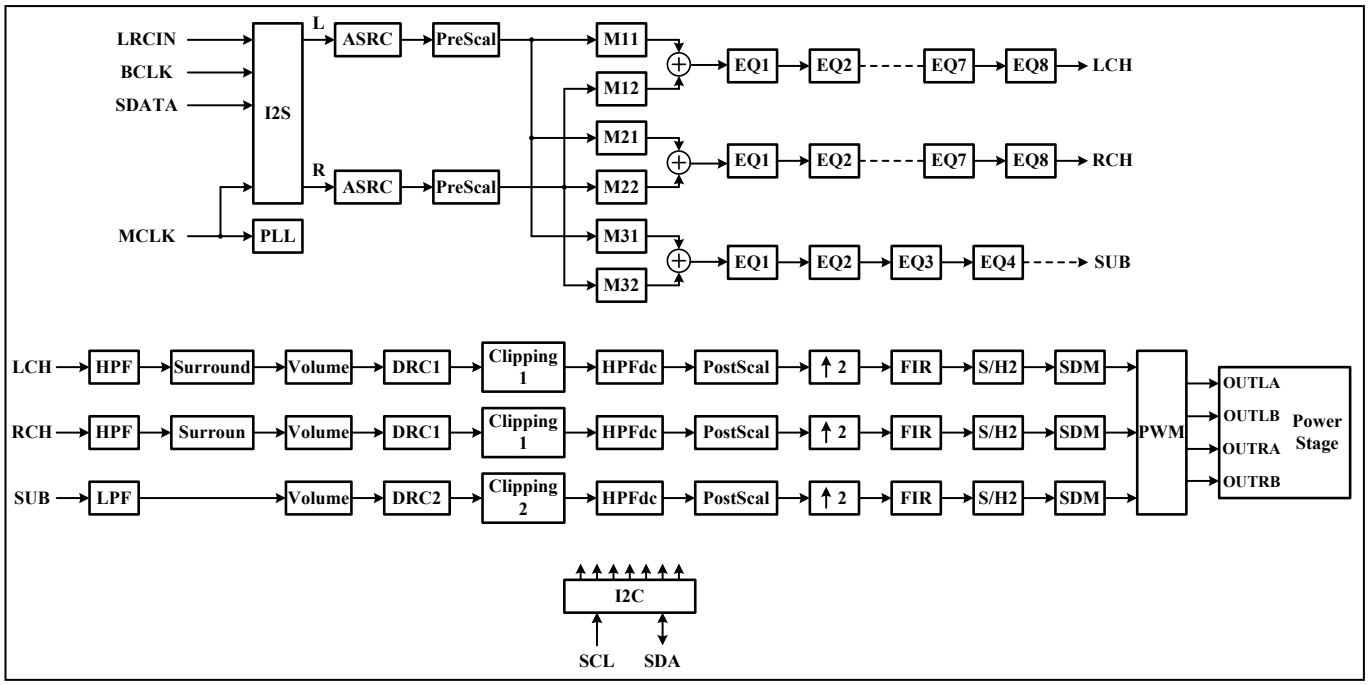


Table 4 Register Function

Address	Name	Table	Default
00h	State Control 1 Register	5	000x 0100
01h	State Control 2 Register	6	x000 0100
02h	State Control 3 Register	7	0xxx 1111
03h	Master Volume Control Register	8	0001 1000
04h~06h	Channel 1~3 Volume Register	9	0001 0100
07h,08h	Bass/Treble Tone Register	10	xxx1 0000
09h	Bass Management Crossover Frequency Register	11	xxxx 0010
0Ah	State Control 4 Register	12	1001 0000
0Bh~0Ch	Channel 1~2 Configuration Register	13	xxx1 0010
0Dh	Channel 3 Configuration Register	14	xxx1 0000
0Eh	DRC Limiter Attack/Release Rate Register	15	0110 1010
0Fh~10h	Reserved	-	-
11h	State Control 5 Register	16	xx11 0010
12h	VCC Under-voltage Selection Register	17	1xxx 0001
13h	Noise Gate Gain Register	18	x000 xx00
14h	Coefficient RAM Base Address Register	19	x000 0000
15h~23h	User-Defined Coefficients Register	20~24	-
24h	Coefficients Control Register	25	xxxx 0000
25h~29h	Reserved	-	-
2Ah	Power Saving Mode Switching Level Register	26	xxx0 1101
2Bh	Volume Fine Tune Register	27	0011 1111

Note: The reserved registers are not allowed to write any bits in them, or the IC will be abnormal.

Table 5 00h State Control 1 Register

Bit	D7:D5	D4	D3
Name	IF	-	PWML_X
Default	000	x	0
Bit	D2	D1	D0
Name	PWMR_X	LV_UVSEL	LREXC
Default	1	0	0

IS31AP2121 supports multiple serial data input formats including I2S, Left-alignment and Right-alignment. These formats are selected by users via D7~D5 of address 00h. The left/right channels can be exchanged to each other by programming to address 00h/D0, LREXC.

IF	Input Format
000	I2S 16-24 bits
001	Left-alignment 16-24 bits
010	Right-alignment 16 bits
011	Right-alignment 18 bits
100	Right-alignment 20 bits
101	Right-alignment 24 bits
Others	Not available

PWML_X	OUTLA/B exchange
0	No exchanged
1	L/R exchanged

PWMR_X	OUTRA/B exchange
0	L/R exchanged
1	No exchanged

LV_UVSEL	LV Under-voltage Selection
0	2.7V
1	3.0V

LREXC	Left/Right Channel Exchanged
0	No exchange
1	L/R exchange

Table 6 01h State Control 2 Register

Bit	D7:	D6	D5:D4	D3:D0
Name	-	BCLK_SEL	FS	PMF
Default	x	0	00	0100

IS31AP2121 has a built-in PLL and support multiple MCLK/Fs ratios. Detail setting is shown in the following table.

BCLK_SEL	MCLK-less (BCLK system)
0	Disabled
1	Enable

FS	Sampling Frequency
00	32/44.1/48kHz
01	64/88.2/96kHz
1x	128/176.4/192kHz

PMF	Multiple MCLK/F_S Ratio Setting
0000	1024x(FS=00)/ 512x(FS=01)/ 256x(FS=1x)
0001	64x
0010	128x
0011	192x
0100	256x
0101	384x (Not available when FS=1x)
0110	512x (Not available when FS=1x)
0111	576x (Not available when FS=01,1x)
1000	768x (Not available when FS=01,1x)
1001	1024x (Not available when FS=01,1x)
Others	Not available

Note: The FS × PMF should be lower than 49.152MHz, or the system will be error.

Table 7 02h State Control 3 Register

Bit	D7	D6:D4	D3	D2:D0
Name	EN_CLK_OUT	-	MUTE	CM1:CM3
Default	0	xxx	1	111

IS31AP2121 has mute function including master mute and channel mute. When master mute is enabled, all 3 processing channels are muted. User can mute these 3 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

EN_CLK_OUT	PLL Clock Output
0	Disabled
1	Enable

MUTE	Master Mute
0	All channel not muted
1	All channel muted

CMx	Channel x Mute
0	Channel x not muted
1	Only channel x muted

Table 8 03h Master Volume Control Register

Bit	D7:D0
Name	MV
Default	0001 1000

IS31AP2121 supports both master-volume (03h Register) and channel-volume control (04h, 05h and 06h Registers) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B. -103dB ≤ Total volume (Level A + Level B) ≤ +24dB.

MV	Master Volume
0000 0000	+12.0dB
0000 0001	+11.5dB
0000 0010	+11.0dB
…	
0001 1000	0dB
…	
1110 0110	-103.0dB
1110 0111	-∞
Others	-∞