Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

IS31FL3740

3×4 DOTS MATRIX LED DRIVER WITH INDIVIDUAL AUTO BREATH FUNCTION

January 2018

GENERAL DESCRIPTION

The IS31FL3740 is a general purpose 3×4 LEDs matrix driver with 1/12 cycle rate. The device can be programmed via an I2C compatible interface. Each LED can be dimmed individually with 8-bit × 8 PWM data which allowing 1024 steps of linear dimming.

IS31FL3740 features 3 Auto Breathing Modes which are noted as ABM-1, ABM-2 and ABM-3. For each Auto Breathing Mode, there are 4 timing characters which include current rising / holding / falling / off time and 3 loop characters which include Loop-Beginning / Loop-Ending / Loop-Times. Every LED can be configured to be any Auto Breathing Mode or No-Breathing Mode individually.

Additionally each LED open and short state can be detected, IS31FL3740 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3740 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3740 is available in QFN-20 (5mm×5mm) and eTSSOP-20 packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 4 current source outputs for row control
- 3 switch current inputs for column scan control
- Up to 12 LEDs (3×4) in dot matrix
- Programmable 3×4 (4 RGBs) matrix size with de-ghost function
- 1MHz I2C-compatible interface
- Selectable 3 Auto Breath Modes for each dot
- Auto breath loop features interrupt pin inform MCU auto breath loop completed
- Auto breath offers128 steps gamma current, interrupt and state lookup registers
- 256 steps global current setting
- Individual on/off control
- Individual 1024 PWM control steps
- Individual Auto Breath Mode select
- Individual open and short error detect function
- Cascade for synchronization of chips
- QFN-20 (5mm×5mm) and eTSSOP-20 packages

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

TYPICAL APPLICATION CIRCUIT

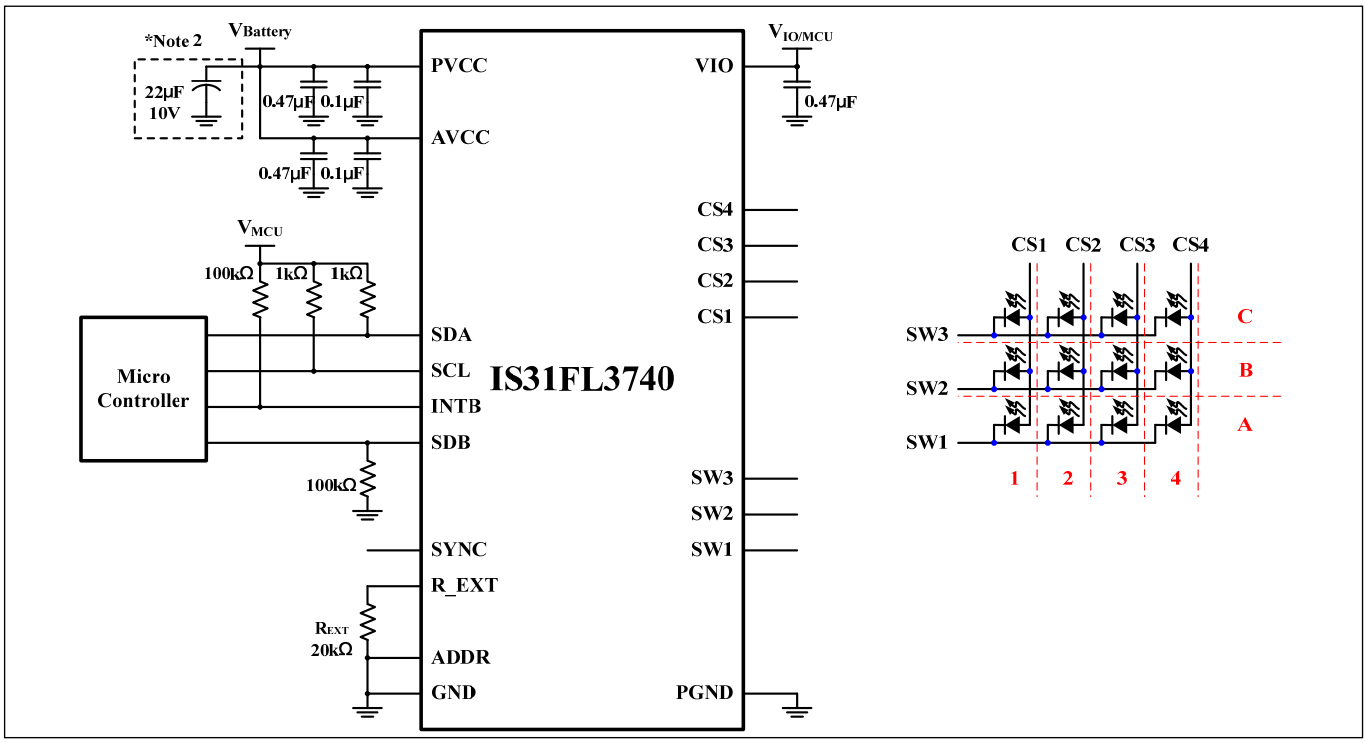


Figure 1 Typical Application Circuit (3×4)

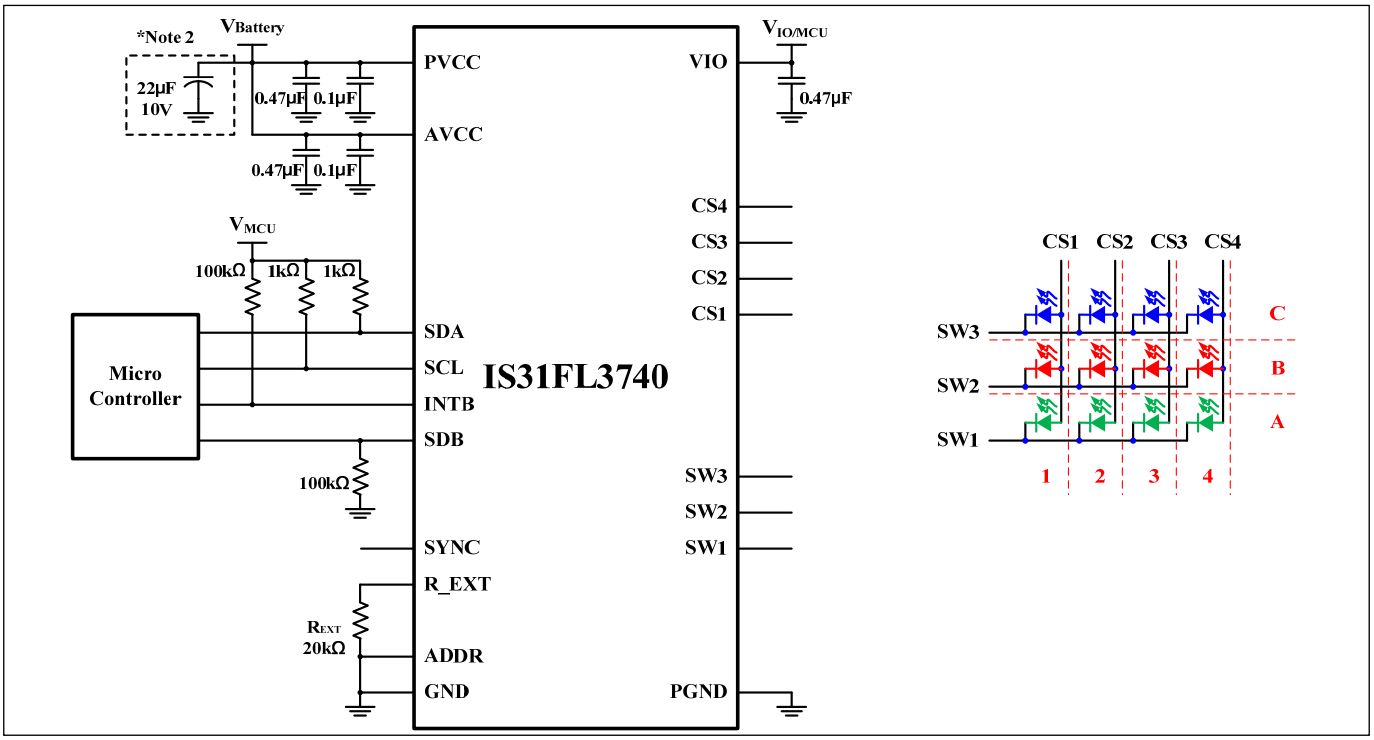


Figure 2 Typical Application Circuit (RGB)

Note 1: For the mobile applications the IC should be placed far away from the mobile antenna in order to prevent the EMI.

Note 2: Electrolytic/Tantalum Capacitor may considerable for high current application to avoid audible noise interference.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

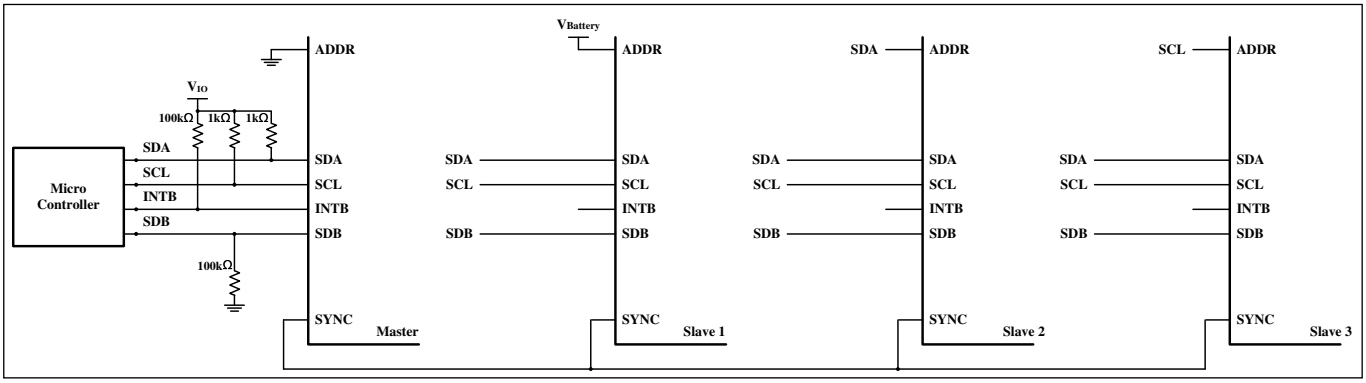
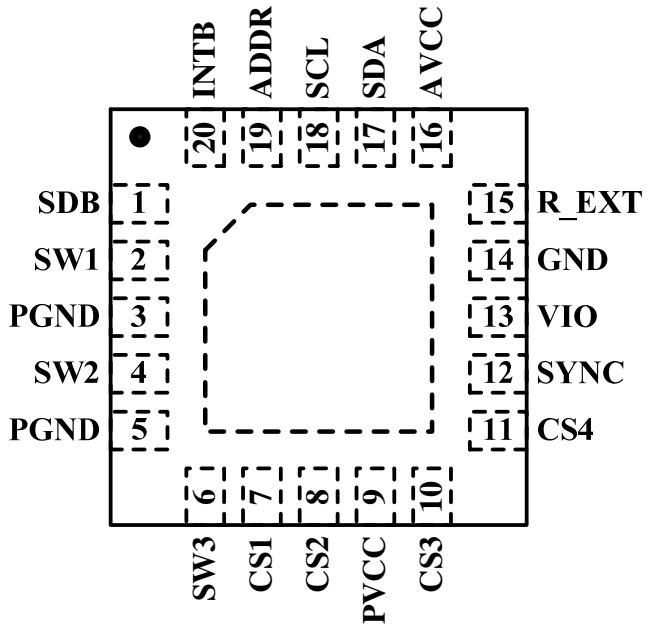
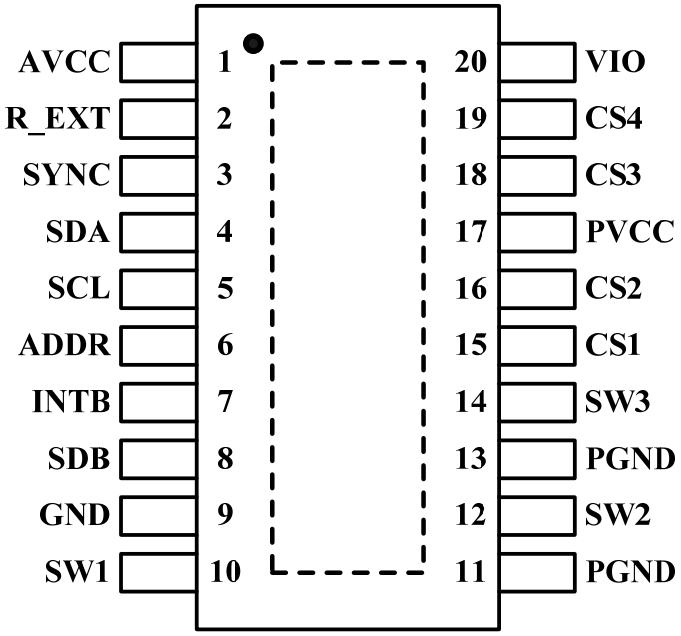


Figure 3 Typical Application Circuit (Four Parts Synchronization-Work)

Note 3: One part is configured as master mode, all the other 3 parts configured as slave mode. Work as master mode or slave mode specified by Configuration Register (Function register, address 00h).Master part output master clock, and all the other parts which work as slave input this master clock.

Note 4: The VIO should be 1.8V≤ V_{IO} ≤V_{CC}. And it is recommended to be equal to V_{OH} of the micro controller. For example, if V_{OH}=1.8V, set V_{IO}=1.8V is recommended.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	
eTSSOP-20	

PIN DESCRIPTION

No.		Pin	Description
QFN	eTSSOP		
16	1	AVCC	Power for analog circuits.
15	2	R_EXT	Input terminal used to connect an external resistor. This regulates current source DC current value.
12	3	SYNC	Synchronize pin. It is used for more than one part work synchronize. If it is not used please float this pin.
17	4	SDA	I2C compatible serial data.
18	5	SCL	I2C compatible serial clock.
19	6	ADDR	I2C address setting.
20	7	INTB	Interrupt output pin. Register F0h sets the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function no used.
1	8	SDB	Shut down the chip when pull to low.
14	9	GND	Connect to GND.
2,4,6	10,12,14	SW1~SW3	Switch pin for LED matrix scanning.
3,5	11,13	PGND	Power GND.
7,8, 10,11	15,16, 18,19	CS1~CS4	Current source.
9	17	PVCC	Power for current source.
13	20	VIO	Input logic reference voltage.
		Thermal Pad	Need to connect to GND pins.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3740-QFLS4-TR	QFN-20, Lead-free	2500
IS31FL3740-ZLS4-TR	eTSSOP-20, Lead-free	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	32.8°C/W (eTSSOP) 42.4°C/W (QFN)
ESD (HBM) ESD (CDM)	±2kV ±750V

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 3.6V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= $V_{CC,}$ all LEDs off		2.17		mA
I_{SD}	Shutdown current	V_{SDB}= 0V		3		μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000		3		
I_{OUT}	Maximum constant current of CS1~CS4	R_{EXT}= 20kΩ		84		mA
I_{LED}	Average current on each LED I_{LED}= (I_{OUT}/2/12.75)×8	R_{EXT}= 20kΩ, GCC= 255, All PWM= 255		26.3		mA
V_{HR}	Current sink headroom voltage SW1~SW3	I_{SINK}= 336mA (Note 1, 2)		200		mV
	Current source headroom voltage CS1~CS4	I_{SOURCE}= 84mA (Note 1)		350		
t_{SCAN}	Period of scanning			128		μs
t_{NOL}	Non-overlap blanking time during scan, the SWy and CSx are all off during this time			8		μs
Logic Electrical Characteristics (SDA, SCL, ADDR, SYNC, SDB)						
V_{IL}	Logic "0" input voltage	V_{IO}= 3.6V	GND		0.2V_{IO}	V
V_{IH}	Logic "1" input voltage	V_{IO}= 3.6V	0.75V_{IO}		V_{IO}	V
V_{HYS}	Input schmitt trigger hysteresis	V_{IO}= 3.6V		0.2		V
V_{OL}	Logic "0" output voltage for SYNC	I_{OL}= 8mA			0.4	V
V_{OH}	Logic "1" output voltage for SYNC	I_{OH}= 8mA	0.75V_{IO}			V
I_{IL}	Logic "0" input current	V_{INPUT}= 0V (Note 3)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= V_{IO} (Note 3)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 3)

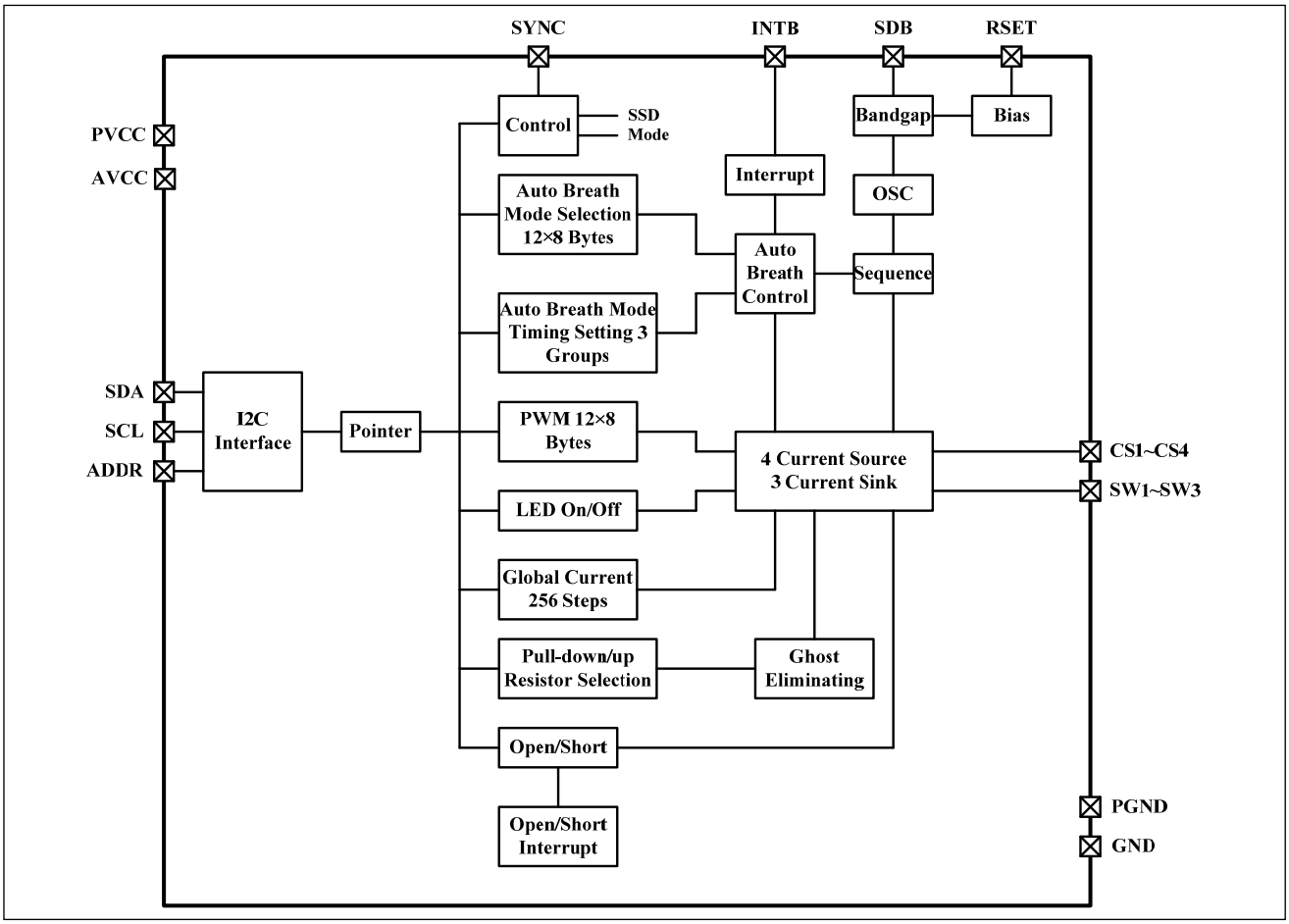
Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 1: In case of R_{EXT} = 20kΩ, Global Current Control Register (PG3, 01h) written “1111 1111”, GCC = “1111 1111”.

Note 2: All LEDs are on and PWM=“1111 1111”, GCC = “1111 1111”.

Note 3: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3740 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3740 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A4:A1 are decided by the connection of the ADDR pin. The complete slave address is:

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A1	A0
GND	GND	101	0000	0/1
SCL	SCL		0101	
SDA	SDA		1010	
VCC	VCC		1111	

ADDR connected to GND, (A4:A1)=0000;
ADDR connected to VCC, (A4:A1)=1111;
ADDR connected to SCL, (A4:A1)=0101;
ADDR connected to SDA, (A4:A1)=1010;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 1kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3740.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDAsignal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3740's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3740 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3740, the register address byte is sent, most significant bit first. IS31FL3740 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3740 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3740, load the address of the data register that the first data byte is intended for. During the IS31FL3740 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3740 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3740 (Figure 7).

READING OPERATION

Register FEh, F1h, 18h~28h, 30h~40h of Page 0 and 11h of Page 3 can be read.

To read the FEh and F1h, after IIC start condition, the bus master must send the IS31FL3740 device

address with the R/$\overline{W}$ bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3740 device address with the

R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3740 to the master (Figure 8).

To read the 18h~28h, 30h~40h of Page 0 and 11h of Page 3, the FDh should write with 00h before follow the Figure 8 sequence to read the data, that means, when you want to read 18h~28h, 30h~40h of Page 0 and 11h of Page 3, the FDh should point to Page 0 or Page 3 first and then you can read the data.

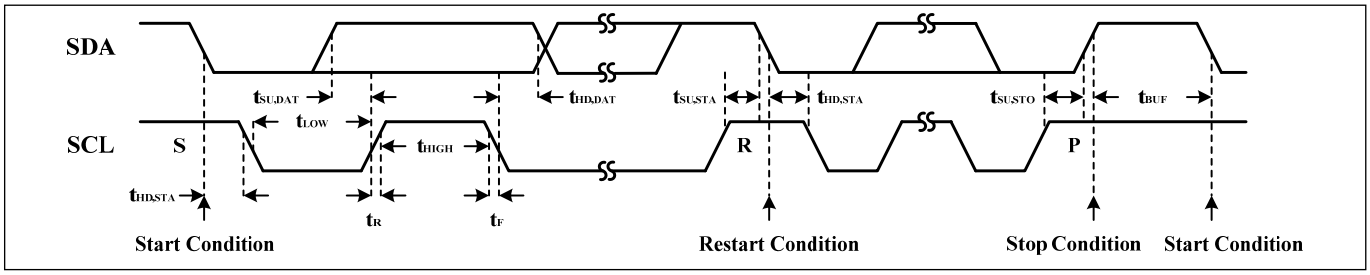


Figure 4 Interface Timing

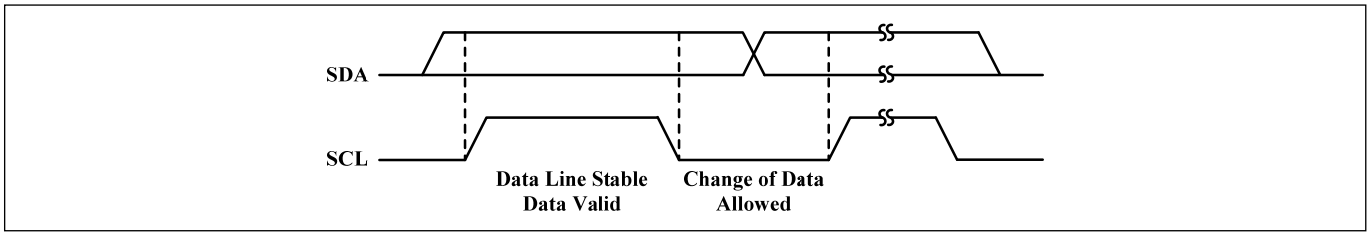


Figure 5 Bit Transfer

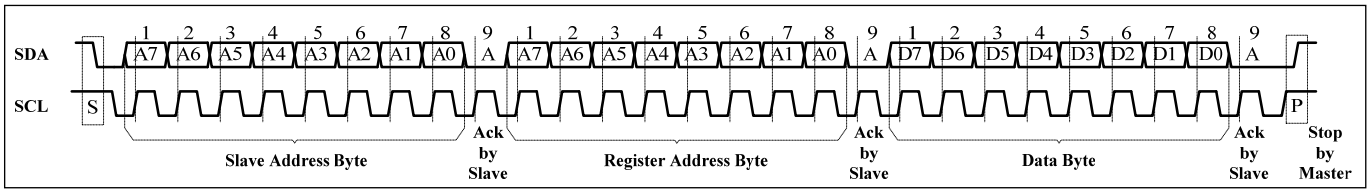


Figure 6 Writing to IS31FL3740 (Typical)

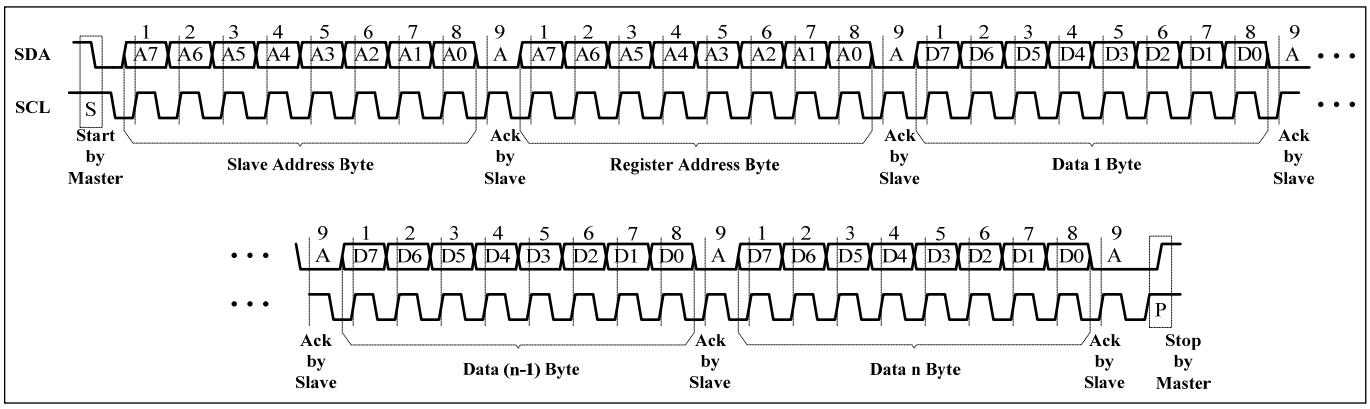


Figure 7 Writing to IS31FL3740 (Automatic Address Increment)

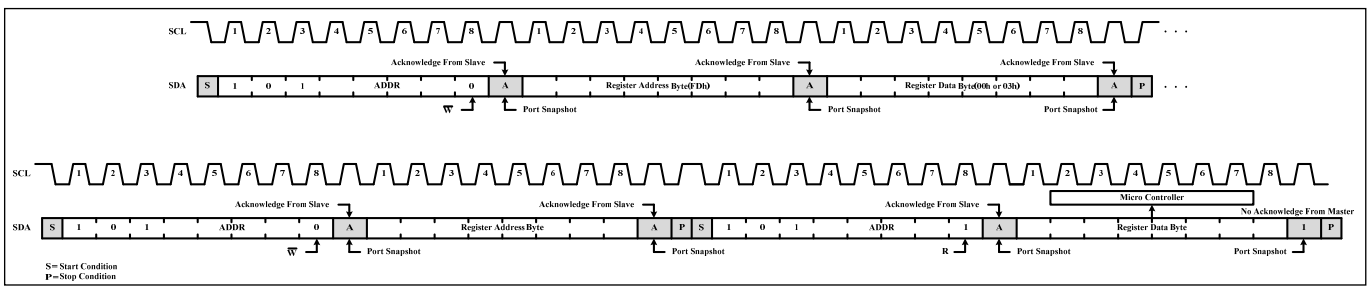


Figure 8 Reading from IS31FL3740

REGISTER DEFINITION-1

Address	Name	Function	Table	R/W	Default
FDh	Command Register	Available Page 0 to Page 3 Registers	2	W	0000 0000
FEh	Command Register Write lock	To lock/unlock Command Register	3	R/W	0000 0000
F0h	Interrupt Mask Register	Configure the interrupt function	4	W	
F1h	Interrupt Status Register	Show the interrupt status	5	R	

REGISTER CONTROL

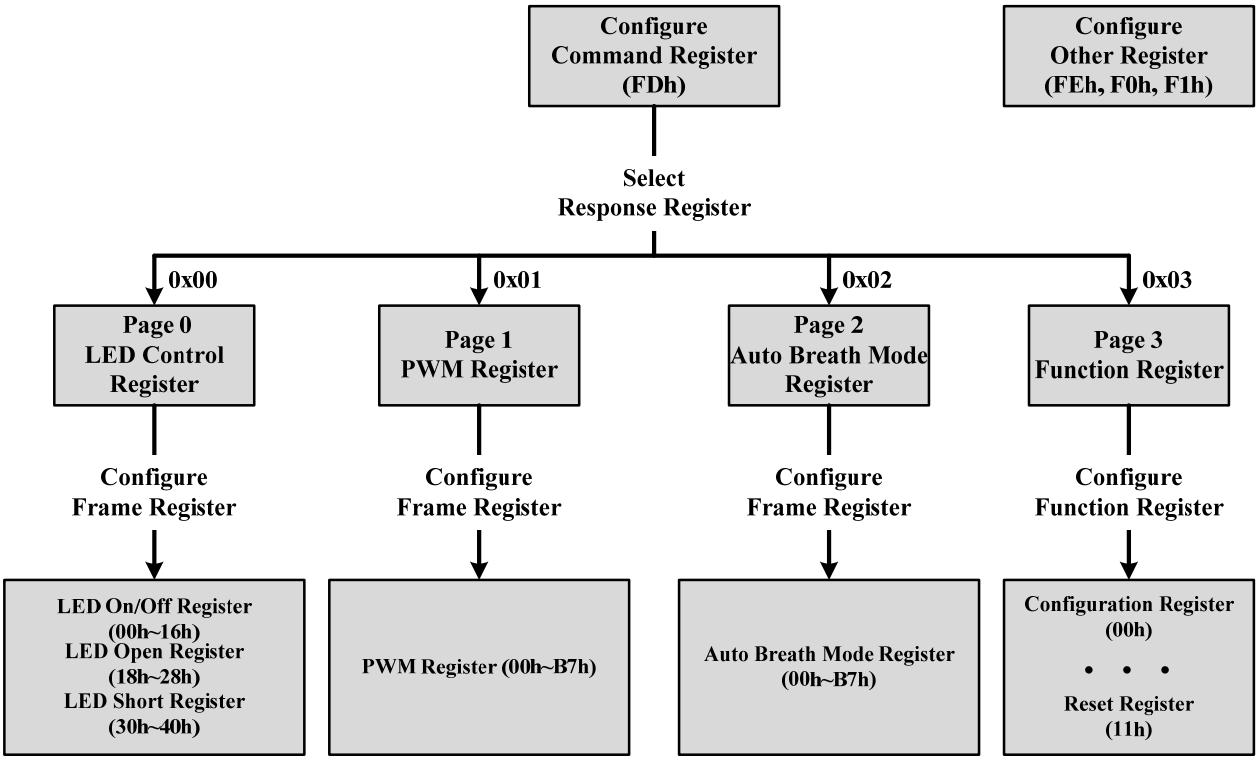


Table 2 FDh Command Register (Write Only)

Data	Function
0000 0000	Point to Page 0 (PG0, LED Control Register is available)
0000 0001	Point to Page 1 (PG1, PWM Register is available)
0000 0010	Point to Page 2 (PG2, Auto Breath Mode Register is available)
0000 0011	Point to Page 3 (PG3, Function Register is available)
Others	Reserved

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 3 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is "0000 0000".

For example, when write "0000 0001" in the Command Register (FDh), the data which writing after will be stored in the Auto breath mode Register. Write new data can configure other registers.

Table 3 FEh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000 (FDh write disable)

To select the PG0~PG3, need to unlock this register first, with the purpose to avoid mis-operation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

CRWL Command Register Write Lock
0x00 FDh write disable
0xC5 FDh write enable once

Table 4 F0h Interrupt Mask Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	IAC	IAB	IS	IO
Default	0000	0	0	0	0

Configure the interrupt function for IC.

IAC Auto Clear Interrupt Bit
0 Interrupt could not auto clear
1 Interrupt auto clear when INTB stay low exceeds 8ms

IAB Auto Breath Interrupt Bit
0 Disable auto breath loop finish interrupt
1 Enable auto breath loop finish interrupt

IS Dot Short Interrupt Bit
0 Disable dot short interrupt
1 Enable dot short interrupt

IO Dot Open Interrupt Bit
0 Disable dot open interrupt
1 Enable dot open interrupt

Table 5 F1h Interrupt Status Register

Bit	D7:D5	D4	D3	D2	D1	D0
Name	-	ABM3	ABM2	ABM1	SB	OB
Default	000	0	0	0	0	0

Show the interrupt status for IC.

ABM3 Auto Breath Mode 3 Finish Bit
0 ABM3 not finish
1 ABM3 finish

ABM2 Auto Breath Mode 2 Finish Bit
0 ABM2 not finish
1 ABM2 finish

ABM1 Auto Breath Mode 1 Finish Bit
0 ABM1 not finish
1 ABM1 finish

SB Short Bit
0 No short
1 Short happens

OB Open Bit
0 No open
1 Open happens

REGISTER DEFINITION-2

Address	Name	Function	Table	R/W	Default
PG0 (0x00): LED Control Register					
00h ~ 16h	LED On/Off Register	Set on or off state for each LED	7	W	0000 0000
18h ~ 28h	LED Open Register	Store open state for each LED	8	R	
30h ~ 40h	LED Short Register	Store short state for each LED	9	R	
PG1 (0x01): PWM Register					
00h~B7h	PWM Register	Set PWM duty for LED	10	W	0000 0000
PG2 (0x02): Auto Breath Mode Register					
00h~B7h	Auto Breath Mode Register	Set operating mode of each dot	11	W	xxxx xx00
PG3 (0x03): Function Register					
00h	Configuration Register	Configure the operation mode	13	W	0000 0000
01h	Global Current Control Register	Set the global current	14	W	
02h	Auto Breath Control Register 1 of ABM-1	Set fade in and hold time for breath function of ABM-1	15	W	
03h	Auto Breath Control Register 2 of ABM-1	Set the fade out and off time for breath function of ABM-1	16	W	
04h	Auto Breath Control Register 3 of ABM-1	Set loop characters of ABM-1	17	W	
05h	Auto Breath Control Register 4 of ABM-1	Set loop characters of ABM-1	18	W	
06h	Auto Breath Control Register 1 of ABM-2	Set fade in and hold time for breath function of ABM-2	15	W	
07h	Auto Breath Control Register 2 of ABM-2	Set the fade out and off time for breath function of ABM-2	16	W	
08h	Auto Breath Control Register 3 of ABM-2	Set loop characters of ABM-2	17	W	
09h	Auto Breath Control Register 4 of ABM-2	Set loop characters of ABM-2	18	W	
0Ah	Auto Breath Control Register 1 of ABM-3	Set fade in and hold time for breath function of ABM-3	15	W	
0Bh	Auto Breath Control Register 2 of ABM-3	Set the fade out and off time for breath function of ABM-3	16	W	
0Ch	Auto Breath Control Register 3 of ABM-3	Set loop characters of ABM-3	17	W	
0Dh	Auto Breath Control Register 4 of ABM-3	Set loop characters of ABM-3	18	W	
0Eh	Time Update Register	Update the setting of 02h ~ 0Dh registers	-	W	
0Fh	SWy Pull-Up Resistor Selection Register	Set the pull-up resistor for SWy	19	W	
10h	CSx Pull-Down Resistor Selection Register	Set the pull-down resistor for CSx	20	W	
11h	Reset Register	Reset all register to POR state	-	R	

Table 6-1 Page 0 (PG0, 0x00): LED Control Register - On Off Register

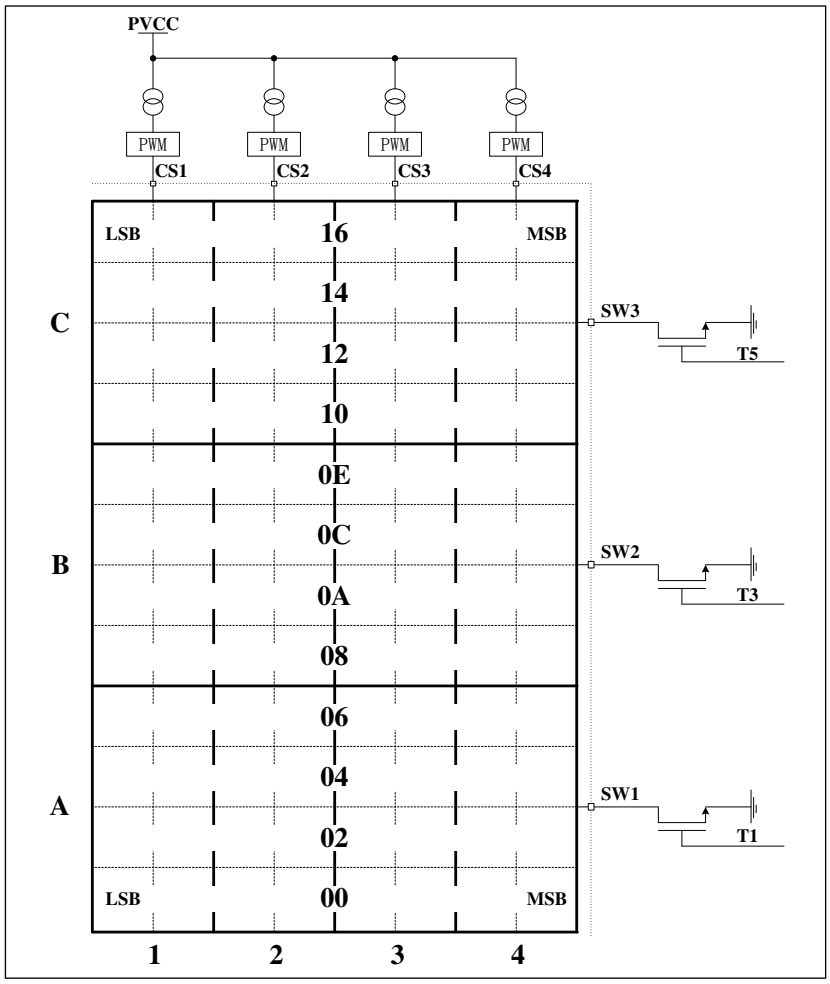


Figure 9 On Off Register

Table 7 00h ~ 16h LED On/Off Register

Bit	D7:D0
Name	C_{CS8} : C_{CS1} or C_{CS16} : C_{CS9}
Default	0000 0000

The LED On/Off Registers store the on or off state of each LED in the Matrix.

Each LED has 8 bits on and off state, need to turn on/off them when turn on/off the LED.

For example:

When turn on LED 1-A, need to turn on

D1:D0 of 00h, 02h, 04h and 06h

C_{X-Y}	LED State Bit
0	LED off
1	LED on

Table 6-2 Page 0 (PG0, 0x00): LED Control Register – Open Detect Register

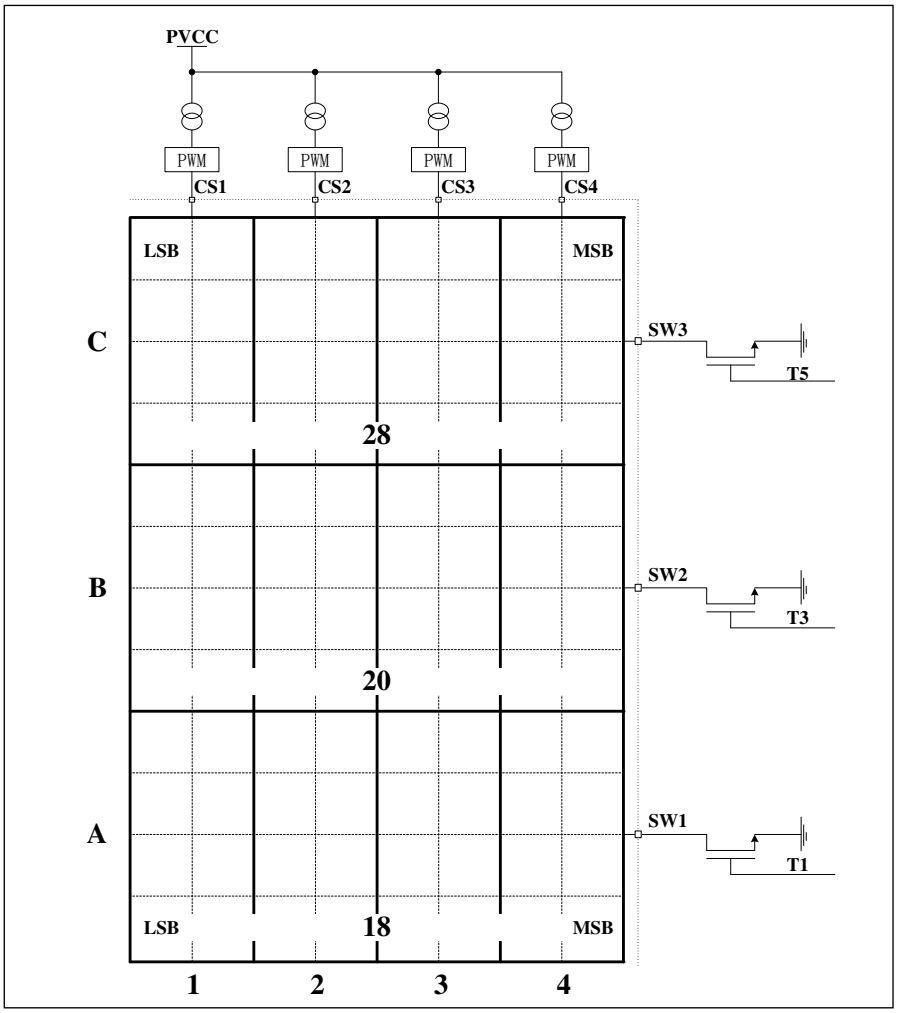


Figure 10 Open Detect Register

Table 8 18h ~ 28h LED Open Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OP_8	-	OP_6	-	OP_4	-	OP_2	-
Default	0	-	0	-	0	-	0	-

The LED Open Registers store the open or normal state of each LED in the Matrix.

OPx LED Open Bit
0 LED normal
1 LED open

Table 6-3 Page 0 (PG0, 0x00): LED Control Register – Short Detect Register

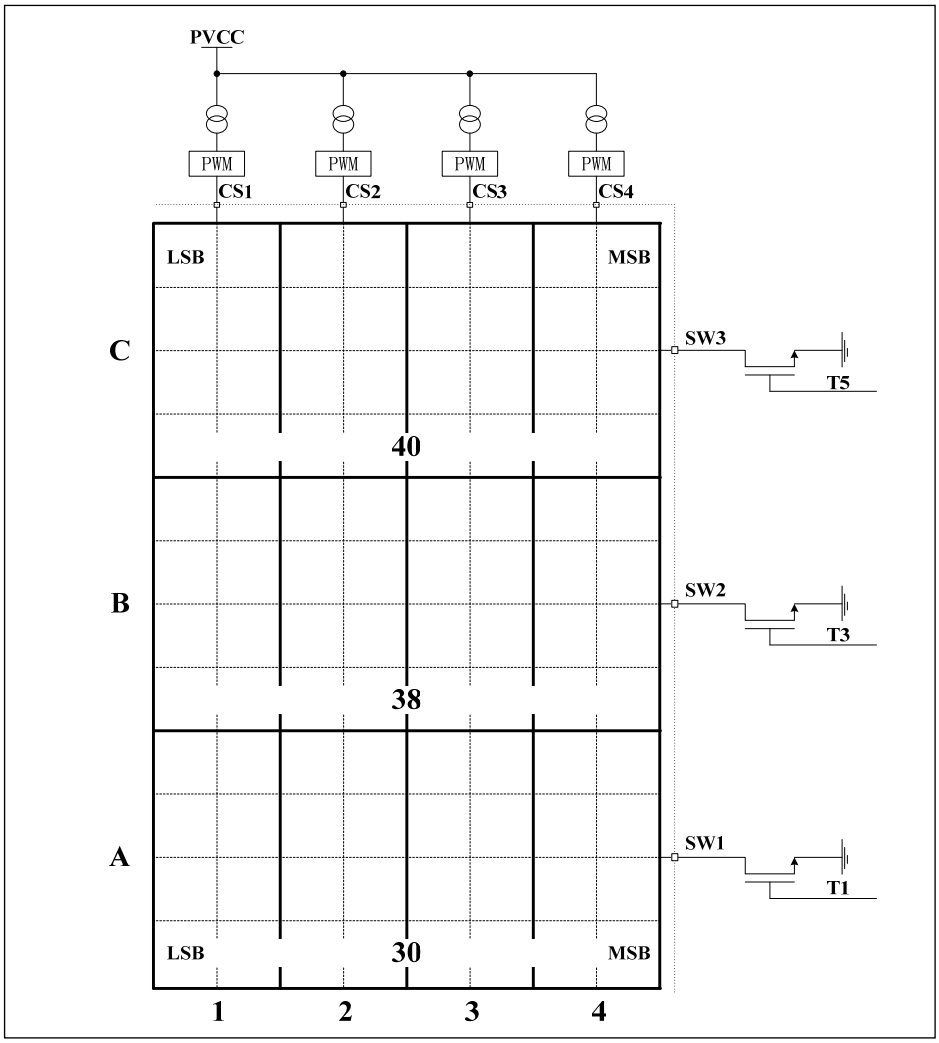


Figure 11 Short Detect Register

Table 9 30h ~ 40h LED Short Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ST_8	-	ST_6	-	ST_4	-	ST_2	-
Default	0	-	0	-	0	-	0	-

The LED Short Registers store the short or normal state of each LED in the Matrix.

OPx	LED Short Bit
0	LED normal
1	LED short

Page 1 (PG1, 0x01): PWM Register

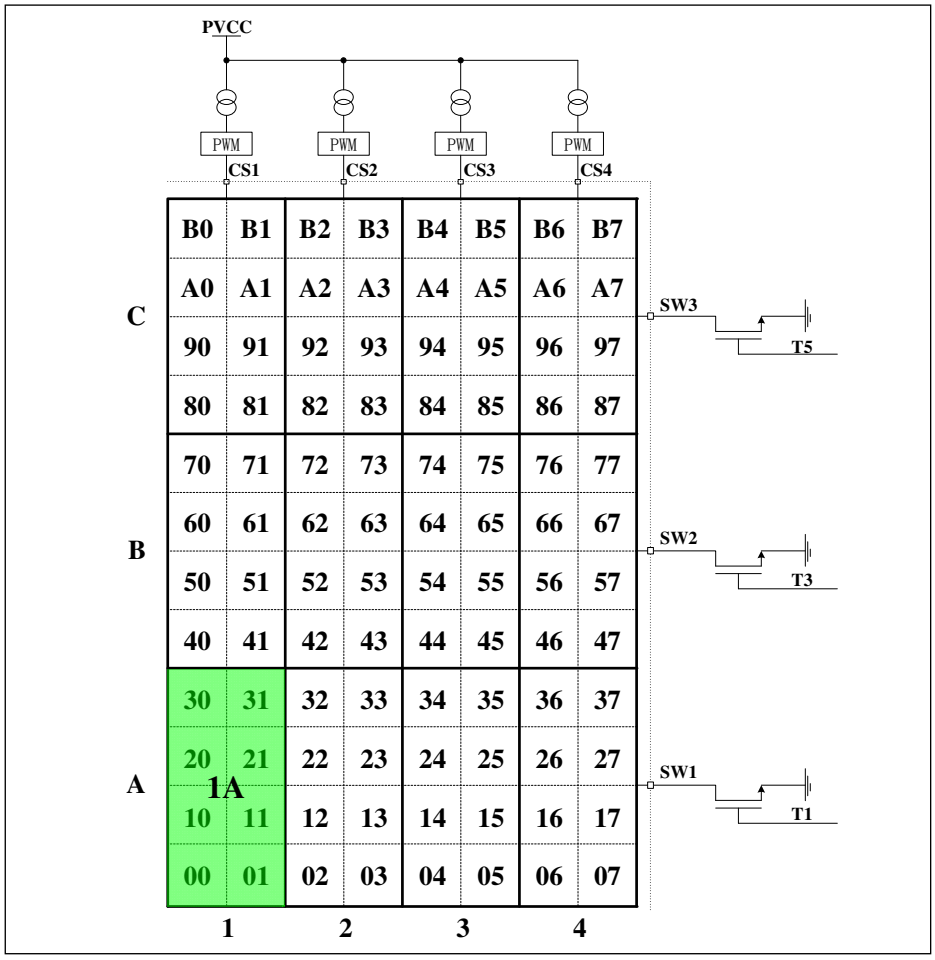


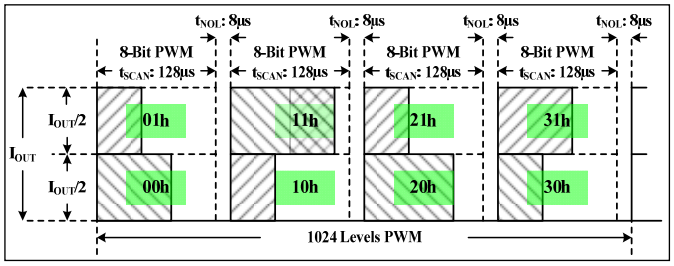
Figure 12 PWM Register

Table 10 00h ~ B7h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has 8 bytes to modulate the PWM duty in 1024 steps.

Each byte controls half of the I_{OUT} and quarter of the duty, like LED 1A (Figure 12), the current will be as shown below:



The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{\sum PWM}{256} \times (I_{OUT} / 2) \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWy/4,

$$Duty = \frac{128\mu s}{(128\mu s + 8\mu s)} \times \frac{1}{3} \times \frac{1}{4} = \frac{1}{12.75} \quad (2)$$

I_{OUT} is the output current of CSx (x=1~4),

$$I_{OUT} = \frac{840}{R_{EXT}} \times \frac{GCC}{256} \times 2 \quad (3)$$

GCC is the Global Current Control register (PG3, 01h) value and R_{EXT} is the external resistor of R_EXT pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example 1:

if 00h=0xff, 01h=0xff, 10h=0xff, 11h=0xff, 20h=0xff, 21h=0xff, 30h=0xff, 31h=0xff,GCC=0xff. R_{EXT}=20kΩ (I_{OUT}=84mA),

$$I_{LED-1A} = \frac{0xff \times 8}{256} \times (I_{OUT} / 2) \times \frac{1}{12.75}$$

$$= 26.3mA$$

For example 2:

if 00h=0x80, 01h=0x80, 10h=0x80, 11h=0x00, 20h=0x80, 21h=0x80, 30h=0x80, 31h=0x00, GCC=0xff. R_{EXT}=20kΩ (I_{OUT}=84mA),

$$I_{LED-1A} = \frac{0x80 \times 6}{256} \times (I_{OUT} / 2) \times \frac{1}{12.75}$$

$$= 9.87mA$$

Page 2 (PG2, 0x02): Auto Breath Mode Register

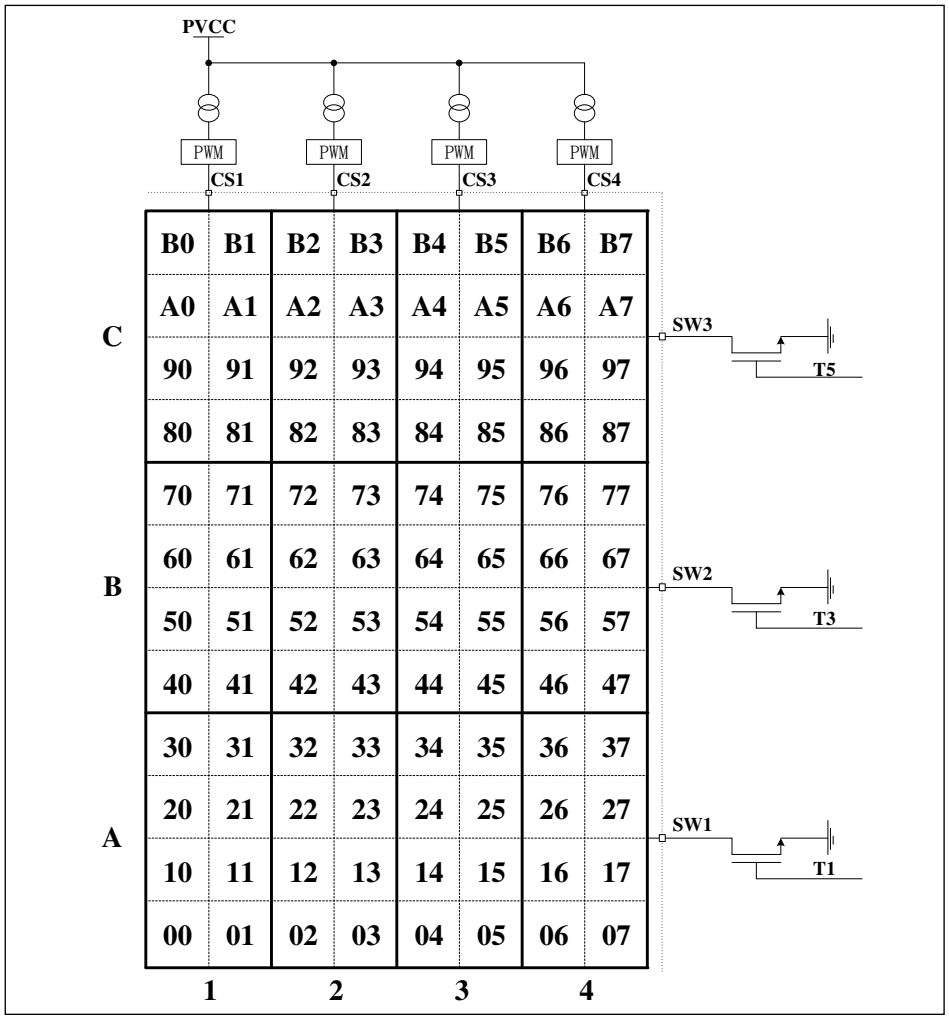


Figure 13 Auto Breath Mode Selection Register

Table 11 00h ~ B7h Auto Breath Mode Register

Bit	D7:D2	D1:D0
Name	-	ABMS
Default	-	00

The Auto Breath Mode Register sets operating mode of each dot, notice eight registers should be the same value when you selecting the mode.

For example, if 00h=0x01, 01h=0x01, 10h=0x01, 11h=0x01, 20h=0x01, 21h=0x01, 30h=0x01, 31h=0x01, then LED 1A work as ABM-1 mode

ABMS Auto Breath Mode Selection Bit
00 PWM control mode
01 Select Auto Breath Mode 1 (ABM-1)
10 Select Auto Breath Mode 2 (ABM-2)
11 Select Auto Breath Mode 3 (ABM-3)

Table 12 Page 3 (PG3, 0x03): Function Register

Register	Name	Function	R/W	Default
00h	Configuration Register	Configure the operation mode	W	0000 0000
01h	Global Current Control Register	Set the global current	W	
02h	Auto Breath Control Register 1 of ABM-1	Set fade in and hold time for breath function of ABM-1	W	
03h	Auto Breath Control Register 2 of ABM-1	Set the fade out and off time for breath function of ABM-1	W	
04h	Auto Breath Control Register 3 of ABM-1	Set loop characters of ABM-1	W	
05h	Auto Breath Control Register 4 of ABM-1	Set loop characters of ABM-1	W	
06h	Auto Breath Control Register 1 of ABM-2	Set fade in and hold time for breath function of ABM-2	W	
07h	Auto Breath Control Register 2 of ABM-2	Set the fade out and off time for breath function of ABM-2	W	
08h	Auto Breath Control Register 3 of ABM-2	Set loop characters of ABM-2	W	
09h	Auto Breath Control Register 4 of ABM-2	Set loop characters of ABM-2	W	
0Ah	Auto Breath Control Register 1 of ABM-3	Set fade in and hold time for breath function of ABM-3	W	
0Bh	Auto Breath Control Register 2 of ABM-3	Set the fade out and off time for breath function of ABM-3	W	
0Ch	Auto Breath Control Register 3 of ABM-3	Set loop characters of ABM-3	W	
0Dh	Auto Breath Control Register 4 of ABM-3	Set loop characters of ABM-3	W	
0Eh	Time Update Register	Update the setting of 02h ~ 0Dh registers	W	
0Fh	SWy Pull-Up Resistor Selection Register	Set the pull-up resistor for SWy	W	
10h	CSx Pull-Down Resistor Selection Register	Set the pull-down resistor for CSx	W	
11h	Reset Register	Reset all register to POR state	R	

Table 13 00h Configuration Register

Bit	D7:D6	D5:D3	D2	D1	D0
Name	SYNC	-	OSD	B_EN	SSD
Default	00	000	0	0	0

The Configuration Register sets operating mode of IS31FL3740.

When SYNC bits are set to “01”, the IS31FL3740 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

When OSD set high, open/short detection will be trigger once, the user could trigger OS detection again by set OSD from 0 to 1.

When B_EN enable, those dots select working in ABM-x mode will start to run the pre-established timing. If it is disabled, all dots work in PWM mode. Following Figure 19 to enable the Auto Breath Mode

When SSD is “0”, IS31FL3740 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SYNC Synchronize Configuration
00/11 High Impedance
01 Master
10 Slave

OSD Open/Short Detection Enable Bit
0 Disable open/short detection
1 Enable open/short detection

B_EN Auto Breath Enable
0 PWM Mode Enable
1 Auto Breath Mode Enable

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

Table 14 01h Global Current Control Register

Bit	D7:D0
Name	GCCx
Default	0000 0000

The Global Current Control Register modulates all CSx (x=1~4) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT} = \frac{840}{R_{EXT}} \times \frac{GCC}{256} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, R_{EXT} is the external resistor of R_EXT pin.

For example: if D7:D0=1011 0101,

$$I_{OUT} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times \frac{840}{R_{EXT}}$$

Table 15 02h, 06h, 0Ah Auto Breath Control Register 1 of ABM-x

Bit	D7:D5	D4:D1	D0
Name	T1	T2	-
Default	000	0000	0

Auto Breath Control Register 1 set the T1&T2 time in Auto Breath Mode.

T1 T1 Setting
000 0.21s
001 0.42s
010 0.84s
011 1.68s
100 3.36s
101 6.72s
110 13.44s
111 26.88s

T2 T2 Setting
0000 0s
0001 0.21s
0010 0.42s
0011 0.84s
0100 1.68s
0101 3.36s
0110 6.72s
0111 13.44s
1000 26.88s
Others Unavailable

Table 16 03h, 07h, 0Bh Auto Breath Control Register 2 of ABM-x

Bit	D7:D5	D4:D1	D0
Name	T3	T4	-
Default	000	0000	0

Auto Breath Control Register 2 set the T3&T4 time in Auto Breath Mode.

T3 T3 Setting
000 0.21s
001 0.42s
010 0.84s
011 1.68s
100 3.36s
101 6.72s
110 13.44s
111 26.88s

T4 T4 Setting
0000 0s
0001 0.21s
0010 0.42s
0011 0.84s
0100 1.68s
0101 3.36s
0110 6.72s
0111 13.44s
1000 26.88s
1001 53.76s
1010 107.52s
Others Unavailable

Table 17 04h, 08h, 0Ch Auto Breath Control Register 3 of ABM-x

Bit	D7:D6	D5:D4	D3:D0
Name	LE	LB	LTA
Default	00	00	0000

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

For the counting of breathing times, do follow Figure 19 to enable the Auto Breath Mode.

If the loop start from T4,

T4->T1->T2->T3(1)->T4->T1->T2->T3(2)->T4->T1->...and so on.

If the loop not start from T4,

Tx->T3(1) ->T4->T1->T2->T3(2)->T4-> T1->...and so on.

If the loop ends at off state(End of T3), the LED will be off state at last. If the loop ends at on state(End of T1), the LED will run an extra T4&T1, which are not included in loop.

LB Loop Beginning Time
00 Loop begin from T1
01 Loop begin from T2
10 Loop begin from T3
11 Loop begin from T4

LE Loop End Time
00 Loop end at off state (End of T3)
01 Loop end at on state (End of T1)
Others Unavailable

LTA 8-11 Bits Of Loop Times
0000 Endless loop
0001 1
0010 2
… …
1111 15

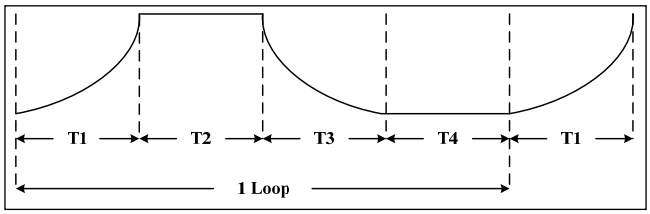


Figure 14 Auto Breathing Function

Table 18 05h, 09h, 0Dh Auto Breath Control Register 4 of ABM-x

Bit	D7:D0
Name	LTB
Default	0000 0000

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

LTB 0-7 Bits Of Loop Times
0000 0000 Endless loop
0000 0001 1
0000 0010 2
… …
1111 1111 255

0Eh Time Update Register (02h~0Dh)

The data sent to the time registers (02h~0Dh) will be stored in temporary registers. A write operation of "0000 0000" data to the Time Update Register is required to update the registers (02h~0Dh). Please follow Figure 19 to enable the Auto Breath Mode and update the time parameters.

Table 19 0Fh SWy Pull-Up Resistor Selection Register

Bit	D7:D3	D2:D0
Name	-	PUR
Default	00000	000

Set pull-up resistor for SWy.

PUR SWy Pull-up Resistor Selection Bit
000 No pull-up resistor
001 0.5kΩ
010 1.0kΩ
011 2.0kΩ
100 4.0kΩ
101 8.0kΩ
110 16kΩ
111 32kΩ

Table 20 10h CSx Pull-Down Resistor Selection Register

Bit	D7:D3	D2:D0
Name	-	PDR
Default	00000	000

Set the pull-down resistor for CSx.

PDR	CSx Pull-down Resistor Selection Bit
000	No pull-down resistor
001	0.5kΩ
010	1.0kΩ
011	2.0kΩ
100	4.0kΩ
101	8.0kΩ
110	16kΩ
111	32kΩ

11h Reset Register

Once user read the Reset Register, IS31FL3740 will reset all the IS31FL3740registers to their default value. On initial power-up, the IS31FL3740 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

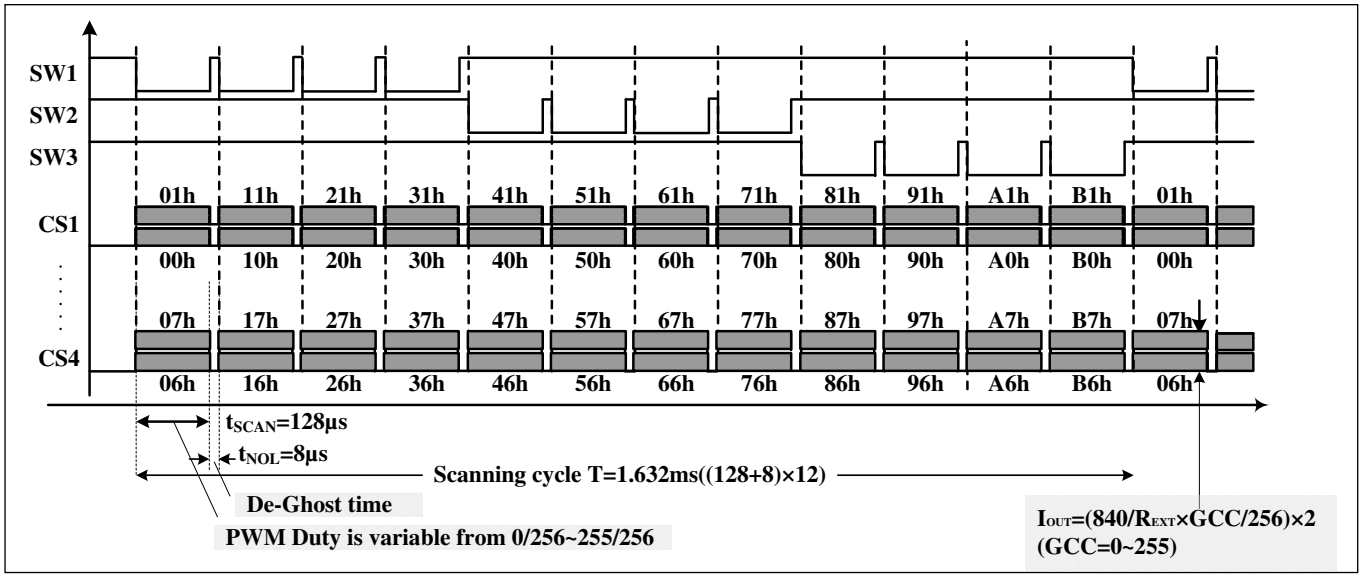


Figure 15 Scanning Timing

SCANING TIMING

As shown in Figure 15, the SW1~SW3 is turned on by serial, LED is driven 12 by 12 within the SWy (x=1~3) on time (SWy, y=1~3) is sink and pull low when LED on, including the non-overlap blanking time during scan, the duty cycle of SWy (active low, y=1~3) is:

$$Duty=\frac{128\mu s}{(128\mu s+8\mu s)}\times\frac{1}{3}\times\frac{1}{4}=\frac{1}{12.75} \quad (2)$$

Where 128μs is t_{SCAN}, the period of scanning and 8μs is t_{NOL}, the non-overlap time.

EXTERNAL RESISTOR (R_{EXT})

The output current for each CSx can be can be set by a single external resistor, R_{EXT}, as described in Formula (3).

$$I_{OUT}=\frac{840}{R_{EXT}}\times\frac{GCC}{256}\times 2 \quad (3)$$

GCC is Global Current Control Register (PG3, 01h) data showing in Table 14.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 1024 steps by PWM Register, as described in Formula (1).

$$I_{LED}=\frac{\sum PWM}{256}\times(I_{OUT}/2)\times Duty \quad (1)$$

Where PWM is PWM Registers (PG1, 00h~BFh) data showing in Table 10.

For example, in Figure 1,

if 00h=0xff, 01h=0xff, 10h=0xff, 11h=0xff, 20h=0xff, 21h=0xff, 30h=0xff, 31h=0xff, GCC=0xff. R_{EXT}=20kΩ (I_{OUT}=84mA),

$$I_{LED-1A}=\frac{0xff\times 8}{256}\times(I_{OUT}/2)\times\frac{1}{12.75}$$
$$=26.3mA$$

For example 2: in Figure 1,

if 00h=0x80, 01h=0x80, 10h=0x80, 11h=0x00, 20h=0x80, 21h=0x80, 30h=0x80, 31h=0x00, GCC=0xff. R_{EXT}=20kΩ (I_{OUT}=84mA),

$$I_{LED-1A}=\frac{0x80\times 6}{256}\times(I_{OUT}/2)\times\frac{1}{12.75}$$
$$=9.87mA$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

LED AVERAGE CURRENT (I_{LED})

As described in Formula (1), the LED average current (I_{LED}) is effected by 3 factors:

1. R_{EXT}, resistor which is connected R_EXT pin and GND. R_{EXT} sets the current of all CSx(x=1~4) based on Formula (3).

2. Global Current Control Register (PG3, 01h). This register adjusts all CSx (x=1~4) output currents by 256 steps as shown in Formula (3).

3. PWM Registers (PG1, 00h~BFh), every LED has an own PWM register. PWM Registers adjust