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IS34ML01G081
IS35ML01G081

1Gb SLC-1b ECC
3.3V X8 NAND FLASH MEMORY STANDARD NAND INTERFACE

1Gb (x8) 3.3V NAND FLASH MEMORY with 1b ECC

FEATURES

- **Flexible & Efficient Memory Architecture**
  - Organization: 128Mb x8
    - Memory Cell Array: (128M + 4M) x 8bit
    - Data Register: (2K + 64) x 8bit
    - Page Size: (2K + 64) Byte
    - Block Erase: (128K + 4K) Byte
    - Memory Cell: 1bit/Memory Cell

- **Highest performance**
  - Read Performance
    - Random Read: 25us (Max.)
    - Serial Access: 25ns (Max.)
  - Write Performance
    - Program time: 400us - typical
    - Block Erase time: 3ms – typical

- **Low Power with Wide Temp. Ranges**
  - Single 3.3V (2.7V to 3.6V) Voltage Supply
  - 15 mA Active Read Current
  - 10 µA Standby Current
  - Temp Grades:
    - Industrial: -40°C to +85°C
    - Extended: -40°C to +105°C
    - Automotive, A1: -40°C to +85°C
    - Automotive, A2: -40°C to +105°C

- **Reliable CMOS Floating Gate Technology**
  - ECC Requirement: X8 - **1bit/512Byte**
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years

- **Efficient Read and Program modes**
  - Command/Address/Data Multiplexed I/O Interface
  - Command Register Operation
  - Automatic Page 0 Read at Power-Up Option
    - Boot from NAND support
    - Automatic Memory Download
  - NOP: 4 cycles
  - Cache Program Operation for High Performance Program
  - Cache Read Operation
  - Copy-Back Operation
  - EDO mode
  - OTO Operation
  - Bad-Block-Protect

- **Advanced Security Protection**
  - Hardware Data Protection
    - Program/Erase Lockout during Power Transitions

- **Industry Standard Pin-out & Packages**
  - T =48-pin TSOP1
  - B =63-ball VFBGA

GENERAL DESCRIPTION

The IS34/35ML1G081 is a 128Mx8bit with spare 4Mx8bit capacity. The device is offered in 3.3V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 1,024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 2,112-Byte page in typical 400us and an erase operation can be performed in typical 3ms on a 128K-Byte for X8 device block.

Data in the page mode can be read out at 25ns cycle time per Byte. The I/O pins serve as the ports for address and command inputs as well as data input/output.

The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array.

This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

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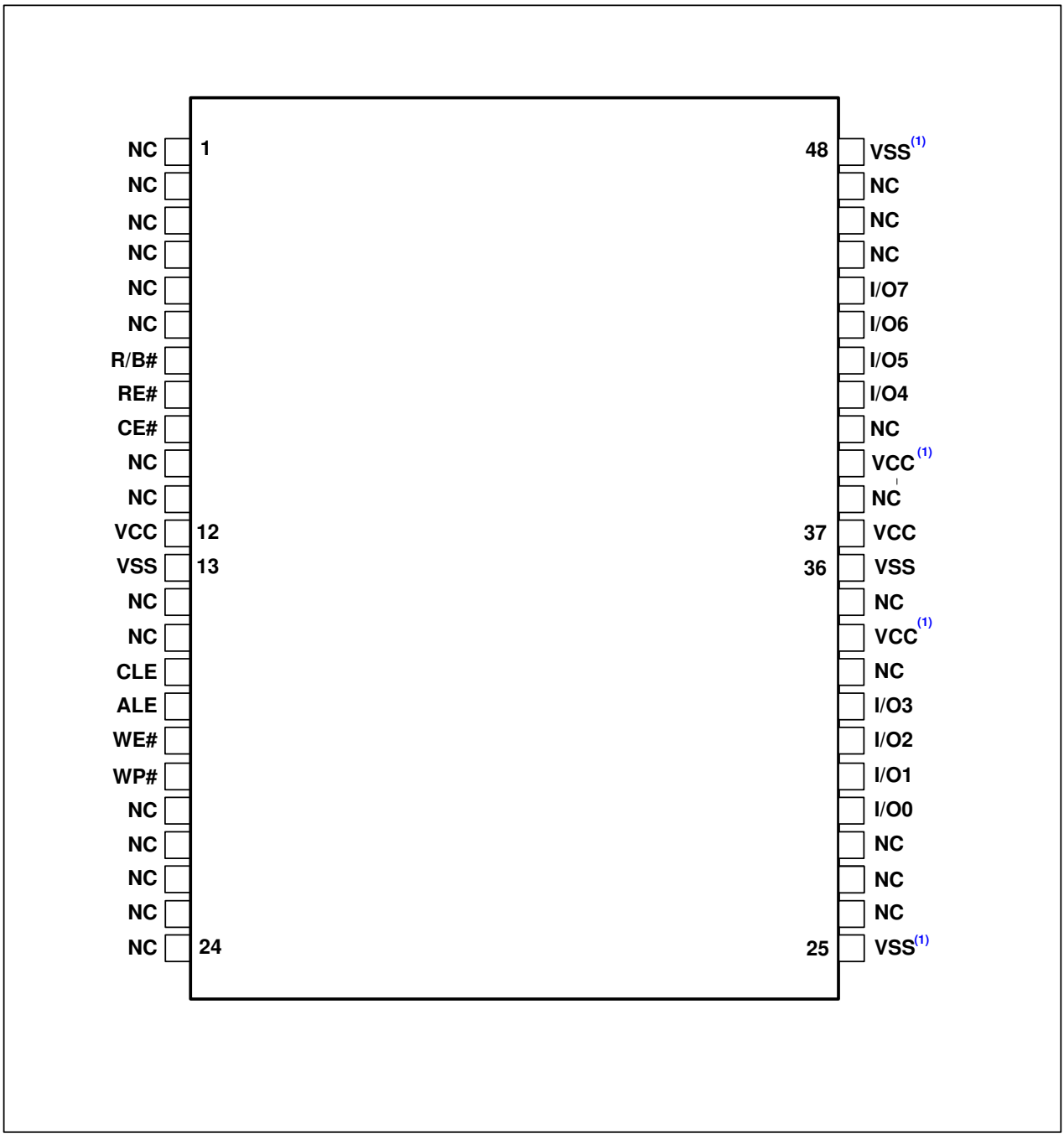
1. PIN CONFIGURATION

48-pin TSOP (Type I)

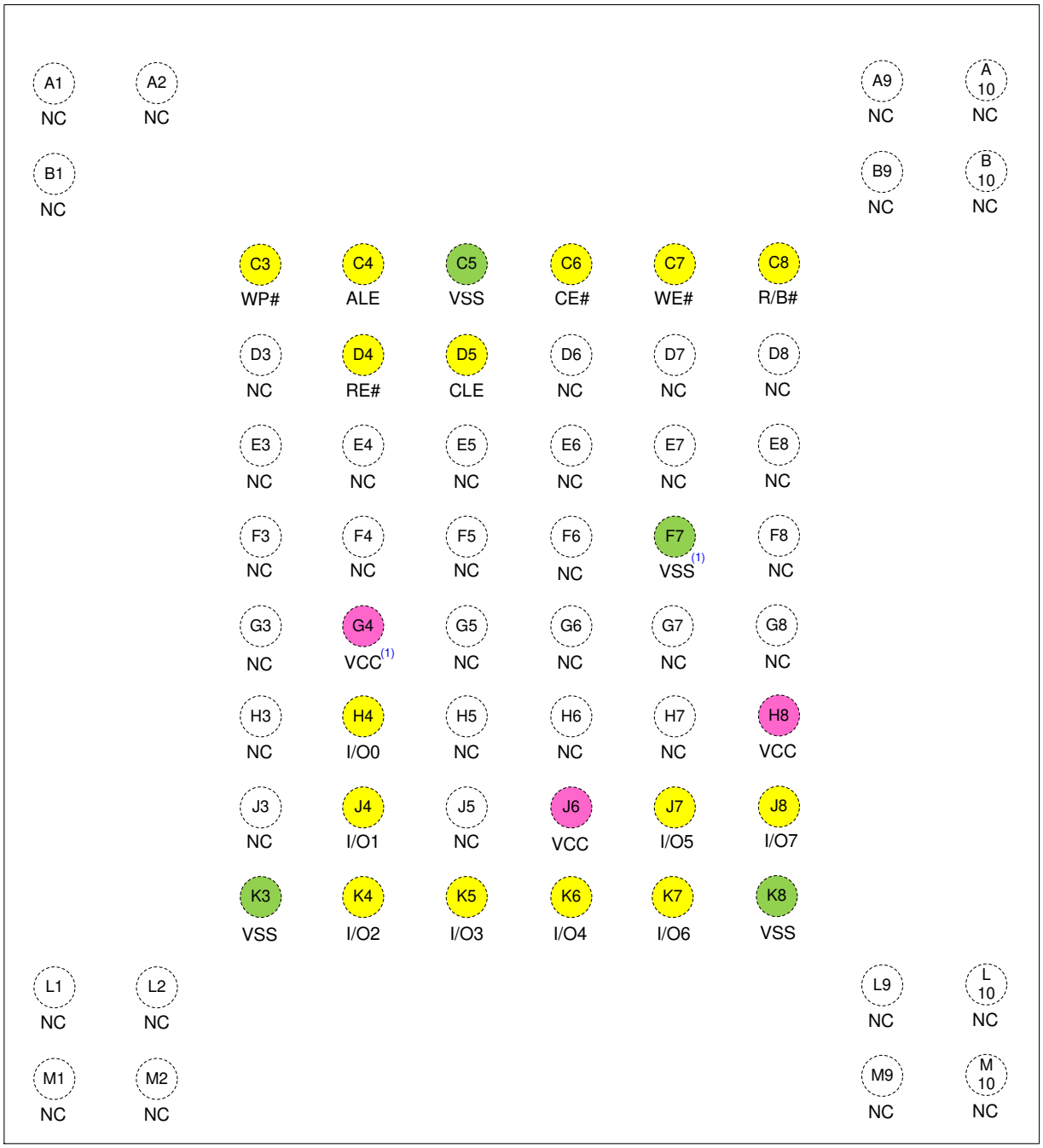


Note:

1. These pins might not be bonded in the package; however it is recommended to connect these pins to the designated external sources for ONFI compatibility.

63-ball VFBGA

Balls Down, Top View



Note:

1. These pins might not be bonded in the package; however it is recommended to connect these pins to the designated external sources for ONFI compatibility.

2. PIN DESCRIPTIONS

Pin Name	Pin Function
I/O0 ~ I/O7 (X8)	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
N.C.	**NO CONNECTION** Lead is not internally connected.

3. BLOCK DIAGRAM

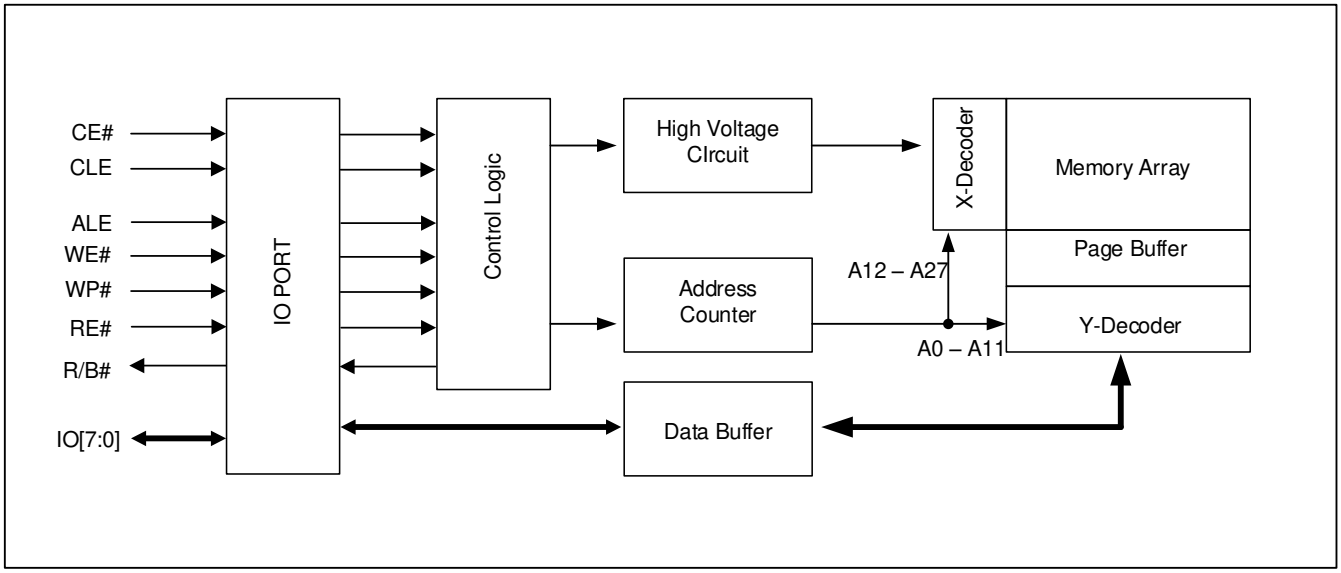


Figure 3.1 Functional Block Diagram

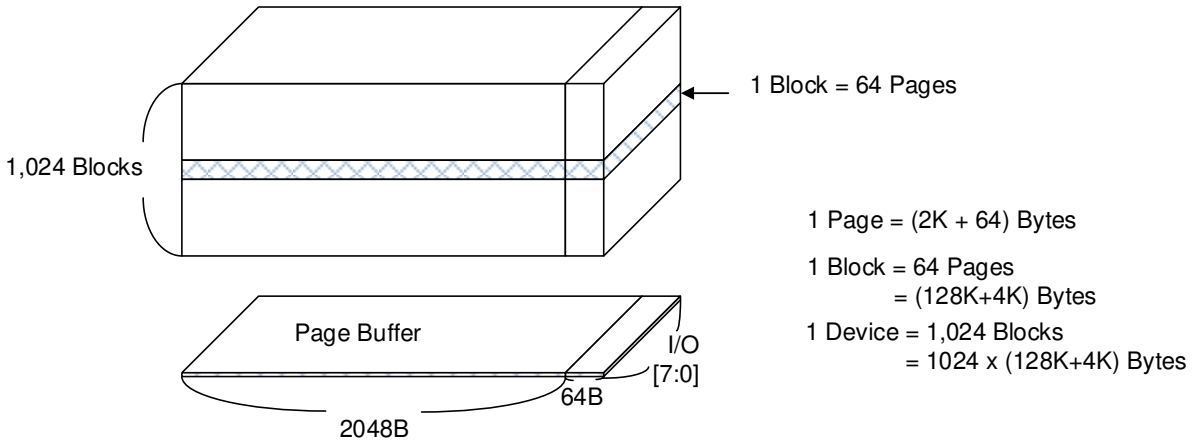


Figure 3.2 Array Organization

Table 3.1 ARRAY Address (x8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_5	A_7	Column Address
2nd cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	Column Address
3rd cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	Row Address
4th cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	Row Address

Notes:
1. Column Address: Starting Address of the Register.
2. *L must be set to “Low”.
3. The device ignores any additional input of address cycles than required.

4. OPERATION DESCRIPTION

The IS34/35ML01G081 is a 1Gbit memory organized as 128K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1,024 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the IS34/35ML01G081.

The device has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Table 4.1 Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start For Last Page Cache Read	3Fh	-	

Note:
1. Random Data Input/Output can be executed in a page.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.6V to +4.6V
All I/O Voltage with Respect to Ground		-0.6V to V_{CC} + 0.3V(< 4.6V)
V_{CC}		-0.6V to +4.6V
Short Circuit Current		5mA
Electrostatic Discharge Voltage (Human Body Model)(2)		-2000V to +2000V

Notes:
1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

5.2 RECOMMENDED OPERATING CONDITIONS

Part Number	IS34/35ML01G081
Operating Temperature (Industrial Grade)	-40°C to 85°C
Operating Temperature (Extended Grade)	-40°C to 105°C
Operating Temperature (Automotive Grade A1)	-40°C to 85°C
Operating Temperature (Automotive Grade A2)	-40°C to 105°C
V_{CC} Power Supply	2.7V (VMIN) – 3.6V (VMAX); 3.3V (Typ)

5.3 DC CHARACTERISTICS

(Under operating range)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	tRC=tRC$_{MIN}$, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15		
	Erase	ICC3	-	-	15		
Stand-by Current (TTL)		ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)		ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)	-	-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)	-	-	+/-10	
Input High Voltage		VIH (1)		0.8xVCC	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-400 uA	2.4	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

Notes:
1. VIL can undershoot to -2V and VIH can overshoot to VCC + 2V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

5.4 VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
IS34/35ML01G081	NVB	1,004	-	1,024	Block

Notes:
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

5.5 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 50pF		pF
TR,TF	Input Rise and Fall Times	-	5	ns
VIN	Input Pulse Voltages	0V to V_{CC}		V
VREFI	Input Timing Reference Voltages	$0.5V_{CC}$		V
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		V

Note:
1. Refer to 8.10 Ready/Busy#, R/B#'s Busy to Ready time is decided by pull up register (Rp) tied to R/B# pin.

5.6 AC PIN CAPACITANCE (TA = 25°C, VCC=3.3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	-	-	8	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	-	8	pF

Note:
1. These parameters are characterized and not 100% tested.

5.7 MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (4 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (4 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

Notes:
1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

5.8 ROGRAM/ERASE PERFORMANCNE

(Industrial: T_A=-40 to 85℃, Automotive, A1: T_A=-40 to 85℃, Vcc=2.7V ~ 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	400	950	us
Dummy Busy Time for Cache Operation	tCBSY	-	3	950	us
Number of Partial Program Cycles in the Same Page	Nop	-	-	4	cycle
Block Erase Time	tBERS	-	2	10	ms

Notes:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25℃ temperature.
2. **tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.**
3. tCBSY max.time depends on timing between internal program completion and data-in.

5.9 AC CHARACTERISTICS FOR ADDRESS/ COMMAND/DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS(1)	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE# Setup Time	tCS(1)	20	-	ns
CE# Hold Time	tCH	5	-	ns
WE# Pulse Width	tWP	12	-	ns
ALE Setup Time	tALS(1)	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS(1)	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE# High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL(2)	70(2)	-	ns

Note:
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. tADL is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

5.10 AC CHARACTERISTICS FOR OPERATION

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	25	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
RE# Pulse Width		tRP	12	-	ns
WE# High to Busy		tWB	-	100	ns
WP# Low to WE# Low (disable mode)		tWW	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		tRC	25	-	ns
RE# Access Time		tREA	-	20	ns
CE# Access Time		tCEA	-	25	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
CE# High to ALE or CLE Don't care		tCSD	0		ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5		ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	10	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Device Resetting Time during…	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5 (1)	us
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR	-	30	us

Note: If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

6. TIMING DIAGRAMS FOR OPERATION

6.1 COMMAND LATCH CYCLE

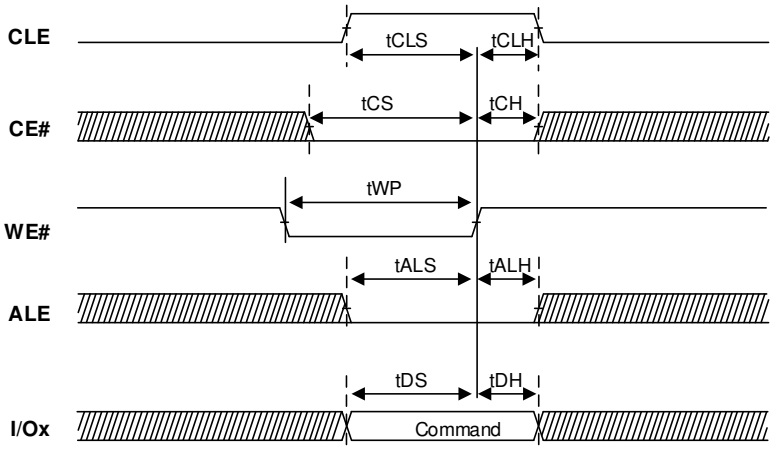


Figure 6.1 Command Latch Cycle

6.2 ADDRESS LATCH CYCLE

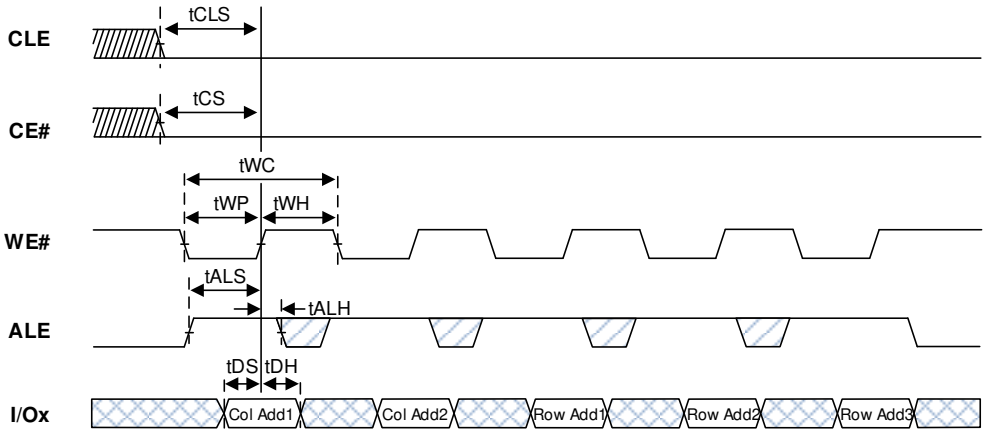


Figure 6.2 Address Latch Cycle

6.3 INPUT DATA LATCH CYCLE

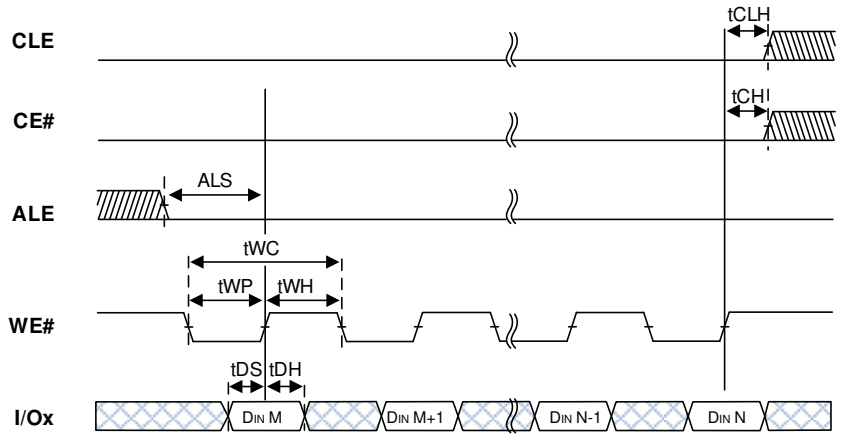
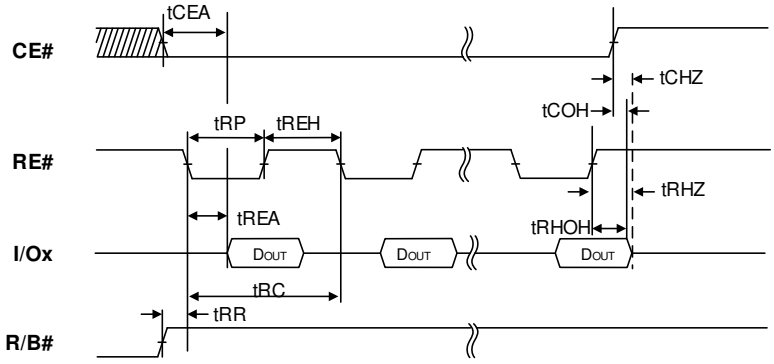


Figure 6.3 Input Data Latch Cycle

6.4 SERIAL ACCESS CYCLE AFTER READ (CLE=L, WE#=H, ALE=L)

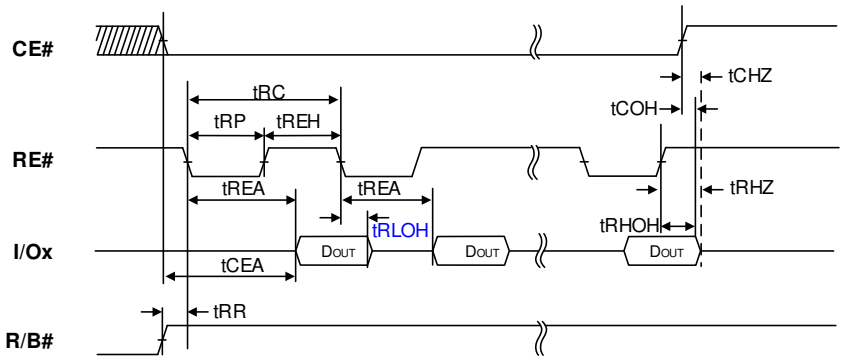


Note:

1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 6.4 Serial Access Cycle after Read

6.5 SERIAL ACCESS CYCLE AFTER READ (EDO TYPE CLE=L, WE#=H, ALE=L)



Notes:
1. Transition is measured at +/-200mV from steady state voltage with load. This parameter is sample and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33MHZ. tRHOH starts to be valid when frequency is lower than 33MHZ.

Figure 6.5 Serial Access Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)

6.6 STATUS READ CYCLE

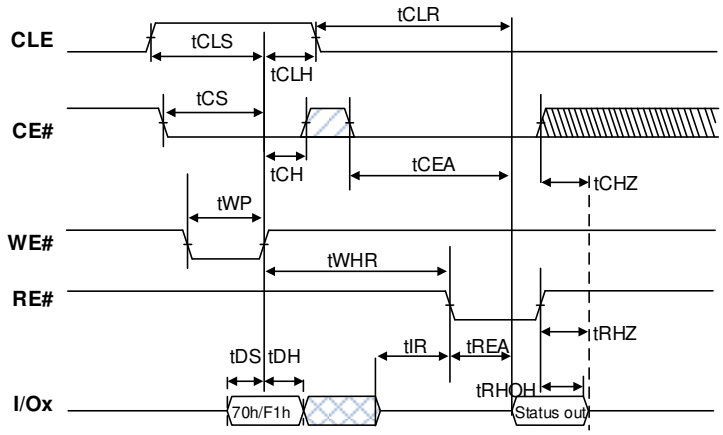


Figure 6.6 Status Read Cycle

6.7 READ OPERATION

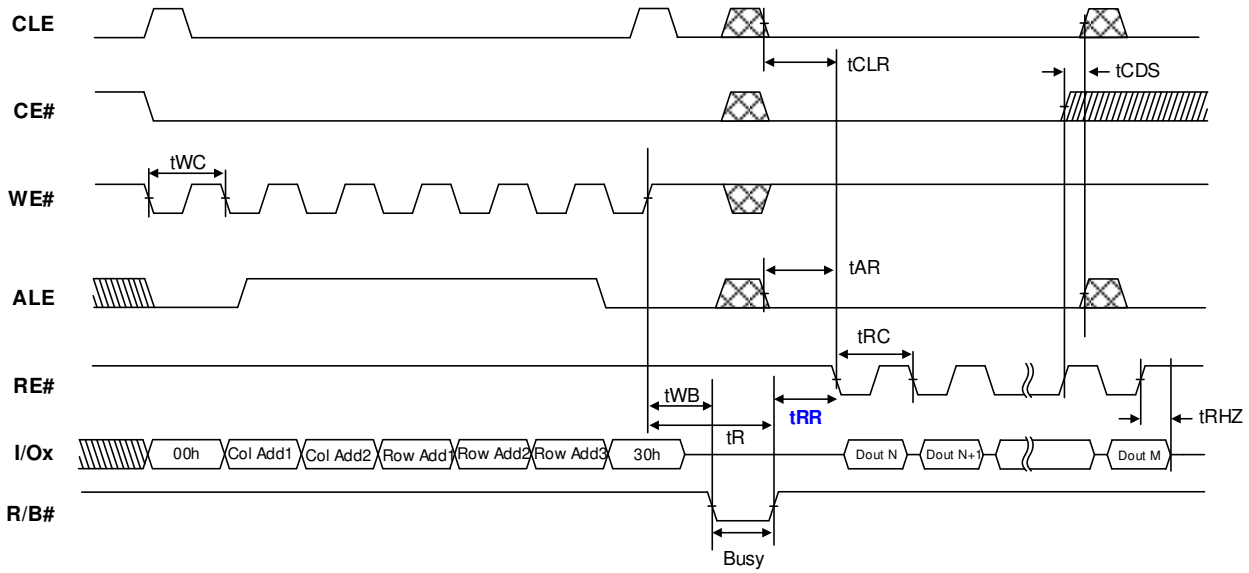


Figure 6.7 Read Operation (One Page)

6.8 READ OPERATION (INTERCEPTED BY CE#)

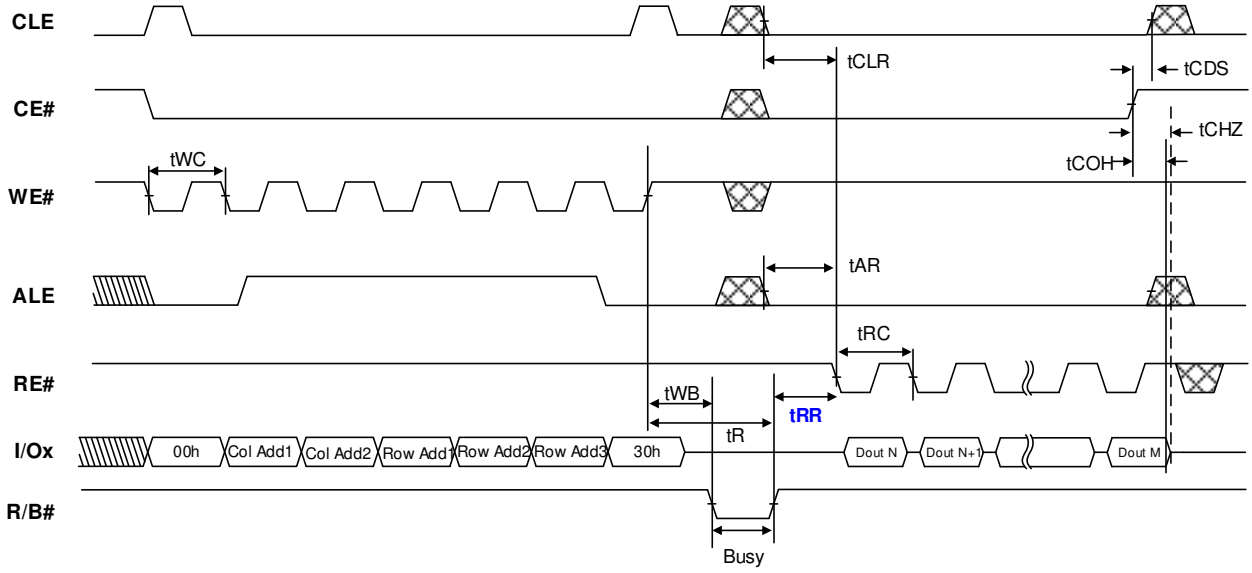


Figure 6.8 Read Operation (Intercepted by CE#)

6.9 RANDOM DATA OUTPUT IN A PAGE

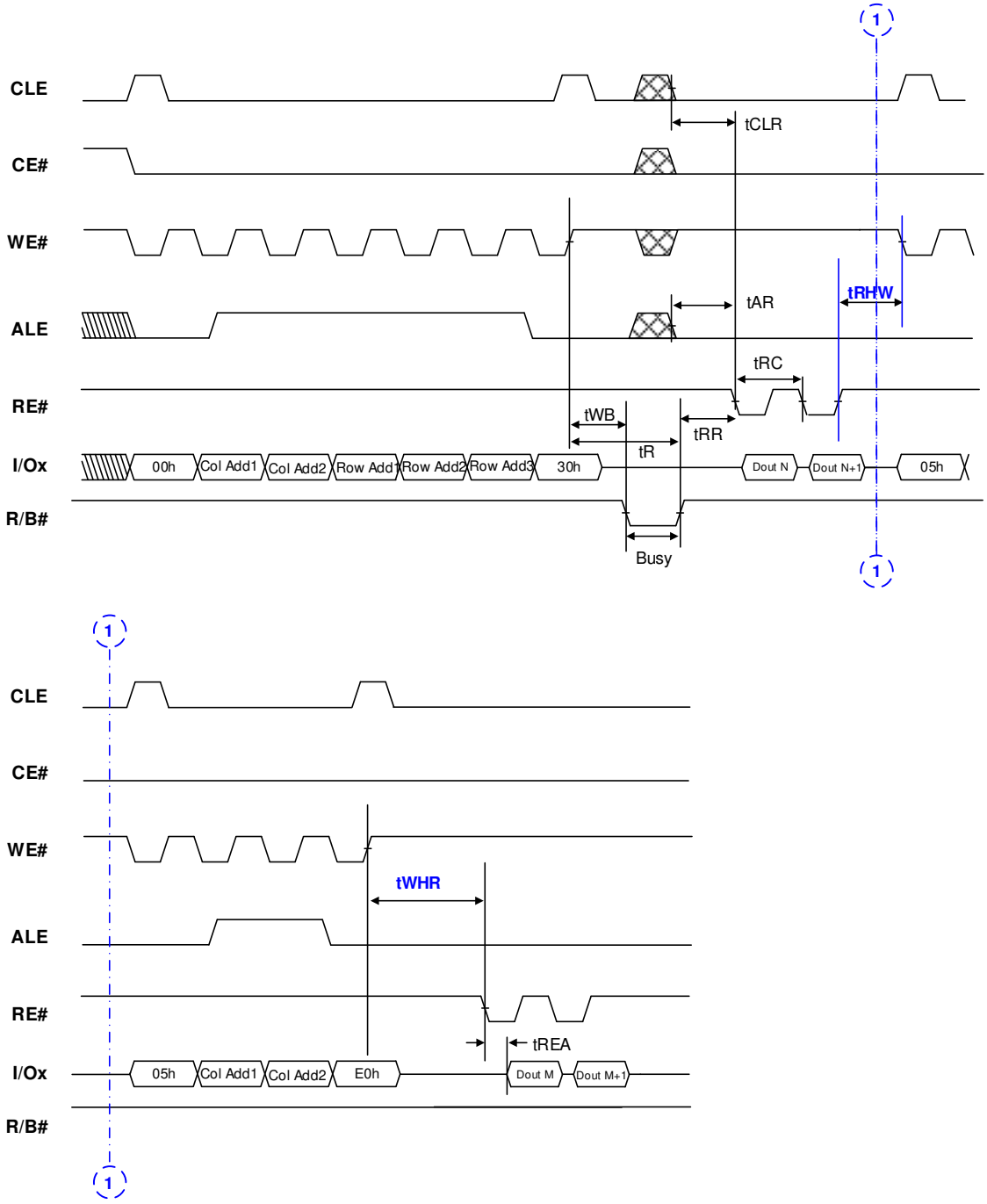
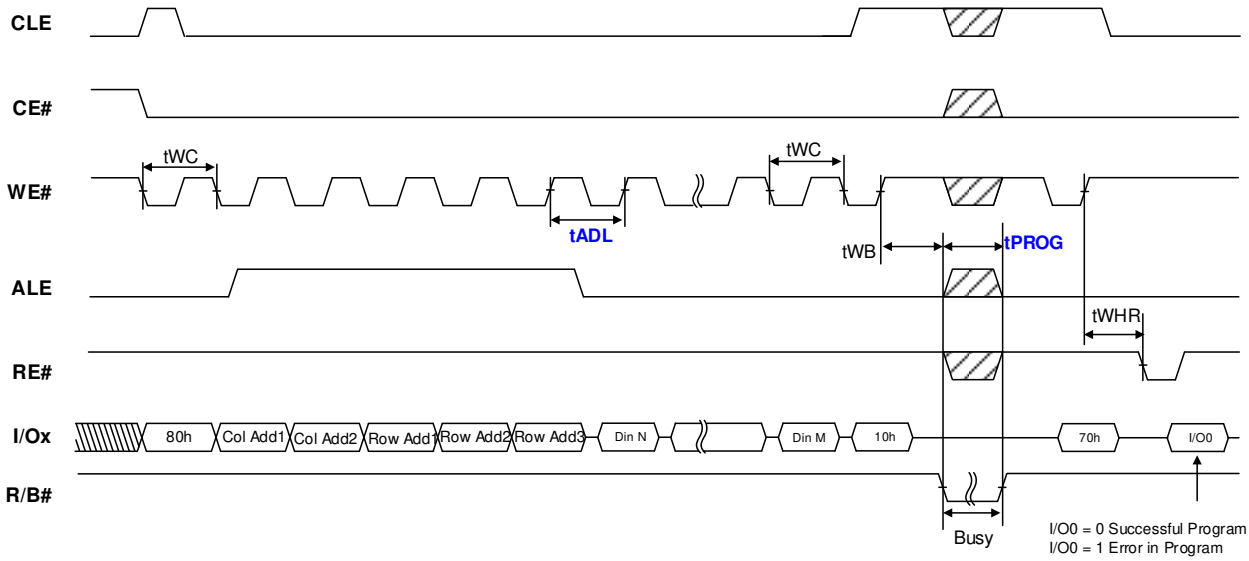


Figure 6.9 Random Data Output in a Page

6.10 PAGE PROGRAM OPERATION

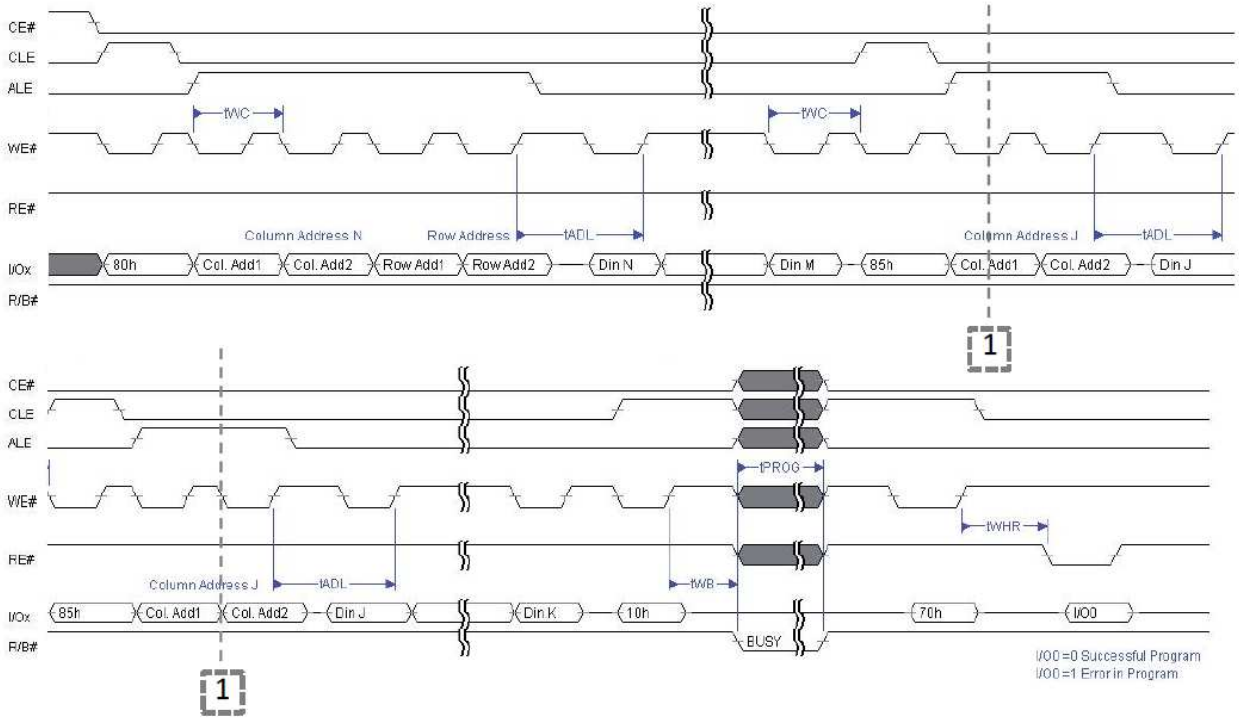


Note:

1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Figure 6.10 Page Program Operation

6.11 PAGE PROGRAM OPERATION WITH RANDOM DATA INPUT



Note: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

Figure 6.11 Page Program Operation with Random Data Input

6.12 COPY-BACK OPERATION WITH RANDOM DATA INPUT

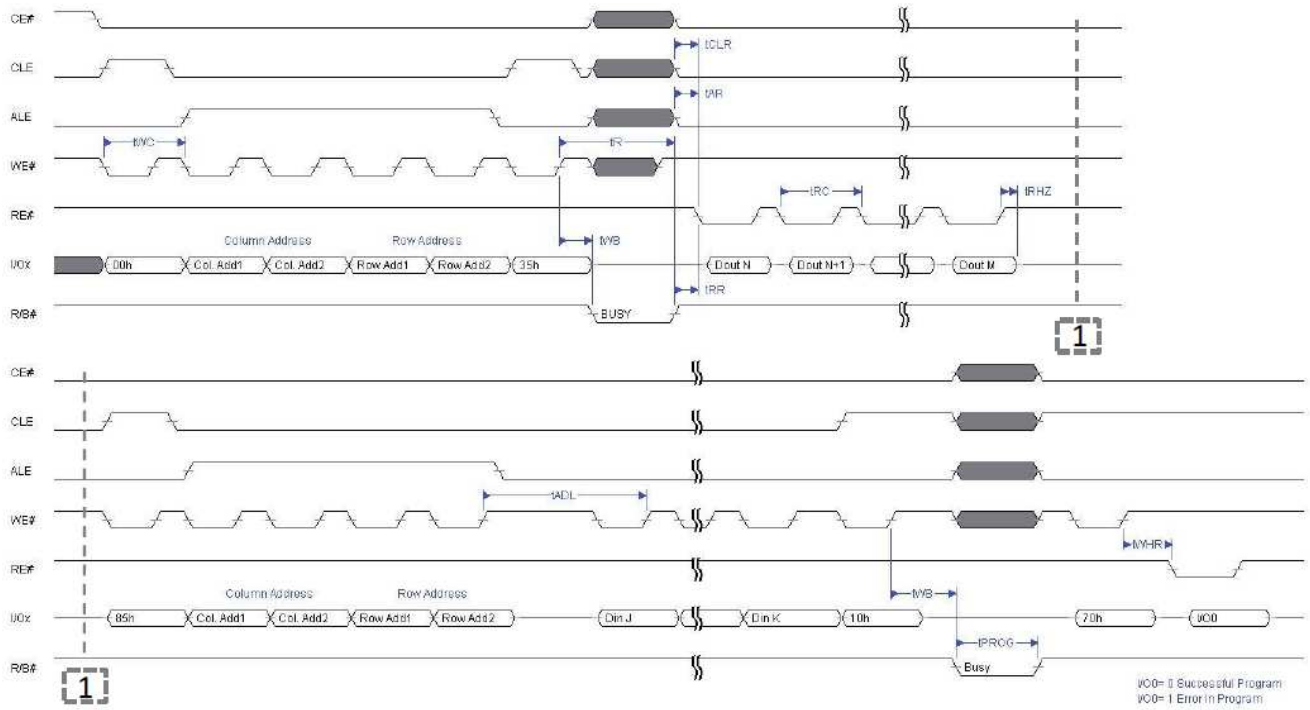


Figure 6.12 Copy-Back Operation with Random Data Input