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IS37SML01G1
IS38SML01G1

1Gb SLC-1b ECC
3.3V SERIAL NAND FLASH MEMORY WITH 104MHZ MULTI I/O SPI INTERFACE

PRELIMINARY DATA SHEET

1Gb 3.3V SPI-NAND FLASH MEMORY WITH 104MHZ MULTI I/O SPI INTERFACE with 1b ECC

PRELIMINARY INFORMATION

FEATURES

- **Flexible & Efficient Memory Architecture**
  - Organization:
    - Memory Cell Array: (128M + 4M) x 8bit
    - Data Register: (2K + 64) x 8bit
    - Page Size: (2K + 64) Byte
    - Block Erase: (128K + 4K) Byte
    - Memory Cell: 1bit/Memory Cell

- **Highest performance**
  - Frequency : 104MHz
  - Internal ECC Implementation: 1-bit ECC
  - Read Performance
    - Read from Cell to Register with Internal ECC: 100us
  - Write Performance
    - Program time: 400us - typical
    - Block Erase time: 4ms – typical

- **Low Power with Wide Temp. Ranges**
  - Single 3.3V (2.7V to 3.6V) Voltage Supply
  - 10 mA Active Read Current
  - 8 µA Standby Current
  - Temp Grades:
    - Industrial: -40°C to +85°C
    - Extended: -40°C to +105°C
    - Automotive, A1: -40°C to +85°C
    - Automotive, A2: -40°C to +105°C

- **Reliable CMOS Floating Gate Technology**
  - Internal ECC Requirement: **1bit/512Byte**
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years

- **Efficient Read and Program modes**
  - Support SPI-Mode 0 and SPI-Mode 3
  - Bus Width: x1, x2[1], x4
  - Command Register Operation
  - NOP: 4 cycles
  - OTP Operation
  - Bad-Block-Protect
  - Boot Read

- **Advanced Security Protection**
  - Hardware Data Protection
    - Program/Erase Lockout during Power Transitions

- **Industry Standard Pin-out & Packages**
  - M =16-pin SOIC 300mil
  - L = 8-contact WSON 8x6mm

Note:

1. **X2 Program Operation is not defined.**

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non- volatile memory storage solution in systems where pin count must be kept to a minimum.
The ISSI IS37/38SML01G1 is a 1Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structure of 32 series connected Flash cells. Each page consists 2112-Byte and is further divided into a 2048-Byte data storage area with a separate 64-Byte spare area. The 64-Byte area is typically used for memory and error management.

The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The pins serve as the ports for signals. The device has six signal lines plus Vcc and ground (GND, Vss). The signal lines are SCK (serial clock), SI (command and data input), SO (response and data output), and control signals CS#, HOLD#, WP#.

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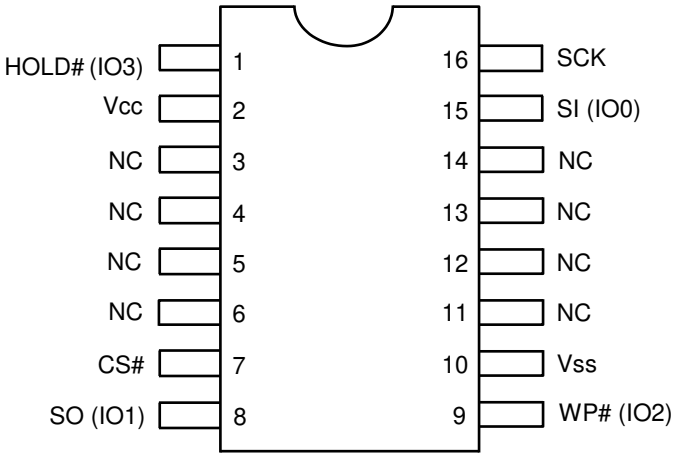
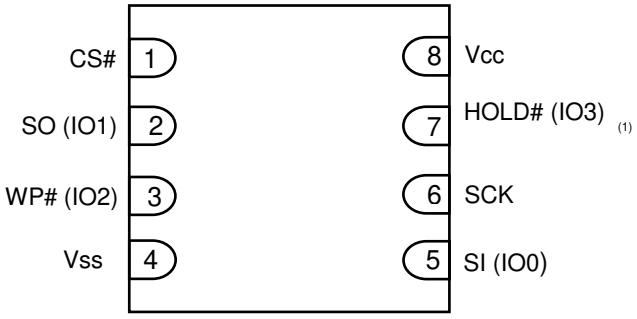
1. PIN CONFIGURATION



16-pin SOIC 300mil



8-contact WSON 8x6mm

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CS#	INPUT	**Chip Select:** The device is activated/deactivated as CS# is driven LOW (1) /HIGH (2). After power-on, the device requires a falling edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
HOLD# / IO3	INPUT/ OUTPUT	**HOLD#/IO3:** Hold pauses any serial communication with the device without deselecting it.(3) When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation.
WP# / IO2	INPUT/ OUTPUT	**Write Protect#/IO2:** WP# is driven LOW to prevent overwriting the block-lock bits (BP0,BP1 and BP2). If block register write disable (BRWD) bit is set. (4) WP# must not be driven during x4 operation.
SCK	INPUT	**Serial Clock:** SCK provides serial interfacing timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data out SO) is triggered after the falling edge of SCK. The clock is valid only when the device is active. (5)
SI / IO_0	INPUT/OUTPUT	**Serial Data Input/IO0:** SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation.
SO / IO_1	INPUT/OUTPUT	**Serial Data Output/IO1:** SO transfers data serially out of the device on the falling edge of SCK.. K. SO must not be driven during x2 or x4 PROGRAM operation.
Vcc(6)	POWER	Vcc is the power supply for device.
Vss(6)	GROUND	Ground
NC	Unused	No Connection Not internally connected.

Notes:

1. **CS# places the device in active power mode.**
2. **CS# deselects the device and places SO at high impedance.**
3. **It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.**
4. **If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can't be altered.**
5. **SI and SO can be triggered only when the clock is valid.**
6. **Connect all Vcc and Vss pins of each device to common power supply outputs. Do not leave Vcc or Vss disconnected.**

3. BLOCK DIAGRAM

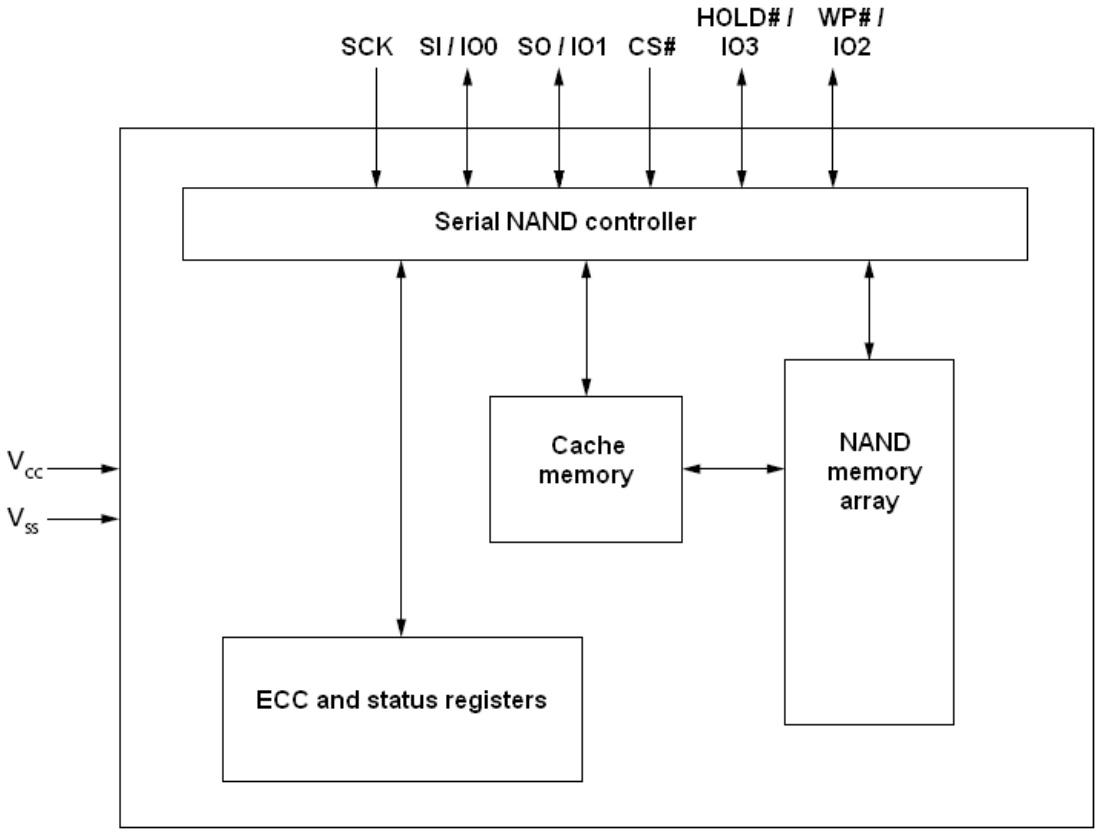


Figure 3.1 Functional Block Diagram

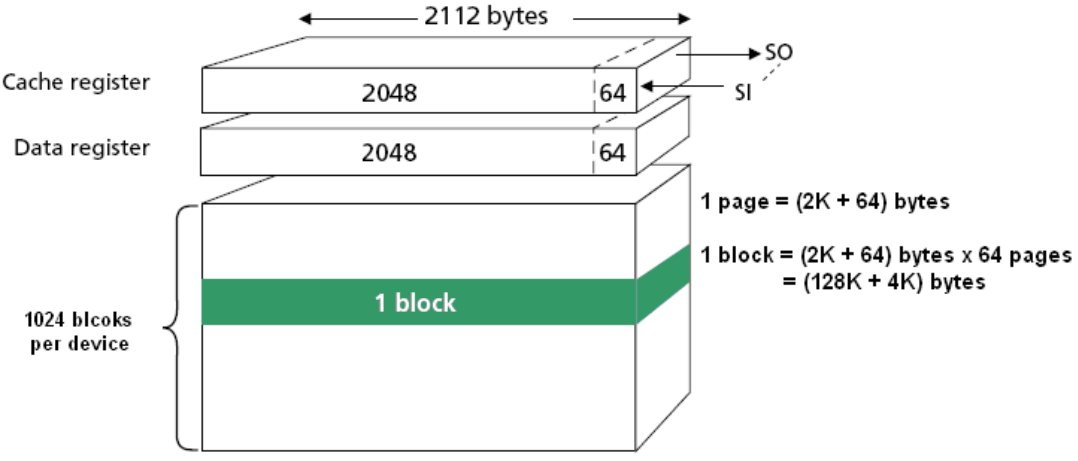


Figure 3.2 Array Organization

4. Command Set

Table 4.1 Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes
Block Erase	D8h	3	0	0
Get Feature(1)	0Fh	1	0	1
Set Feature	1Fh	1	0	1
Write Disable	04h	0	0	0
Write Enable	06h	0	0	0
Program Load	02h	2	0	1 to 2112
Program Load x4(2)	32h	2	0	1 to 2112
Program Load Random Data	84h	2	0	1 to 2112
Program Load Random Data x4(2)	34h	2	0	1 to 2112
Program Execute	10h	3	0	0
Page Read	13h	3	0	0
Read from Cache	03h, 0Bh	2	1	1 to 2112
Read from Cache x2	3Bh	2	1	1 to 2112
Read from Cache x4(2)	6Bh	2	1	1 to 2112
Read ID(3)	9Fh	1	0	2
RESET	FFh	0	0	0

Notes:
1. **Refer to Feature Register.**
2. **Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.**
3. **Address is 00h to get JEDEC ID.**

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.6V to +4.6V
All I/O Voltage with Respect to Ground		-0.6V to V_{CC} + 0.3V(< 4.6V)
V_{CC}		-0.6V to +4.6V
Short Circuit Current		5mA
Electrostatic Discharge Voltage (Human Body Model)(2)		-2000V to +2000V

Notes:
1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

5.2 RECOMMENDED OPERATING CONDITIONS

Part Number	IS37/38SML01G1
Operating Temperature (Industrial Grade)	-40°C to 85°C
Operating Temperature (Extended Grade)	-40°C to 105°C
Operating Temperature (Automotive Grade A1)	-40°C to 85°C
Operating Temperature (Automotive Grade A2)	-40°C to 105°C
V_{CC} Power Supply	2.7V (VMIN) – 3.6V (VMAX); 3.3V (Typ)

5.3 DC CHARACTERISTICS

(Under operating range)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	fC=104MHz, CS#=VIL, IOUT=0mA	-	16	20	mA
	Program	ICC2	-	-	16		
	Erase	ICC3	-	-	16		
Stand-by Current (TTL)		ISB1	CS#=VIH, WP#=0V/Vcc	-	-	1	
Stand-by Current (CMOS)		ISB2	CS#=VCC-0.2, WP#=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)	-	-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)	-	-	+/-10	
Input High Voltage		VIH (1)		0.7xVCC	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-20 uA	0.7xVCC	-	-	
Output Low Voltage Level		VOL	IOL=1mA	-	-	0.15xVCC	

Notes:
1. VIL can undershoot to - 2V and VIH can overshoot to Vcc + 2V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

5.4 VALID BLOCK

Description	Requirement
Minimum / Maximum number of Valid block number	1004 / 1024
Bad Block Mark	Non FFh
Mark Location	Column 2048 of page 0 and page 1

Notes:
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

5.5 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 15pF		pF
TR,TF	Input Rise and Fall Times	-	2.4	ns
VIN	Input Pulse Voltages	0.2Vcc to 0.8 V_{CC}		V

5.6 AC PIN CAPACITANCE (TA = 25°C, VCC=3.3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	-	-	8	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	-	8	pF

Note:
1. These parameters are characterized and not 100% tested.

5.7 READ/PROGRAM/ERASE PERFORMANCNE

(Industrial: T_A=-40 to 85℃, Automotive, A1: T_A=-40 to 85℃, Vcc=2.7V ~ 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	cycle
Block Erase Time	tBERS	-	4	10	ms
Data Transfer from Cell to Register with Internal ECC	tRD	-	-	100	us

5.8 GENERAL TIMING CHARACTERISTICS

Parameter	Symbol	Min	Max
Clock frequency	f_C		104MHz
Hold# non-active hold time relative to SCK	t_{CD}	4.5ns	
Hold# hold time relative to SCK	t_{CH}	4.5ns	
Command deselect time	t_{CS}	100ns	
CS# setup time	t_{CSS}	5ns	
CS# hold time	t_{CSH}	5ns	
The last valid Clock low to CS# high	t_{CSCL}	5ns	
Output disable time	t_{DIS}		20ns
Hold# non-active setup time relative to SCK	t_{HC}	4.5ns	
Hold# setup time relative to SCK	t_{HD}	4.5ns	
Data input setup time	t_{SUDAT}	2ns	
Data input hold time	t_{HDDAT}	3ns	
Output hold time	t_{HO}	0ns	
Hold# to output Hi-Z	t_{HZ}		7ns
Hold# to output Low-Z	t_{LZ}		7ns
Clock low to output valid	t_V		8ns
Clock high time	t_{WH}	4.5ns	
Clock low time	t_{WL}	4.5ns	
Clock rise time (slew rate)	t_{CRT}	0.1V/ns	
Clock fall time (slew rate)	t_{CFT}	0.1V/ns	
WP# setup time	t_{WPS}	20ns	
WP# hold time	t_{WPH}	100ns	
Resetting time during Idle/Read/Program/Erase	t_{RST}		5/5/10/500us

Note:
1. For the first RESET condition after power up, tRST will be 1ms MAX.

6. Operations and Timing Diagrams

6.1 READ OPERATIONS AND SERIAL OUTPUT

The command sequence is as follows:

- 13th (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1)/ 3Bh (x2) / 6Bh (x4)

PAGE READ command requires 24-bit address with 8 dummy and a 16-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for t_R time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

READ FRAM CACHE command requires 16-bit address with 4 dummy bits and 12-bit column address for the starting byte. The starting byte can be 0 to 2111, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

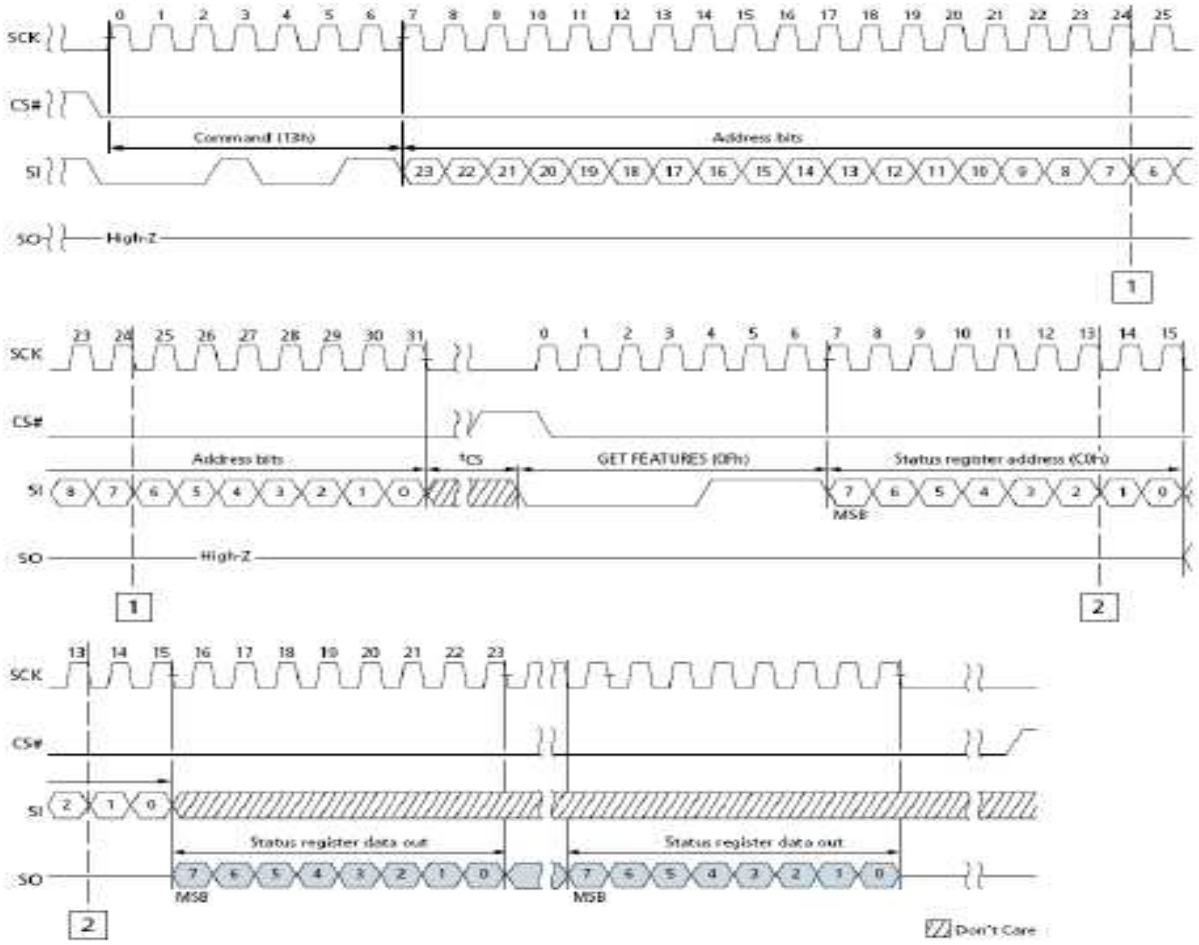


Figure 6.1 PAGE READ (13h) Timing

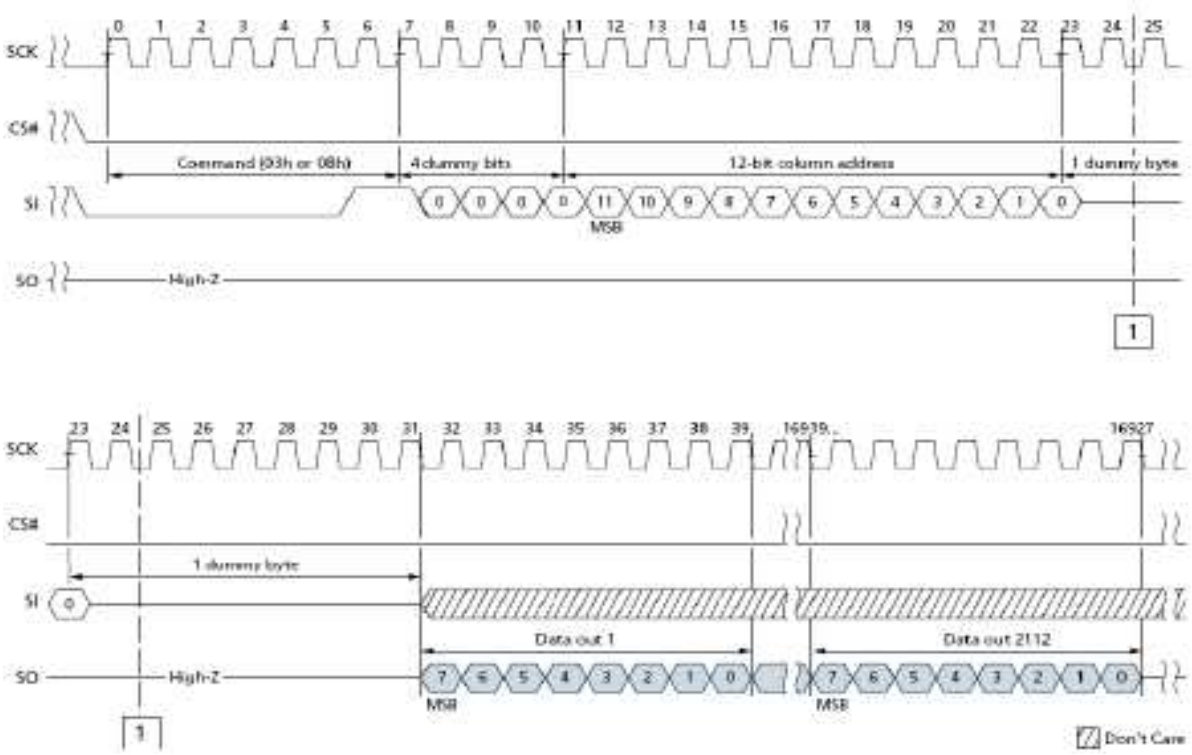


Figure 6.2 READ FROM CACHE (03h or 0Bh) Timing

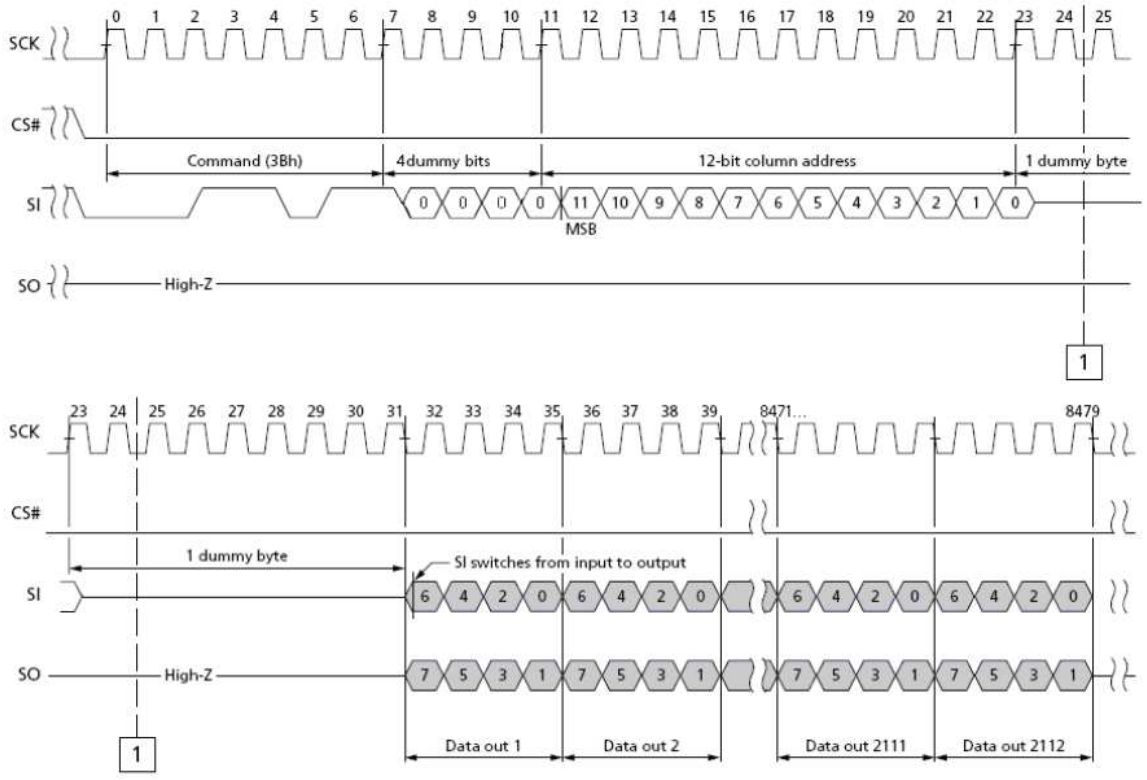


Figure 6.3 READ FROM CACHE x2 (3Bh) Timing

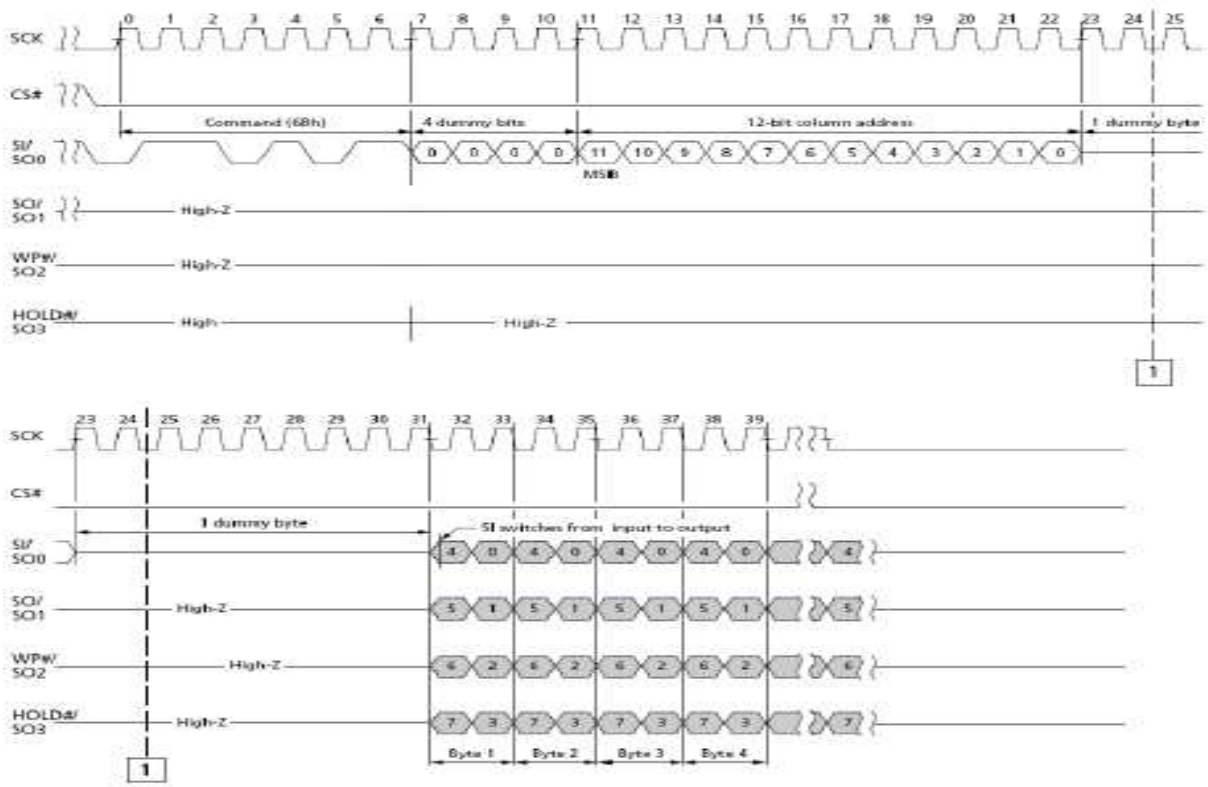


Figure 6.4 READ FROM CACHE x4 (6Bh) Timing

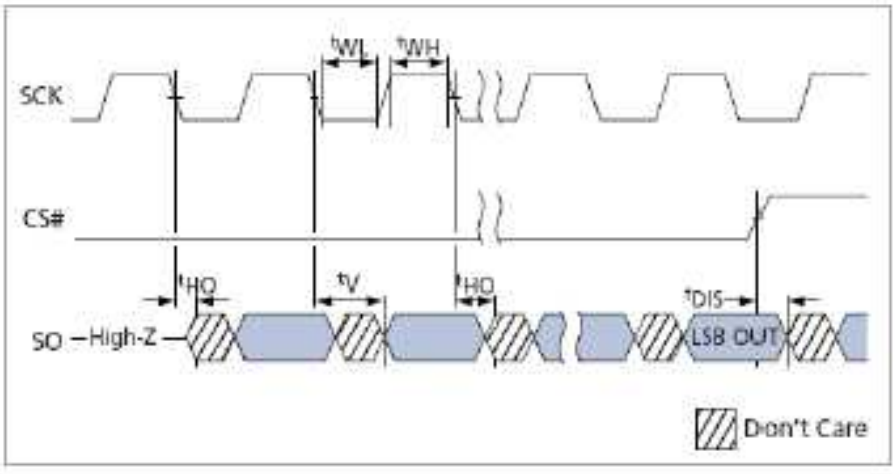


Figure 6.5 SERIAL OUTPUT Timing

6.2 PROGRAM OPERATIONS AND SERIAL INPUT

6.2.1 Page Program

The command sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The page program operation sequence programs 1 byte to 2112 bytes of data within a page. WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register.

After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 8 dummy bits and a 16-bit row address.

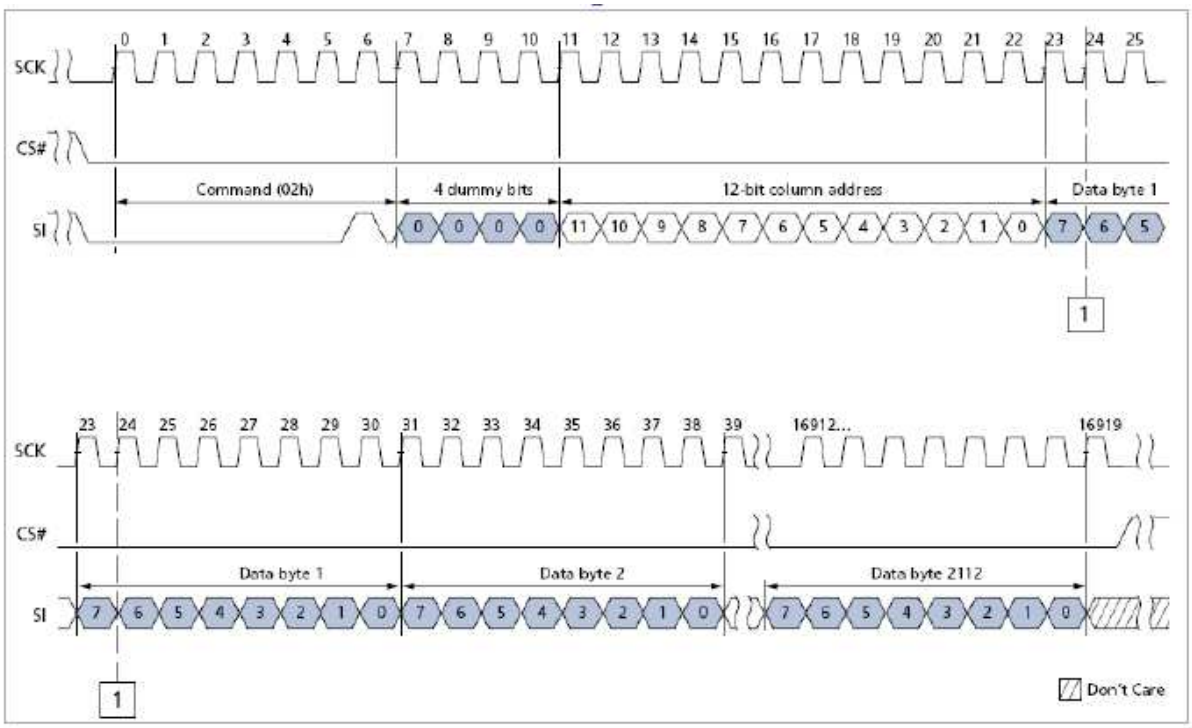
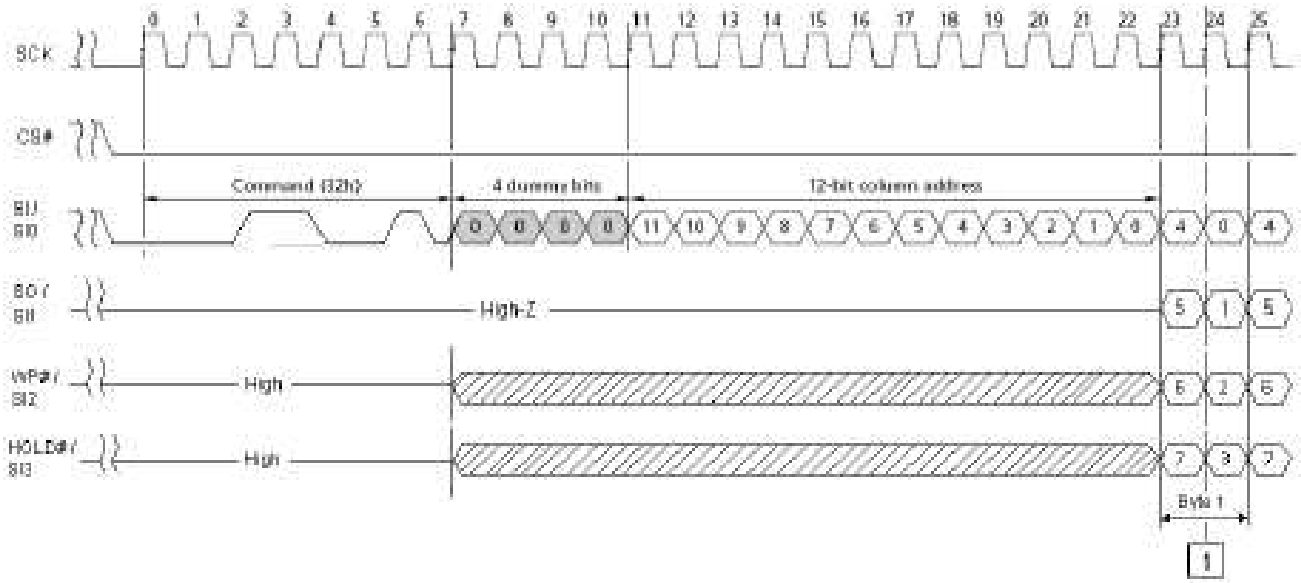


Figure 6.6 PROGRAM LOAD (02h) Timing



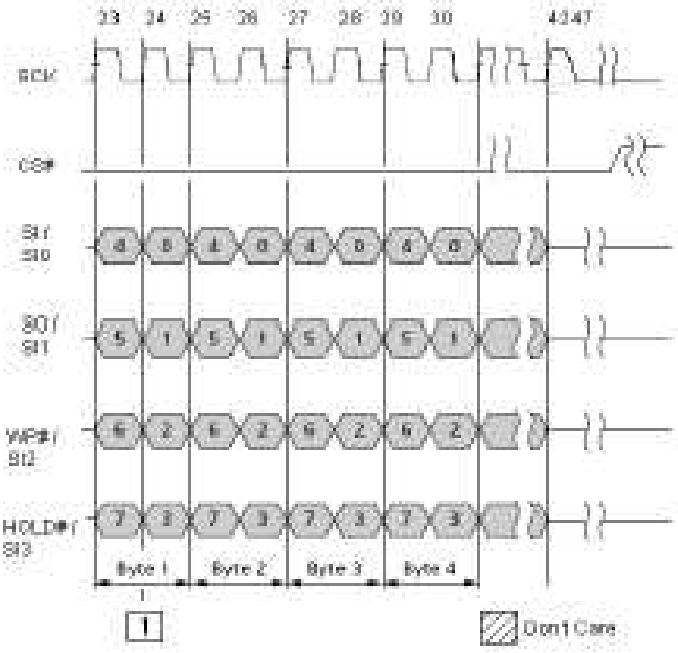


Figure 6.7 PROGRAM LOAD x4 (32h) Timing

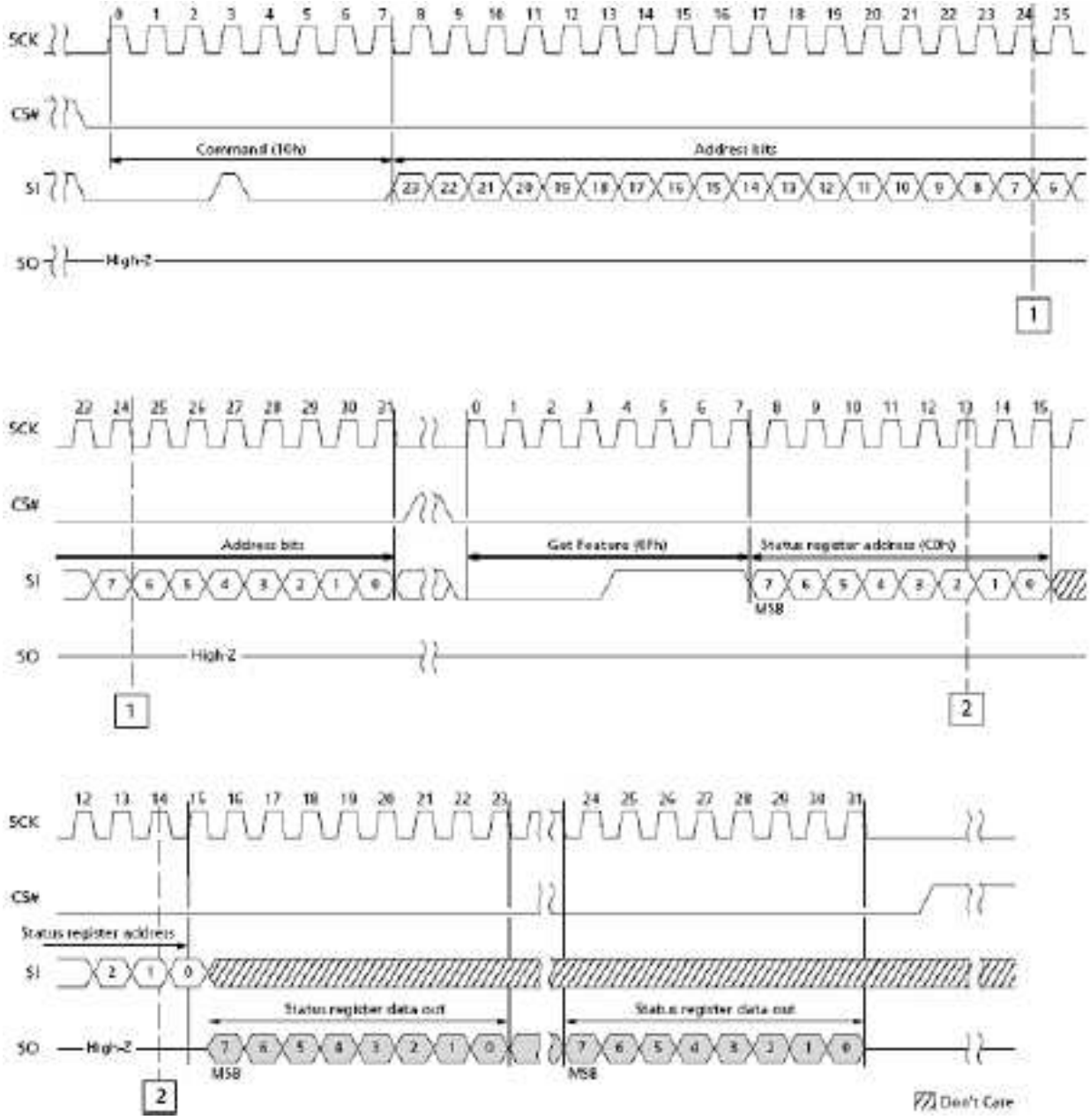


Figure 6.7 PROGRAM EXECUTE (10h) Timing

6.2.2 Random Data Program

The command sequence is as follows:

- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

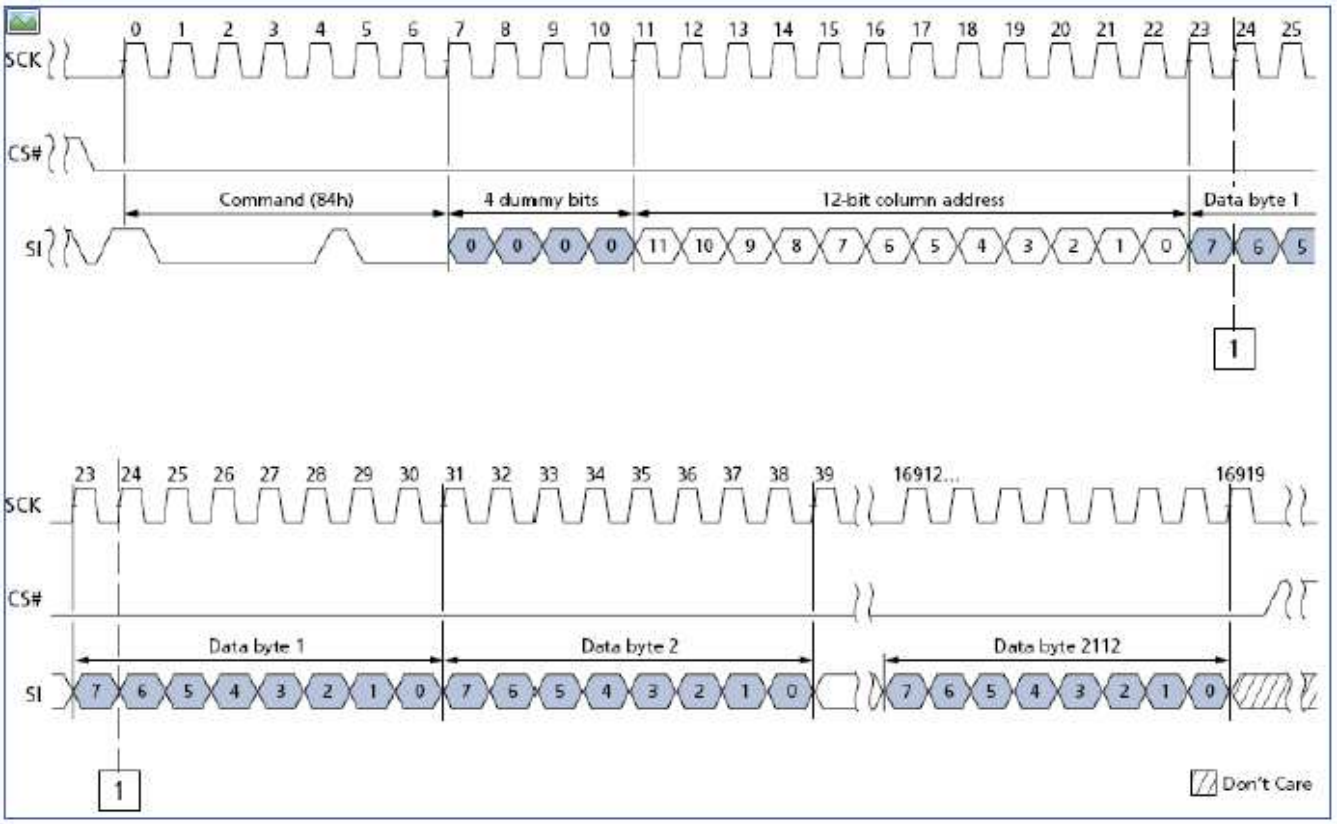


Figure 6.8 PROGRAM LOAD RANDOM DATA (84h) Timing

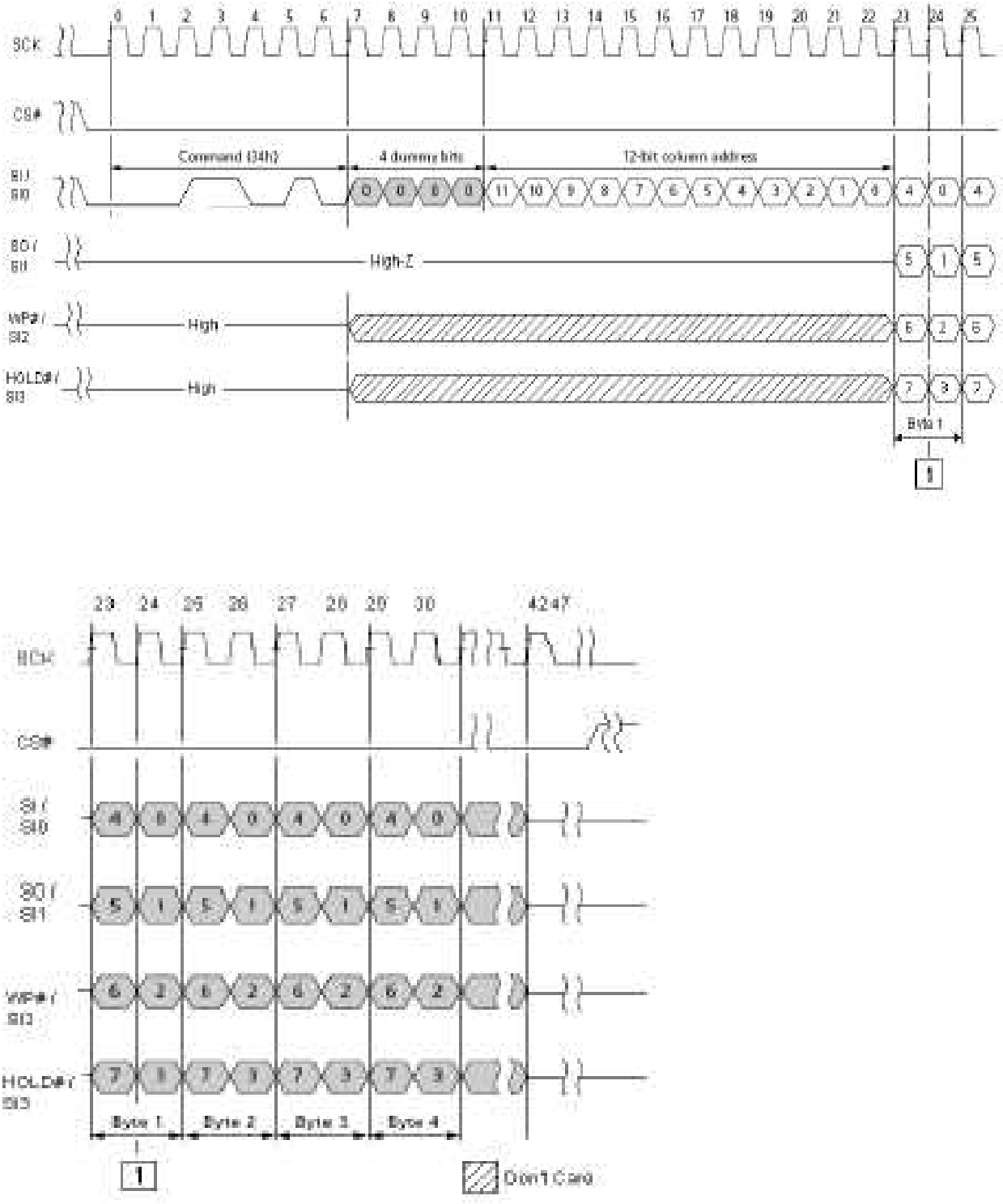
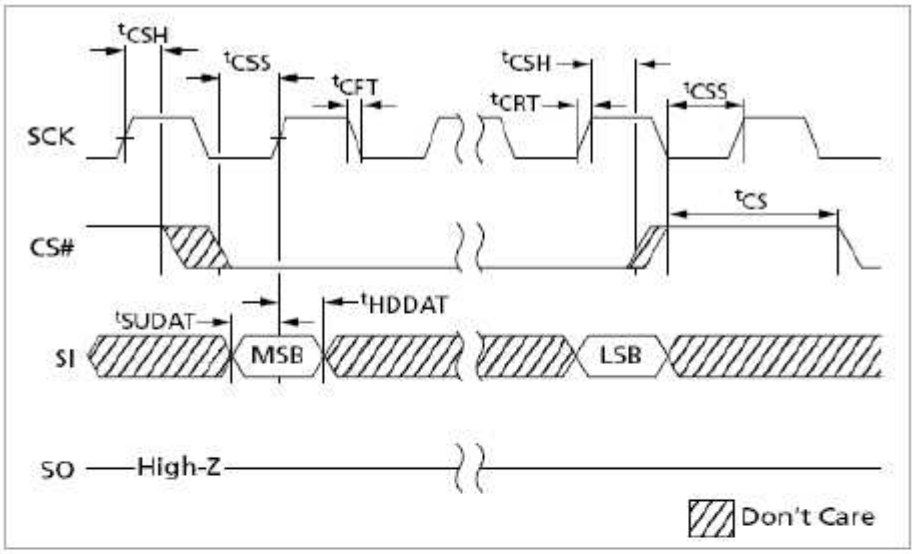


Figure 6.9 PROGRAM LOAD RANDOM DATA x4 (34h) Timing



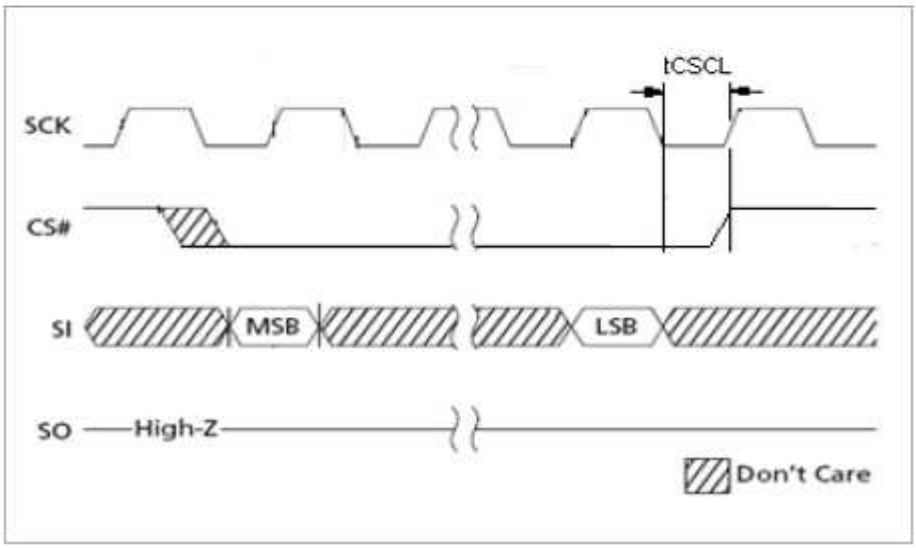


Figure 6.10 Serial Input and tCSCL Timing

6.3 INTERNAL DATA MOVE

The command sequence is as follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h(x4); this is OPTIONAL in sequence
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or replaces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

6.4 ERASE OPERATION

The command sequence is as follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 8 dummy bits and a 16-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

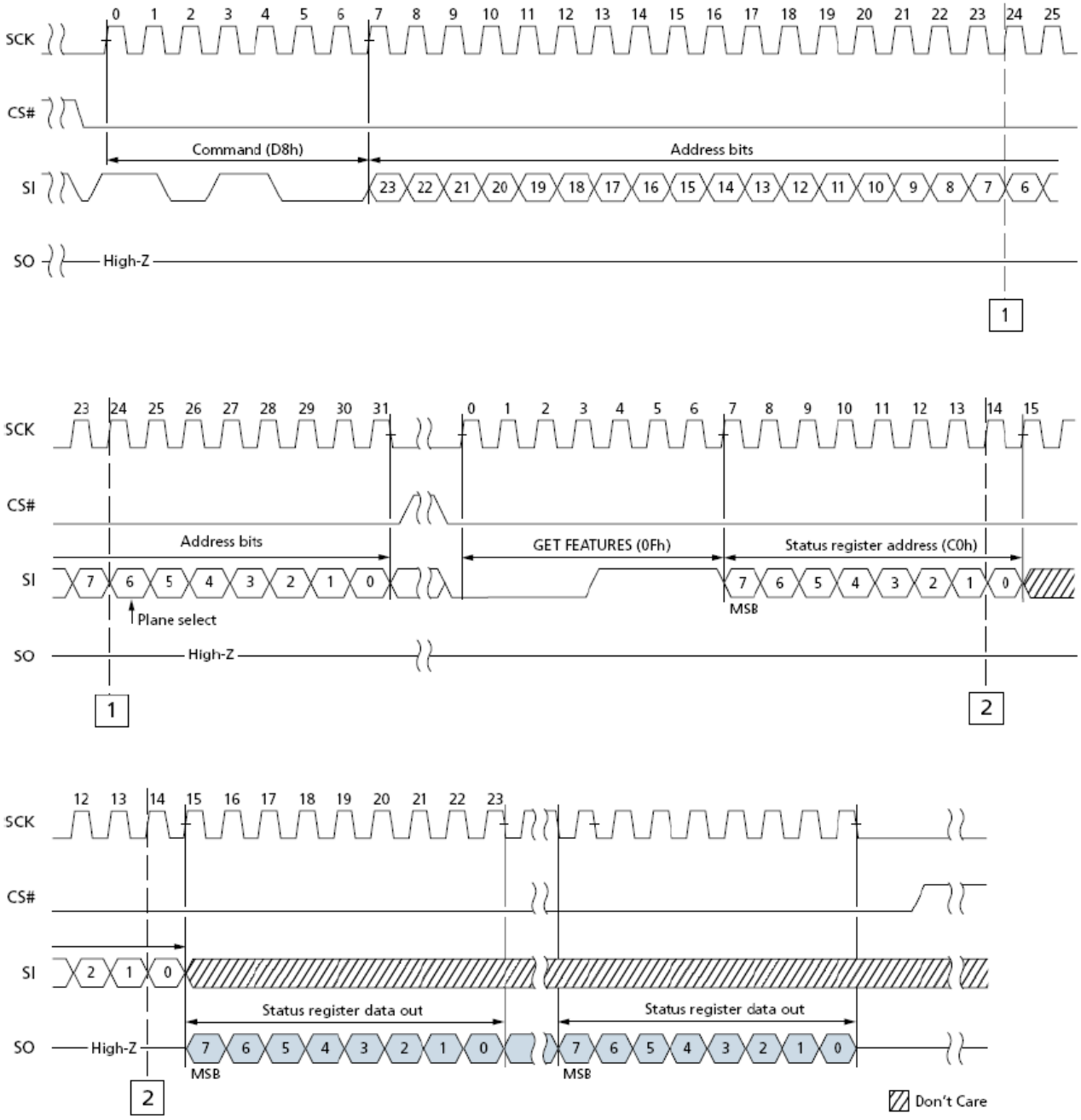


Figure 6.11 BLOCK ERASE (D8h) Timing

6.5 READ ID

The device contains a product identification mode, initiated by writing 9Fh to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h) and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode untial further commands are issued to it.

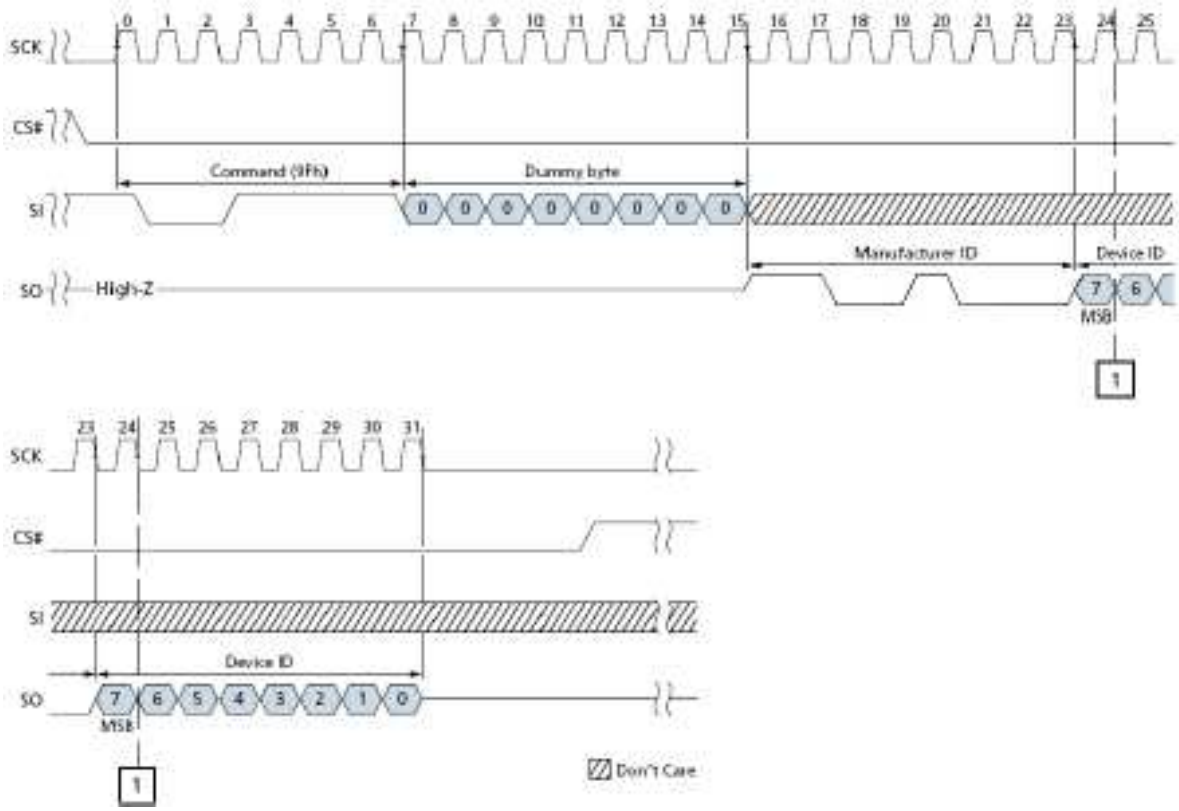


Figure 6.12 Read ID Timing

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
IS37/38SML01G1	C8h	21h	7Fh	7Fh	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	JEDEC Maker Code Continuation Code, 7Fh
4th Byte	JEDEC Maker Code Continuation Code, 7Fh
5th Byte	JEDEC Maker Code Continuation Code, 7Fh

Table 6.1 ID Definition Table